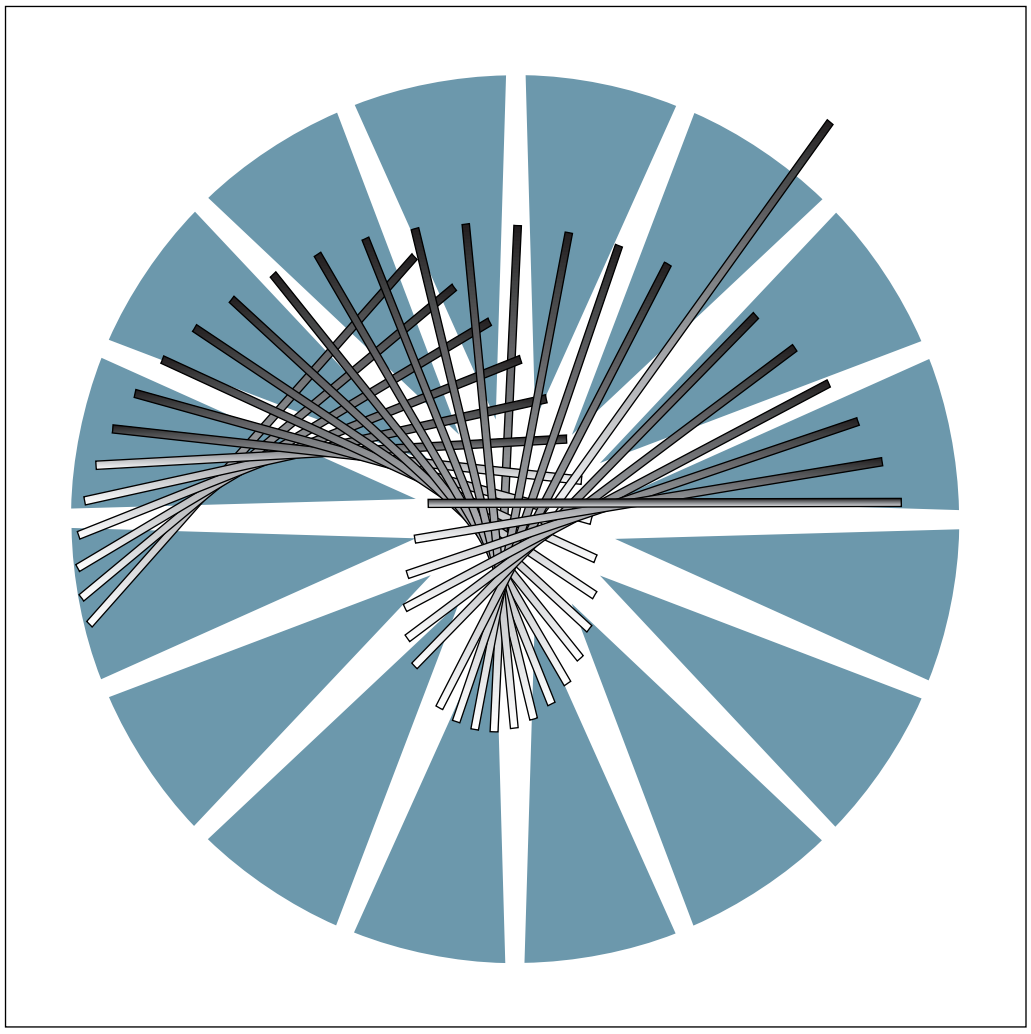
IBM 3745 Communication Controller
Models 210 to 61A

Maintenance Information Reference
Part 2



SY33-2056-8

IBM 3745 Communication Controller
Models 210 to 61A

Maintenance Information Reference
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SY33-2056-8

Note!

Before using this information and the product it supports, be sure to read the general information under “Notices” on page ix.

Ninth Edition (October 1993)

The information contained in this manual is subject to change from time to time. Any such changes will be reported in subsequent revisions. Changes have been made throughout this edition, and this manual should be read in its entirety.

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Contents

Part 1

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Part 2

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Product Safety Information

General Safety

This product meets IBM* safety standards.

For general safety information, see:

- *Telecommunication Products Safety Handbook,* GA33-0126

Safety Notices

See *Safety Notices* located at the beginning of the *Maintenance Information Procedures* manual, SY33-2054.

Service Inspection Procedures

The Service Inspection Procedures helps service personnel check whether the 3745 conforms to IBM safety criteria. They have to be used each time the 3745 safety is suspected.

The *Service Inspection Procedures* section is located at the beginning of the *3745 Maintenance Information Procedures (MIP)* manual.

The 3745 areas and functions checked through service inspection procedures are:

1. External covers
2. Safety labels
3. Safety covers and shields
4. Grounding
5. Circuit breaker and protector rating
6. Input power voltage
7. Power-ON indicator
8. Emergency power OFF.

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About This Book

This manual provides:

1. Introductory and how-to-fix information
2. Information for maintaining CSAs (Common Sub-assemblies)
3. Description of IBM 3745 Communication Controller functional units.

The console(s) and operator panel procedures are not provided in this manual, but are provided in the:

- *3745 Advanced Operations Guide*, SA33-0097, and *3745 Service Functions*, SY33-2055, for the maintenance functions used by service personnel.
- *3745 Basic Operations Guide*, SA33-0098, for the control panel functions.

Who Should Use This Book

This manual is intended for the product support-trained CE (PST CE) to service the IBM 3745 Communication Controller whenever the product-trained CE (PT CE) cannot repair the machine using the *Maintenance Information Procedures* (MIP) manual.

The person using this *Maintenance Information Reference* (MIR) manual should:

- Have an understanding of the telecommunications environment.
- Be trained to service the 3745 Communication Controller.
- Be familiar with the data circuit terminating equipment (modems, autocall units, and so on) and the terminals that attach to 3745s.
- Be familiar with the host channel to which the 3745 can be attached.

Service Personnel Definition

See *Maintenance Information Procedures* manual.

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How to Use the Maintenance Library

Maintenance on the 3745 is performed only when a failure or suspected failure occurs in the machine. The customer is first expected to perform problem determination to see if a 3745 problem exists. He uses the *Problem Determination Guide* and a host or 3745 console to perform the requested procedures. The problem determination guide generally produces a reference code that the customer should provide to the Hardware Central Service (HCS)

If the HCS is contacted, they will confirm that the initial problem determination has been done correctly, and determine if a hardware failure is indicated. Where hardware replacement is required, the HCS will determine which FRU(s) should be replaced, and dispatch a CE with the information needed to identify and replace them. When replacement has been completed, the CE will test the machine as directed by the *MIP* and *Service Functions* manuals, to verify the repair.

At this point, the *Maintenance Information Procedures* portion of the 3745 Maintenance Library has been exhausted. If additional problem analysis is required, the CE should contact the HCS for assistance, since the problem may require special tools or techniques that are described in the *Maintenance Information Reference* and *Service Functions* manuals, and are applied by a Product Support-Trained CE.

For more details, see "Maintenance Philosophy" in Chapter 1.

Where to Find More Information

See "Bibliography" page X-17.

Summary of Changes

This revised edition gives information concerning the 3745 Models 21A, 31A, 41A, 61A and the 3746 Model 900 connection.

This revised edition also gives information on 3746-900 expansion enclosure and new 3746-900 line processor (CLP) and line couplers (LIC type 11 and LIC type 12).

This edition also corrects minor errors or omissions.

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Part 2

Part 2 contains Chapters 07 to 14, the Abbreviation list, Glossary, and Index.

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Chapter 7. Channel Adapter (CA)

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The Channel Adapter in 3745 Data Flow

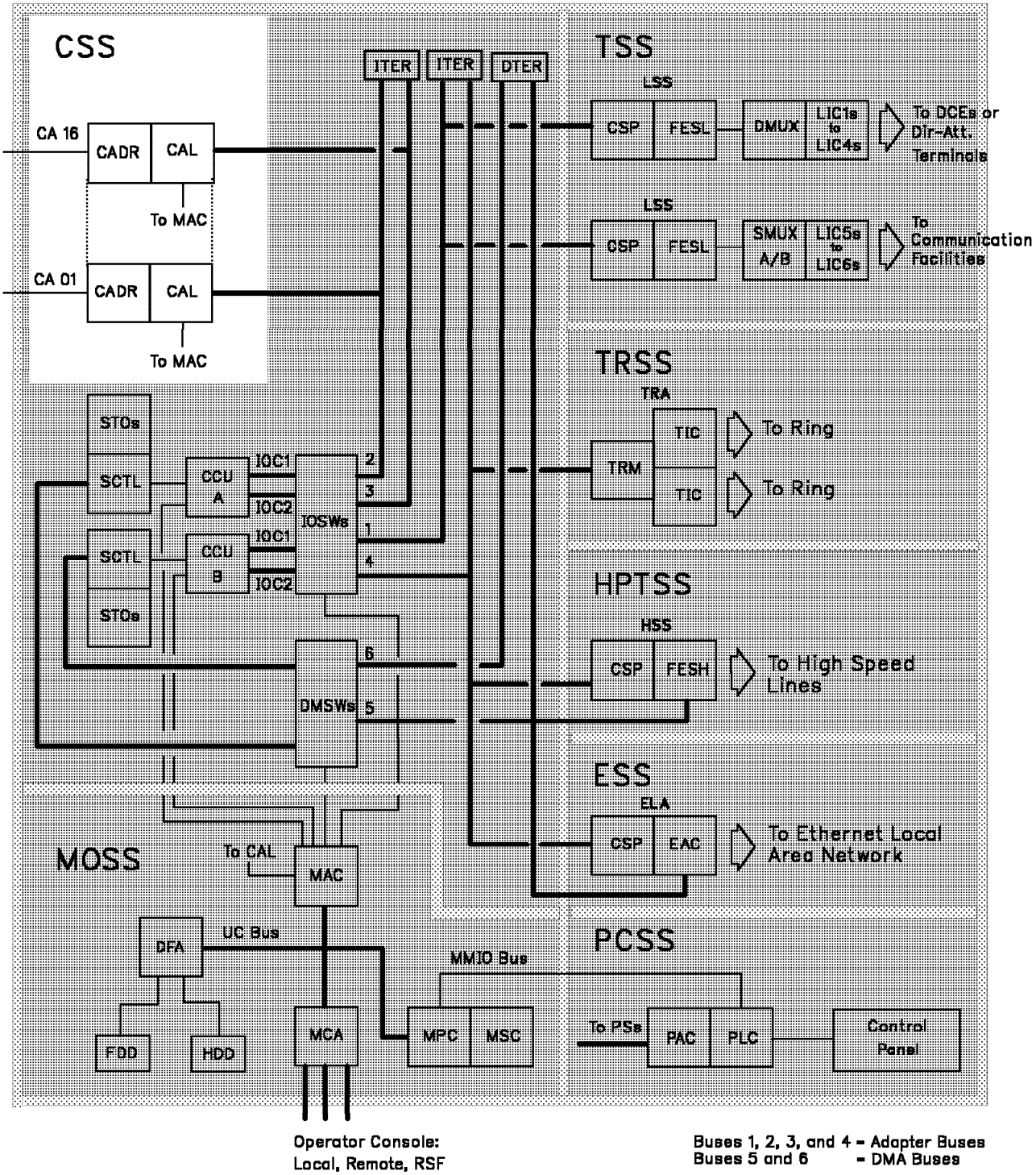


Figure 7-1. The Channel Adapter in 3745 Data Flow. For models 21A-61A, DMA and IOC buses are connected to the CBC in the 3746-900. The MCA card is replaced by the MLA card which interfaces to the MPC card through the MMIO bus. This MLA card links the MOSS to the Service Processor through a LAN.

Introduction

The microcoded CA attaches the 3745 Communication Controller to one or more System 3033 (for **CADS** only) /308X/309X/4341/4361 (for **CADS** only) /4381/9370/ES/9000 host processors via selector, block multiplexor, or byte multiplexor channels.
The 3745 supports the channel adapter data streaming (**CADS**, CA type 6), and the buffer chaining channel adapter (**BCCA**, CA type 7).

From the 3745 MOSS console, an operator can:

- Enable/disable a CA
- Reset a CA
- Display a CA status
- Display CA storage and registers
- Display CA initialization parameters
- Enter/modify CA initialization parameters
- Get a CA dump
- Start/stop a CA trace
- Allow CA concurrent maintenance.

Buffer Chaining Channel Adapter (BCCA)

The **BCCA** is a new type of channel adapter with improved performances. The BCCA is based on CADS design and improves the CADS throughput and channel efficiency. Without NCP intervention, the BCCA handles buffer chaining in write channel program, and both buffer chaining and PIU chaining in read channel program.

BCCA and CADS may be mixed in the 3745. The BCCA operates in native mode only under the Network Control Program (NCP), it does not support the Partitioned Emulation Program (PEP).
The BCCA acts as a CADS when buffer chaining mode is not set, except that it does not support ESC mode.

Note:
In the following pages, specifics of a **type 7 CA** will be indicated by **BCCA.**
CA stands for **CADS** and **BCCA**.

Packaging

One CADS or BCCA is packaged on one channel adapter logic (CAL) card, and one channel adapter driver/receiver (CADR) card. (See page YZ 037 for CA board and connector locations, and page YZ 337 for test points.)

A built-in two-processor switch (TPS) feature is available. The TPS allows a single CA to connect two separate host channels, or two channels of a single host. A CA can have two host interfaces (TPS operative) by adding a second CADR card.
Only odd-numbered CAs support the TPS feature (see Figure 7-3 on page 7-8). If a CA is equipped with the TPS support, the next CA cannot be installed. A bypass card assuring serial line continuity must be installed instead.

Refer to Figure 7-4 on page 7-9 for a diagram of components and interconnections.

Supported Features

The following features are supported by **CADS** and **BCCA**:

- I/O error alert
- Two-processor switch (TPS)
- High speed transfer (Data in/Data out)
- Buffer chaining (BCCA only)
- Data streaming with selectable speeds for 1 MB, 2 MB, 3 MB or 4.5 MB channel speed. These values are the host channel speeds, not the actual transfer rates which are much lower. (The 3745 may be connected to a 4.5 MB channel attachment even if operating at its own speed. In this case, it must be attached beyond the last control unit on the I/O interface which is capable of the 4.5-MB data-transfer rate.)

  WARNING: Data streaming cannot be used when the 3745 is connected to systems 3033, 308X or 43XX. When a CA defined with the data streaming option is connected to a host which does not support data streaming, abend code 300A is issued.

Non-Supported Features

The following features are not supported:

- Bus extension
- Command retry
- Suppress data (interlock transfer)
- Dynamic reconnection

Configuration

Eight channel interfaces are available via the IOC BUS. In the base frame 01 or adapter frame 02, the maximum configuration is eight CAs without TPS, or four CAs with TPS. Thus, a maximum of 16 channel interfaces may be installed on a 3745, numbered from 1 to 16.

Since the Control Program (CP) can address only eight CAs via the IOC BUS, conventional numbering has been chosen as shown in Table 7-1. The CP address is used with input instructions X'0E'and X'0F', and output X'07' and X'40'.

Table 7-1. CA Numbering

CP Address	Numbering used by the 3745 for Adapter Bus 2	Numbering used by the 3745 for Adapter Bus 3
000	CA 1	CA 5
001	CA 2	CA 6
010	CA 3	CA 7
011	CA 4	CA 8
100	CA 9	CA 13
101	CA 10	CA 14
110	CA 11	CA 15
111	CA 12	CA 16

The following table shows to which IOC are connected Adapter Bus 2 and Adapter Bus 3, depending on the operating mode of the controller:

Operating Mode	**Adapter Bus 2 is connected to**	**Adapter Bus 3 is connected to**
Single	IOC2 of CCU A	IOC1 of CCU A
Twin Dual or Twin Backup	IOC2 of CCU A	IOC1 of CCU B
Standby (A Active or Fallback on A)	IOC2 of CCU A	IOC1 of CCU A
Standby (B Active or Fallback on B)	IOC2 of CCU B	IOC1 of CCU B

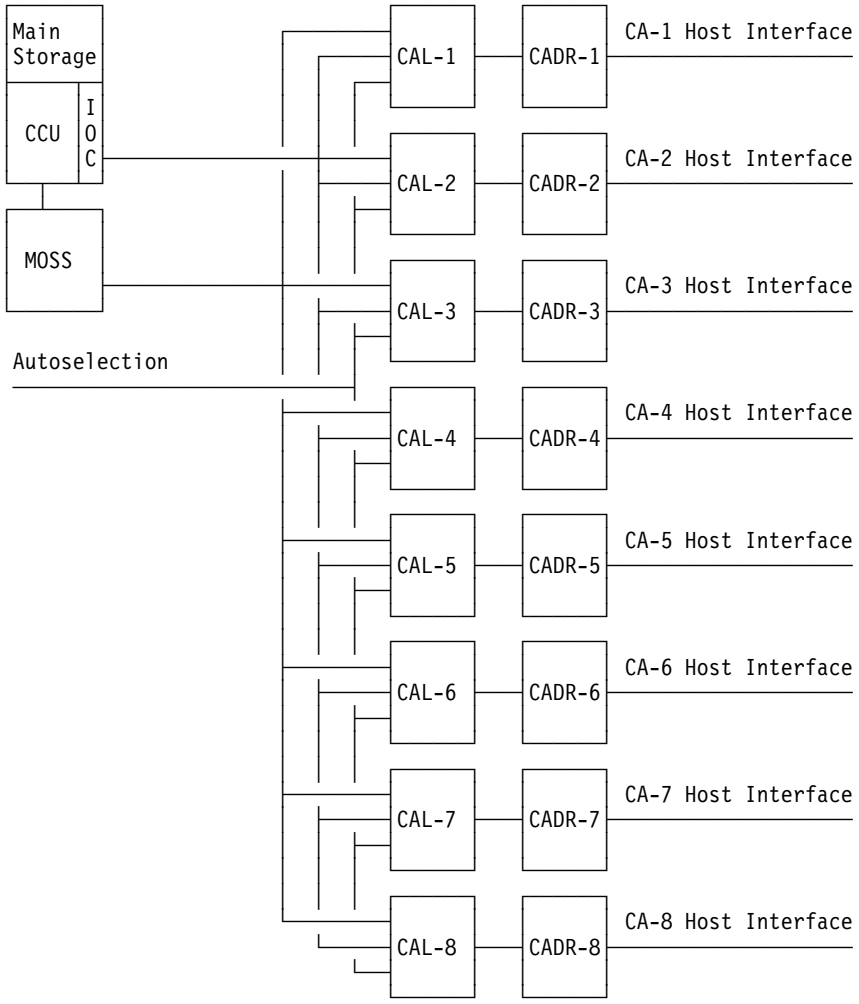


Figure 7-2. Example of a CA Configuration without TPS Feature

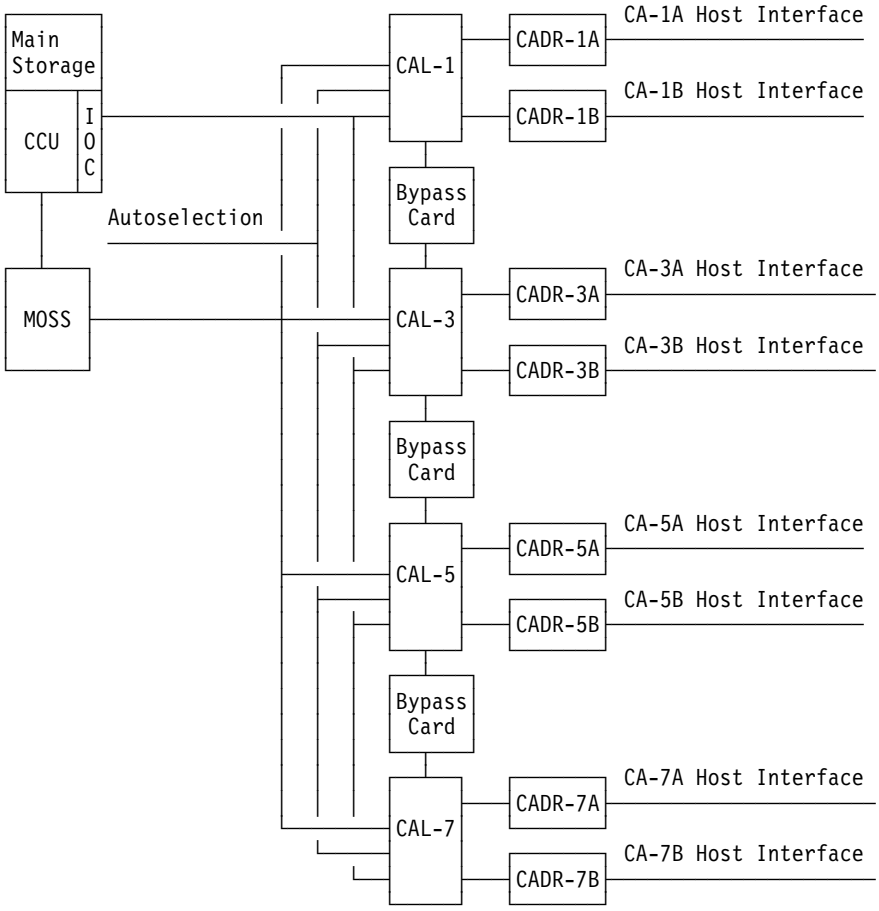
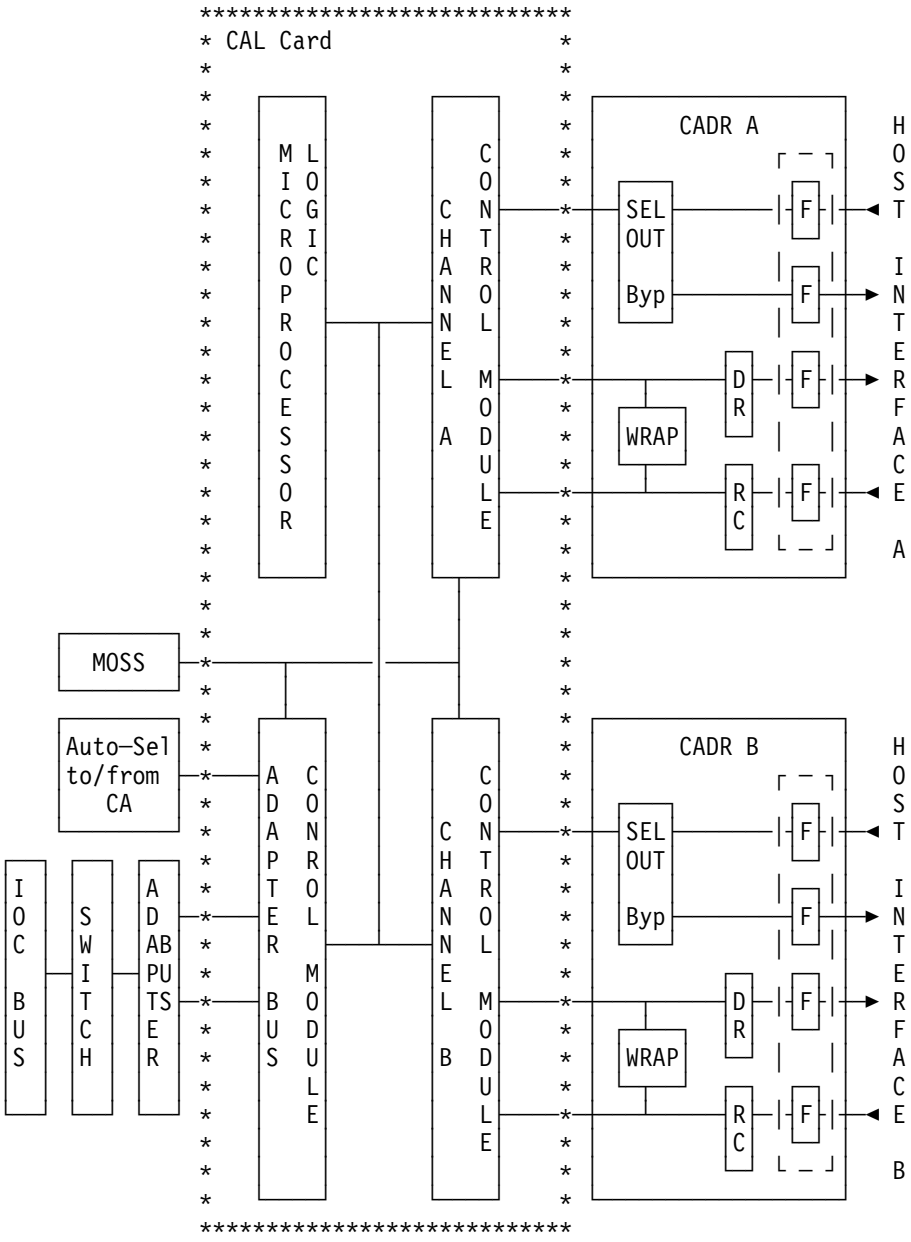


Figure 7-3. Example of a CA Configuration with TPS Features Installed



F = Fuse only for UK (CADRUK Card only)

Figure 7-4. CA Components and Data Flow

CA Operating Environment

The CA is used by the 3745 control program (NCP or PEP) to communicate with an application program in the host(s) through various telecommunication access methods.

Physically, channel interface tags and buses attach the CA to the host channels, and IOC buses attach the CA to the CCU.

Modes of Operation

The CA can run in either native subchannel (NSC) mode or in emulation subchannel (ESC) mode. The CA operates in the following modes:

- NSC with the Network Control Program (NCP)
- NSC and ESC simultaneously with the Partitioned Emulation Program (PEP)

Notes:

1. With PEP, the NSC is used for loading and dumping.
2. Initial program load (IPL) must always be done in NSC mode.
3. **BCCA** works only in native mode (NCP).

NSC Mode

The NSC mode is supported for all types of host channel (byte multiplex, selector, or block multiplex), and allows servicing any number of lines using only one host subchannel address. Line address decoding is handled entirely by the NCP.

ESC Mode

The ESC mode is supported for byte multiplex channels only, and allows the controller to emulate the 2701 Data Adapter Unit, 2702 Transmission Control, and 2703 Transmission Control using existing host programs and subchannel addresses. This mode requires the Partitioned Emulation Program (PEP) in the 3745, and a separate subchannel address for each PEP line. The ESC mode is not supported with **BCCA.**

Host Unit Control Word (UCW)/Host I/O Configuration Data Set (IOCDS)

The host system UCW/IOCDS requirements for the controller vary according to the type of control program and features. They are described in the appropriate host *I/O Configuration Program (IOCP) User's Guide and Reference*. UCW/IOCDS requirements are determined as follows:

- One UCW/IOCDS is required for each unique NSC address.
- An additional UCW/IOCDS is required for each emulated subchannel address. For example, a controller running PEP with two ESCs needs three UCW/IOCDS.
- All UCW/IOCDS must be unshared and unfolded.

Overall Operation

The CA is connected to the 370 channel and to the IOC bus, and enables communications over these two data paths.

Data Transfer Methods (PIO and AIO)

Two methods are used to transfer data between the CA and the CCU (via the IOC bus, the switching device, and the adapter bus):

- **Program-initiated operation (PIO):**

  PIO mode provides data buffering for up to four bytes, with program intervention required every four bytes.

  PIO mode may be used when performance is not critical.

- **Adapter-initiated operation (AIO):**

  – When the buffer chaining mode is not set, AIO mode provides a 255-byte buffering. A program intervention is required after each 255-bytes transfer.
  – When the buffer chaining mode is set, **BCCA** provides two 255-bytes buffers. A program intervention is required at end of PIU in the write channel program, or at end of PIU chain in the read channel program.

  AIO mode should always be used when performance is critical.

CA Instructions

The CA is controlled by instructions issued from the control program.

The NCP and PEP exclusively use adapter input/output halfword (IOH) instructions and input/output immediate halfword (IOHI) instructions.

These instructions examine or set the CA registers, load or read buffers, and initiate cycle stealing.

Note: Throughout this chapter, the channel IOH/IOHI instructions are referred to as input X'nn' or output X'nn'.

CA States

The CA may be in one of the following states:

- **Ready**

  In the ready state, the CA accepts instructions, but is not in one of the three active states (initial selection, data transfer, or status transfer).

- **Initial Selection**

  The CA enters the initial selection state when an initial selection is started by the host processor. The CA continuously monitors its channel interface for one of its assigned addresses. When it detects one of these addresses, the CA enters the initial selection state, and proceeds with the operation.

- **Data Transfer**

  The CA enters the data transfer state when the control program initiates a data transfer sequence. Data is transferred across the interface from the host channel to the CA, or from the CA to the host, by the hardware.

- **Status Transfer**

The CA enters the status transfer state when the control program initiates a status transfer sequence.

- **Disabled**

  When the CA is in the disabled state, it does not reply to selection signals coming from the host.

CA Interrupt Requests

The CA can raise interrupt requests to the CCU at level 1 and level 3 (normal mode), and interrupt requests to MOSS at level 1 and level 4 when the MOSS is the owner of the resource.

- **Level 1 Interrupt**

  Level 1 interrupt requests to the CCU are caused by check or error conditions.

  Level 1 interrupt requests to MOSS are caused by check or error conditions when the MOSS is the owner of the resource (IPL or concurrent maintenance).

- **Level 3 Interrupt**

  (See “Level 3 Interrupt Request” on page 7-48.) Level 3 interrupt requests are caused by:

  1. Initial selection interrupt requests.
  2. Data/status interrupt requests.

- **Level 4 Interrupt**

  Level 4 interrupt requests are raised to MOSS in diagnostic mode only.

Accessing CA Registers

The CA registers are accessed by:

- CCU input/output (IOH) or input/output immediate (IOHI) instructions from the CP.
- MOSS input/output (MIOH) instructions, used to initialize or diagnose the CA from MOSS.
- The operator selecting the CA services when using MOSS functions.

The CCU IOH and IOHI instructions are used to transfer the contents of one of the CCU general registers to a selected CA register, or conversely. All instructions are described in this chapter.

Channel Interface Tag Signals Used by the CA

Address in

Address out

Bus in

Bus out

Command out

Data in [1]

Data out [1]

Disconnect in

Operational in

Operational out

Request in

Select in

Select out, and Hold out

Service in

Service out

Status in

Suppress out

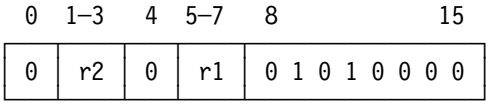
[1] Used only with 'High Speed Transfer' and 'Data Streaming' options.

Input/Output Instruction Format

IOH and IOHI (IOH Immediate) instructions are transferred in PIO mode between the CCU and the CA. MIOH (MOSS IOH) instructions are transferred in PIO mode between the MOSS and the CA.

To respond to a command, a CA must first have been selected via an output X'07' instruction, except for input commands X'07', X'08', X'0E' and X'0F' which are broadcast commands addressing all CAs.

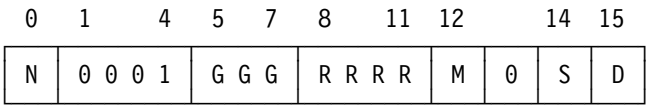
IOH/MIOH Instruction Format



At TD time, this halfword instruction transfers the contents of a CCU register specified by the r1 field of the instruction (bits 5-7) to the selected CA register, or places information coming from the selected CA register into the CCU register specified by the r1 field of the instruction. For the output commands X'07', X'40', and the inputs X'0E', X'0F', the CA selection is executed at TD time of the instruction with R1 register bits 4-6 (used to address the CA to be selected).

The IOC bus number, command/register number, and data movement direction are indicated by the contents of register R2, specified by the r2 field (bits 1-3) of the instruction. The R2 register contents are sent over the IOC bus at the TA instruction time.

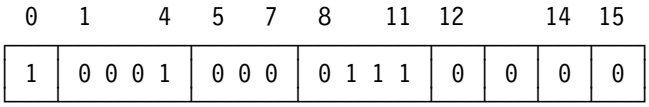
R2 Contents at TA Time:



- Bit 0 (N) indicates the UC bus number (0 = IOC1, 1 = IOC2).
- Bits 1-4 (0001) indicate a CA instruction (address type).
- Bits 5-7 (GGG) indicate the register group if bit 14 (S) is zero.
  - GGG = 000 indicate X'0n' register group as listed on page 7-16.
  - GGG = 001 indicate X'1n' register group. These registers are hardware registers in the adapter bus control module (CAL card).
  - GGG = 010 indicate X'2n' register group. These registers are hardware registers in the channel A control module (CAL card).
  - GGG = 011 indicate X'3n' register group. These registers are hardware registers in the channel B control module (CAL card).
  - GGG = 100 indicate X'4n' register group.
  - GGG = 101 indicate X'5n' register group.
  - GGG = 110 indicate X'6n' register group.
- Bits 8-11 (RRRR) are associated to the group and indicate the register unit position if bit 14 (S) is zero.
- Bit 12 (M), if set to 0, indicates instruction coming from CCU; if set to 1, indicates instruction coming from MOSS.

- Bit 14 (S), if set to 1, permits data storage read/write (1 = CA storage 255-byte buffers, 0 = registers).
- Bit 15 (D) indicates input or output direction (1 = in, 0 = out).

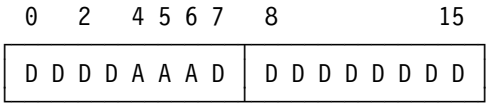
Example of R2 Contents at TA Time for an Output X'07':



- Bit 0 = 1 indicates IOC2 of the active CCU.
- Bits 1-4 = 0001 is the address type (indicate a CA instruction).
- Bits 5-11 = 0000111 indicate the X'07' command/register.
- Bit 12 = 0 indicates instruction coming from CP.
- Bit 15 = 0 indicates an output command.

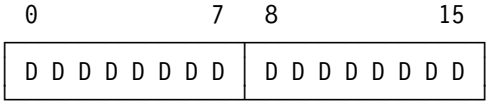
Bus Contents at TD Time (R1 Register)

- For the output commands X'07', X'40' and the input commands X'0E', X'0F', at TD time the bus contents are the following:



  - D is information data depending on the executed command.
  - Bits 4-6 (AAA) indicate the selected CA address.

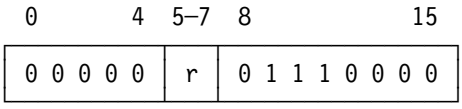
- For all other instructions, the bus contents at TD time are data pertaining to the executed instruction:



IOHI Instruction Format

This **fullword** instruction transfers the contents of a CCU register specified by the r field (bits 5-7) to the CA register, or places information coming from the CA into the CCU register specified by the r field. The CA register and the direction of data movement are both specified by the contents of the second halfword.

IOHI First Halfword:



IOHI Second Halfword: The second halfword contents are similar to the contents of register R2 in IOH instructions. See “R2 Contents at TA Time” on page 7-14.

CA Instructions (Register Contents)

The CA contains X'nn' registers that are accessible by MOSS or the CP. Register contents are listed hereafter in this chapter.

Register Group X'0n'

Details on bits can be found in the *3745 Principles of Operation*, GA33-0102.

Bits 5-7	Bits 8-11	Input Reg N°	Output Reg N°	Register Function
000	0000	X'00'		Initial Selection Control
000	0000		X'00'	Reset Initial Selection
000	0001	X'01'		Initial Selection Address and Command
000	0001		X'01'	Diagnostic Command or NCP Buffer Control (**BCCA**)
000	0010	X'02'	X'02'	Data/Status Control
000	0011	X'03'	X'03'	ESC Address and Status Byte or VTAM Buffer Length (**BCCA**)
000	0100	X'04'	X'04'	PIO Data Buffer (Bytes 1-2)
000	0101	X'05'	X'05'	PIO Data Buffer (Bytes 3-4)
000	0110	X'06'	X'06'	NSC Status/Control
000	0111	X'07'	X'07'	CA Controls
000	1000	X'08'		Autoselection Chain Check
000	1001	X'09'		Autoselection Chain Status
000	1001		X'09'	Bypass CA from Autoselection Chain
000	1010	X'0A'		Cycle Steal Chain Status
000	1010		X'0A'	Bypass CA from CS Chain
000	1011	X'0B'	X'0B'	ESC Test I/O Address and Status (CADS) (Invalid command for **BCCA**)
000	1100	X'0C'	X'0C'	Cycle Steal Mode Control (CADS)
000	1101	X'0D'		CA Check
000	1110	X'0E'		CA L1 Interrupt Requests
000	1111	X'0F'		CA L3 Interrupt Requests - Autoselection

Register Group X'1n'

X'1n' instructions are MIOH instructions reserved for diagnostic purposes. They allow access to hardware registers of the adapter bus control module.

Reg N°	Register Function
X'10'	UC Bus State
X'11'	Interrupts to CP/MOSS
X'12'	UC Bus Sense Register
X'13'	CP/MOSS address - CAL card EC
X'14'	AS/CS Chains
X'15'	CS Index - Data Index - Diag
X'16'	IOH/MIOH Validation - Autoselect State
X'17'	CS Burst Counter - RAM Address Counter
X'18'	Bus Adapter Module Interrupt - μP Commands
X'19'	TA Register
X'1A'	TD Register
X'1B'	UC Bus Tag Out
X'1C'	UC Bus Tag In - MOSS Interface
X'1D'	Miscellaneous 1
X'1E'	Miscellaneous 2
	Cycle Steal Buffer Counter (**BCCA**)
X'1F'	CS interval timer (**BCCA**)

Register Groups X'2n', X'3n'

X'2n' instructions are MIOH instructions reserved for diagnostic purposes. They allow access to hardware registers of the channel A control module.

X'3n' instructions are MIOH instructions reserved for diagnostic purposes. They allow access to hardware registers of the channel B control module. Since channel A and channel B control modules are identical, to access a particular register of the channel B module, use an X'3n' instead of an X'2n' instruction.

Reg N°	Register Function
X'20'	Channel Control Module Interrupts
X'21'	Data Registers
X'22'	NSC Address - Host Interface Features
X'23'	ESC Address Range **(CADS)**
X'24'	CADR Card EC/Channel Module EC
X'25'	Logic Errors in Channel Module
X'26'	SIDI/SODO Counters
X'27'	Residual Byte Counter - RAM Address Counter
X'28'	RAM Index
X'29'	Timer Counters
X'2A'	μP commands - MOSS Commands
X'2B'	μP Commands - Character Monitoring
X'2C'	Data/Status Transfer States
X'2D'	Initial Selection State - Misc. States
X'2E'	Tags Out - Tags In
X'2F'	Miscellaneous

Register Group X'4n'

Reg N°	Register Function
X'40'	CP Address
X'41'	Interface A Host Parameters
X'42'	Interface B Host Parameters
X'43'	Interface A Channel Burst Length
X'44'	Interface B Channel Burst Length
X'45'	A Interface ESC Range **(CADS)**
X'46'	B Interface ESC Range **(CADS)**
X'47'	CS Burst Length
X'48'	Enable/Disable Channel Drivers/Receivers
X'49'	Basic CAL Card EC Sense
X'4A'	Microcode Level - TPS EC Sense
X'4B'	Checkout Result
X'4C'	Diagnostics
X'4F'	Channel Monitoring

Register Groups X'5n', X'6n', X'7n'

Reg N°	Register Function
X'50'	Adapter Bus Control Module Check
X'51'	Channel A Control Module Check
X'52'	Channel B Control Module Check
X'57'	Stop Trace
X'58'	Marker
X'59'	Trace Inhibit
X'5A'	Inhibit Trace Bit
X'5B'	Trace Address
X'5C'	Trace Area Page Address
X'5D'	Set Address Command
X'5E'	Data Register
X'5F'	Save Diagnostic Area
X'60'	Microcode-Detected Error Code
X'61' to X'7F'	Microcode information

CA Broadcast Commands

IOH CA commands Input X'07', X'08', X'0E', X'0F' and Output X'07' are recognized and executed by every CA on the IOC bus, whether selected or not. These commands are called 'broadcast commands'.

As each CA executes the broadcast command, the 'common valid feed auto' line is activated. Since this line is DOT-ANDed, the line goes active only when all CAs have executed and responded to the broadcast command.

During the IOH CA commands input X'07', X'08', X'0E' and X'0F', the CA DOT-ORes bits onto the IOC data bus. The parity bit is not generated. The parity valid (PV) tag is not raised because parity may be bad. The 'common valid feed auto' line signals that all bits have been placed on the IOC bus, and the selected CA validates the data to the CCU.

Validation Table

CA commands are checked against a command validation table which is loaded by the MOSS into the CA RAM at IPL time. This checking depends on:

1. Whether the command was issued by MOSS or by the CP,
2. The selection mode of the CA, functional or concurrent. Only the MOSS can select a CA in concurrent mode, when there is no risk of disturbing a normal CA operation, that is:
   - The CCU is not running, or
   - No control program is loaded, or
   - The CA is not initialized, or
   - The CA is not connected.

Input X'00': Initial Selection Control

Byte 0	Name	Byte 1	Name
0	Initial selection interrupt	0	Initial selection on interface B [3]
1	Interface disconnect	1	(Not used)
2	Selective reset	2	(Not used)
3	Channel bus out check	3	(Not used)
4	0 = NSC mode, 1 = ESC (Must be 0 with **BCCA**) [2]	4	(Not used)
		5	(Not used)
5	Stacked initial status byte	6	(Not used)
6	Status byte cleared	7	(Not used)
7	System reset		

Output X'00': Reset Initial Selection

This command resets all the initial selection hardware latches (bits 0.0 to 0.6 of the input X'00' register), as well as the initial selection interrupt request on level 3. Register bit settings are not relevant.

Note: For reset System Reset, output X'07' with byte 1, bit 3 = 1 is used.

Input X'01': Initial Selection Address and Command

Byte 0	Name	Byte 1	Name
0-7	Address byte	0-7	I/O command byte

Output X'01': Diagnostic Command (CADS) or NCP Buffer Control (BCCA)

This instruction is used to write register X'01' for diagnostic purposes only. With **BCCA**, this instruction sets the first NCP buffer control register.

- **CADS:**

Byte 0	Name	Byte 1	Name
0-7	Initial selection address byte	0-7	I/O command byte

- **BCCA**

Byte 0	Name	Byte 1	Name
0-7	First inbound offset	0-7	NCP buffer length

[2] **BCCA** supports only NCP.

[3] Bit used only in **BCCA** (0 = Initial selection occurred on interface A, 1 = Initial selection occurred on interface B).

Input X'02': Data/Status Control

Byte 0	Name	Byte 1	Name
0	Outbound data transfer sequence	0	Channel bus out check
1	Inbound data transfer sequence	1	Selective reset
2	Status transfer sequence	2	Always = 0
3	ESC operation (0 = NSC, 1 = ESC) (Must be 0 with **BCCA**) [2]	3	Stacked ending status
		4	Priority outbound service [4]
4	Data streaming time out	5-7	Residual byte count (PIO mode only)
5	Channel stop/Interface disconnect (see page 7-56)		
6			
7	Suppress out monitor interrupt Program requested interrupt		

Output X'02': Data/Status Control

Byte 0	Name	Byte 1	Name
0	Set/reset outbound data transfer sequence	0	Set monitor for circle B [6]
1	Set/reset inbound data transfer sequence	1	Reset ESC address active [6]
2	Set/reset status transfer sequence	2	Set monitor for 2848 ETX [6]
3	Set/reset ESC operation (0 = NSC, 1 = ESC) (**BCCA:** 0 = No buffer chaining, 1 = Buffer chaining) [5]	3	Set suppressible status
		4	Priority outbound service [6]
4	Set/reset PIO mode (0 = AIO, 1 = PIO)	5-7	Request byte count (PIO mode)
5	Reset initial selection interrupt level 3		
6	Reset data status interrupt level 3		
7	I/O error alert (see page 7-57)		

4 This bit must be 0 with **BCCA.**

5 This bit must be set only with bit 0.0 or 0.1 on, and bit 0.4 off.

6 This bit must be 0 with **BCCA.**

In/Out X'03': ESC Address and Status Bytes (CADS) or VTAM Buffer Length (BCCA)

With **BCCA**, this instruction loads the VTAM buffer length register.

- **CADS**

Byte 0	Name	Byte 1	Name
0-7	ESC Address byte bits 0-7	0 1 2 3 4 5 6 7	ESC: Attention ESC: Status modifier ESC: Control unit end ESC: Busy ESC: Channel end ESC: Device end ESC: Unit check ESC: Unit exception

- **BCCA**

Byte 0	Name	Byte 1	Name
0-7	VTAM buffer length byte 0	0-7	VTAM buffer length byte 1

Input/Output X'04': PIO Data Buffer (Bytes 1-2)

Byte 0	Name	Byte 1	Name
0-7	Data buffer byte 1	0-7	Data buffer byte 2

Input/Output X'05': PIO Data Buffer (Bytes 3-4)

Byte 0	Name	Byte 1	Name
0-7	Data buffer byte 3	0-7	Data buffer byte 4

Input X'06': NSC Status Byte

Byte 0	Name	Byte 1	Name
0	(Not used)	0	NSC: Attention
1	(Not used)	1	NSC: Status modifier
2	(Not used)	2	NSC: Control unit end
3	(Not used)	3	NSC: Busy
4	(Not used)	4	NSC: Channel end
5	(Not used)	5	NSC: Device end
6	(Not used)	6	NSC: Unit check
7	(Not used)	7	NSC: Unit exception

Output X'06': NSC Control and Status Byte

Byte 0	Name	Byte 1	Name
0	(Not used)	0	Set NSC: Attention
1	(Not used)	1	Set NSC: Status modifier
2	(Not used)	2	Set NSC: Control unit end
3	(Not used)	3	Set NSC: Busy
4	(Not used)	4	Set NSC: Channel end
5	(Not used)	5	Set NSC: Device end
6	(Not used)	6	Set NSC: Unit check
7	(Not used)	7	Set NSC: Unit exception

Input X'07': CA Controls

All CAs respond to this broadcast instruction. (For CA numbering, see Table 7-1 on page 7-6.)

Byte 0	Name	Byte 1	Name
0	CA 9/13 interface A enabled	0	CA 1/5 interface A enabled
1	CA 11/15 interface A enabled	1	CA 1/5 interface B enabled
2	CA 10/14 interface enabled	2	CA 2/6 interface A enabled
3	CA 9/13 interface B enabled	3	CA 2/6 interface B enabled
4	CA 11/15 interface B enabled	4	CA 3/7 interface A enabled
5	NSC address active	5	CA 3/7 interface B enabled
6	0 = CS mode, 1 = PIO mode	6	CA 4/8 interface A enabled
7	CA 12/16 interface enabled	7	CA 4/8 interface B enabled

Output X'07' from CP: CA Controls

This instruction is recognized by all CAs, and has two purposes:

1. Selection of a CA either for the duration of the instruction (temporary selection), or until the selection is changed (by autoselection process or another output X'07'). For CA numbering, see Table 7-1 on page 7-6.
2. Setting/resetting various control latches in the CA, according to bits received on the IOC bus.

Byte 0	Name	Byte 1	Name
0	Enable autoselection	0	Set suppress out monitor
1	Disable autoselection	1	Set program requested interrupt
2	Select CA addressed by bits 4-6	2	Reset CA interrupt L1 checks
3	Execute output on CA addressed by bits 4-6	3	Reset system reset/NSC address active
4-6	CA Address:	4	Set allow channel interface enable (A and B)
	000: CA 1/5 100: CA 9/13	5	Set ESC address active [7]
	001: CA 2/6 101: CA 10/14	6	Set ESC command free [8]
	010: CA 3/7 110: CA 11/15	7	Set allow channel interface disable (A and B)
	011: CA 4/8 111: CA 12/16		
7	CA programmed reset		

Notes:

1. If one of the installed CAs is already selected, bits 0.2 and 0.3 can be OFF.
2. If no CA is selected, bits 0.2 and 0.3 are ON with the address of the CA to be selected in bits 0.4-6.
3. If bit 0.3 is used, the selection is only temporary.

Output X'07' from MOSS: CA Controls

This MOSS output is the only allowed when the CP is the owner of the CA.

Byte 0	Name	Byte 1	Name
0	Set concurrent diagnostic mode	0	Reset CCU level 1 and level 3
1	Reset concurrent mode	1	(Not used, must be 0)
2	Select CA addressed by bits 4-6	2	Reset CA Level 1 interrupt to MOSS
3	(Not used, must be 0)	3	Reset CA Level 4 interrupt to MOSS
4-6	CA Address:	4	Disable Interrupt Request to MOSS
	000: CA 1/5 100: CA 9/13	5	Enable Interrupt Request to MOSS
	001: CA 2/6 101: CA 10/14	6	(Not used, must be 0)
	010: CA 3/7 110: CA 11/15	7	(Not used, must be 0)
	011: CA 4/8 111: CA 12/16		
7	(Not used, must be 0)		

[7] With **BCCA**, if this bit is 1, a level 1 interrupt will be raised (with in x'0D' bit 0.5 on) on the next Output x'03' command to prevent the Emulation Program accessing the **BCCA**.

[8] This bit must be 0 with **BCCA.**

Input X'08': Autoselection Chain Check

This is a broadcast command. It should be executed by the control program to determine the CAs which are in the autoselect chain, and the CAs which detected an error during the previous input X'0F'. (“Autoselection” on page 7-44 is a description of the AS mechanism.)

Byte 0	Name	Byte 1	Name
0	CA 1/5 in AS chain	0	AS error detected by CA 1/5 [9]
1	CA 2/6 in AS chain	1	AS error detected by CA 2/6 [9]
2	CA 3/7 in AS chain	2	AS error detected by CA 3/7 [9]
3	CA 4/8 in AS chain	3	AS error detected by CA 4/8 [9]
4	CA 9/13 in AS chain	4	AS error detected by CA 9/13 [9]
5	CA 10/14 in AS chain	5	AS error detected by CA 10/14 [9]
6	CA 11/15 in AS chain	6	AS error detected by CA 11/15 [9]
7	CA 12/16 in AS chain	7	AS error detected by CA 12/16 [9]

Note: For CA numbering, refer to Table 7-1 on page 7-6.

Input X'09': Autoselection Chain Status

(Refer to “Autoselection” on page 7-44 for a description of the AS mechanism.)

Byte 0	Name	Byte 1	Name
0	CA in autoselect chain	0	(Not used)
1	Previous CA in autoselect chain	1	(Not used)
2	Next CA in autoselect chain	2	(Not used)
3	Last CA in autoselect chain	3	(Not used)
4	CP interrupt L1/L3 disabled	4	(Not used)
5	(Not used)	5	(Not used)
6	(Not used)	6	(Not used)
7	(Not used)	7	(Not used)

Output X'09': Bypass CA from Autoselection Chain

(Refer to “Autoselection” on page 7-44 for a description of the AS mechanism.)

Byte 0	Name	Byte 1	Name
0	Set CA in AS chain	0	Reset CA in AS chain
1	Set previous CA in AS chain	1	Reset previous CA in AS chain
2	Set next CA in AS chain	2	Reset next CA in AS chain
3	Set last CA in AS chain	3	Reset last CA in AS chain
4	Set interrupt L1/L3 disabled	4	Reset CP interrupt L1/L3 disabled
5	(Not used, must be 0)	5	(Not used, must be 0)
6	(Not used, must be 0)	6	(Not used, must be 0)
7	(Not used, must be 0)	7	(Not used, must be 0)

[9] This bit is set to 1 during the input X'0F' process if the 'halt' signal is active, and the 'sample in' signal inactive. This bit is meaningless when the CA is not in the AS chain. This bit is reset by output X'07' bit 1.2 (reset CA interrupt L1 check).

Input X'0A': Cycle Steal Chain Status

(Refer to “Cycle Steal” on page 7-46 for a description of the CS mechanism.)

Byte 0	Name	Byte 1	Name
0	CA in the CS chain	0	(Not used)
1	Previous CA in the CS chain	1	(Not used)
2	Next CA in the CS chain	2	(Not used)
3	First CA in the CS chain	3	(Not used)
4	CS request disabled	4	(Not used)
5	(Not used)	5	(Not used)
6	(Not used)	6	(Not used)
7	(Not used)	7	(Not used)

Output X'0A': Bypass CA from Cycle Steal Chain

(Refer to “Cycle Steal” on page 7-46 for a description of the CS mechanism.)

Byte 0	Name	Byte 1	Name
0	Set CA in CS chain	0	Reset CA in CS chain
1	Set previous CA in CS chain	1	Reset previous CA in CS chain
2	Set next CA in CS chain	2	Reset next CA in CS chain
3	Set first CA in CS chain	3	Reset first CA in CS chain
4	Set CS request disabled	4	Reset CS request disabled
5-7	(Not used, must be 0)	5-7	(Not used, must be 0)

Input/Output X'0B': ESC Test I/O Address and Status

Output X'0B' must only be executed in response to an ESC TIO initial selection interrupt. These instructions are invalid for **BCCA.**

Byte 0	Name	Byte 1	Name
0	ESC TIO: Address bit 0	0	ESC TIO: Attention
1	ESC TIO: Address bit 1	1	ESC TIO: Status modifier
2	ESC TIO: Address bit 2	2	ESC TIO: Control unit end
3	ESC TIO: Address bit 3	3	ESC TIO: Busy
4	ESC TIO: Address bit 4	4	ESC TIO: Channel end
5	ESC TIO: Address bit 5	5	ESC TIO: Device end
6	ESC TIO: Address bit 6	6	ESC TIO: Unit check
7	ESC TIO: Address bit 7	7	ESC TIO: Unit exception

Input X'0C': Cycle Steal Mode Control

- **CADS:** Byte 1 of this register indicates the results of the last data transfer sequence in AIO mode.

Byte 0	Name	Byte 1	Name
0 1 2 3 4-7	SYN monitor control latch DLE remember control latch USASCII monitor control latch EBCDIC monitor control latch (Not used)	0-7	Residual byte count (AIO mode)

- **BCCA**: In buffer chaining mode, byte 1 is meaningful only in inbound operation, and contains the number of bytes in the last NCP buffer not successfully transferred from the host:

Byte 0	Name	Byte 1	Name
0-7	**BCCA**: Not used, must be 0	0-7	**BCCA**: Residual byte count

Output X'0C': Cycle Steal Mode Control

This instruction controls the transfer of data between the host CPU and the CCU in AIO mode when the buffer chaining mode is not set. (Out x'0C' is not performed in buffer chaining mode because **BCCA** finds the number of bytes to be transferred.)

- **CADS** (only)

Byte 0	Name	Byte 1	Name
0 1 2 3 4-7	SYN monitor control latch DLE remember control latch USASCII monitor control latch EBCDIC monitor control latch (Not used)	0-7	Request byte count (AIO mode)

Input X'0D': CA Check Register

Byte 0	Name	Byte 1	Name
0	IOC bus parity error (outbound from CCU)	0	Output exception check
1	Microcode detected error [10]	1	PIO halt remember latch
2	CA hardware logic check [10]	2	Cycle steal halt remember latch
3	(Not used, must be 0)	3	Channel bus-in check interface A [10]
4	(Not used, must be 0)	4	(Not used, must be 0)
5	ESC address compare error [10] or EP access (**BCCA**) [10]	5	Channel bus-in check interface B [10]
6	Operation in progress	6	(Not used, must be 0)
7	(Not used, must be 0)	7	(Not used, must be 0)

[10] When this bit is ON, a level 1 interrupt request has been raised. (Refer to “CA Error Condition” on page 7-54.)

Input X'0E': CA Level 1 Interrupt Requests

Input X'0E' is a broadcast command to which all CAs respond. Thus this input will present all CA L1 requests to the IOC bus, with the selected CA indicated. For CA numbering, see Table 7-1 on page 7-6.

Byte 0	Name	Byte 1	Name
0	CA 9/13 L1 interrupt request	0	CA 1/5 L1 interrupt request
1	CA 11/15 L1 interrupt request	1	(Not used, must be 0)
2	CA 10/14 L1 interrupt request	2	CA 2/6 L1 interrupt request
3	Any CA L1 interrupt request	3	(Not used, must be 0)
4-6	Selected CA Address:	4	CA 3/7 L1 interrupt request
	000: CA 1/5 100: CA 9/13	5	(Not used, must be 0)
	001: CA 2/6 101: CA 10/14	6	CA 4/8 L1 interrupt request
	010: CA 3/7 110: CA 11/15	7	(Not used, must be 0)
	011: CA 4/8 111: CA 12/16		
7	CA 12/16 L1 interrupt request		

Input X'0F': CA Level 3 Interrupt Requests.

Input X'0F' is a broadcast command. (For CA numbering, see Table 7-1 on page 7-6.)

Byte 0	Name	Byte 1	Name
0	CA type, must be 1 for 3745.	0	CA 1/5 level 3 pending [12]
1	TPS installed	1	CA 2/6 level 3 pending [12]
2	Selected CA initial selection L3 interrupt request	2	CA 3/7 level 3 pending [12]
3	Selected CA data/status L3 interrupt request	3	CA 4/8 level 3 pending [12]
4-6	CA Address:	4	CA 9/13 level 3 pending [12]
	000: CA 1/5 100: CA 9/13	5	CA 10/14 level 3 pending [12]
	001: CA 2/6 101: CA 10/14	6	CA 11/15 level 3 pending [12]
	010: CA 3/7 110: CA 11/15	7	CA 12/16 level 3 pending [12]
	011: CA 4/8 111: CA 12/16		
7	Buffer chaining mode (**BCCA**) [11]		

[11] This bit is set to 1 when the transfer has been done in buffer chaining mode (requested by an out x'02' with bit 0.3 on).

[12] This bit is set to 1 if the CA has a level 3 pending and if the CA is no longer in the autoselect chain (see “Autoselection Mechanism” on page 7-44). For input X'0F'from MOSS, the autoselection mechanism is not started; the actual MOSS-selected CA responds to the MOSS input X'0F'.

Input X'10': IOC Bus State

Byte 0	Name	Byte 1	Name
0	Connected (set by checkout)	0	CCU interrupt disabled
1	Concurrent mode (set by μP)	1	CS request disabled
2	MOSS interface enabled	2	CA selected from CP (set by hardware)
3	Operation in progress	3	CA selected from MOSS (set by hardware)
4	Cycle steal read (hardware)	4	MOSS interrupt disabled
5	Diagnostic mode	5-7	(Not used, must be 0)
6	**BCCA**: Buffer chaining mode (hardware)		
7	(Not used, must be 0)		

Input/Output X'11': Interrupts to CP/MOSS

Byte 0	Name	Byte 1	Name
0	CCU Level 3 [13]	0	MOSS level 1 [15]
1	Normal initial selection level 3 [14]	1	MOSS interrupt level 4 [15]
2	Initial selection system reset L3 [14]	2	IPL detect bit
3	Normal data/status level 3 [14]	3-7	(Not used, must be 0)
4	Priority outbound data/status level 3 [14]		
5	Other data/status level 3 [14]		
6	Set CCU level 1 [14]		
7	CCU Level 1 [13]		

Input/Output X'12': IOC Bus Sense Register

Byte 0	Name	Byte 1	Name
0	Halt sense	0	CS burst count check
1	IOC parity out check	1	RAM address count check
2	Out exception check	2	Data bus parity check
3	Invalid command	3	Receiver check
4	IOC check	4	CS buffer count check **(BCCA)**
5	Set autoselect sense	5-7	(Not used, must be 0)
6	Autoselect error detected		
7	Reset autoselect sense		

[13] Bits 0 and 7 of byte 0 are set by hardware.

[14] Bits 1 through 6 of byte 0 are reset by hardware.

[15] Bits 0 and 1 of byte 1 are reset by hardware.

Input/Output X'13': CP/MOSS Address - Bus Module EC - CAL Card EC

Byte 0	Name	Byte 1	Name
0	CP address available	0	Adapter bus module EC number bit 0 (1•••)
1	CA hard-wired address bit 0 (1••)	1	Adapter bus module EC number bit 1 (•1••)
2	CA hard-wired address bit 1 (•1•)	2	Adapter bus module EC number bit 2 (••1•)
3	CA hard-wired address bit 2 (••1)	3	Adapter bus module EC number bit 3 (•••1)
4	CP logic address bit 0 (1••)	4	CAL Card EC number bit 0 (1••)
5	CP logic address bit 1 (•1•)	5	CAL Card EC number bit 1 (•1•)
6	CP logic address bit 2 (••1)	6	CAL Card EC number bit 2 (••1)
7	(Not used, 0)	7	Channel B module installed

Input/Output X'14': AS/CS Chain Information

Byte 0	Name	Byte 1	Name
0	CA in AS chain	0	IOC selected
1	Previous CA in AS chain	1-7	0 (Not used)
2	Next CA in AS chain		
3	Last CA in AS chain		
4	CA in CS chain		
5	Previous CA in CS chain		
6	Next CA in CS chain		
7	First CA in CS chain		

Input/Output X'15': CS/DMA Index - Diagnostics

Byte 0	Name	Byte 1	Name
0	CS index bit 0	0	Force error on register/counter
1	CS index bit 1	1	Inhibit out exception check
2	CS index bit 2	2	Inhibit IOC μP interrupt
3	Data index bit 0 (1•••)	3	Disable sample rec
4	Data index bit 1 (•1••)	4	0 (Not used)
5	Data index bit 2 (••1•)	5	Set sample
6	Data index bit 3 (•••1)	6	0 (Not used)
7	0 (Not used)	7	0 (Not used)

Input/Output X'16': IOH/MIOH Validation Byte - Autoselect State

Byte 0	Name	Byte 1	Name
0	CP invalid write command	0	Previous CA selected
1	MOSS invalid write command	1	Autoselect complete
2	Write interrupt	2	Autoselect enable
3	Out exception flag	3	Loop indicator
4	CP invalid read command	4	0 (Not used)
5	MOSS invalid read command	5	0 (Not used)
6	Read interrupt	6	0 (Not used)
7	Use CS index	7	0 (Not used)

Input/Output X'17': CS Burst Counter - RAM Address Counter

Byte 0	Name	Byte 1	Name
0-7	CS burst counter (residual byte count)	0-7	RAM address pointer

Input/Output X'18': Bus Module Interrupt to μP - μP Commands

Byte 0	Name	Byte 1	Name
0	PIO interrupt	0	Reset PIO interrupt
1	AIO interrupt	1	Reset AIO interrupt
2	IOC error interrupt	2	Reset IOC error interrupt
3	Tag reset interrupt	3	Reset tag reset interrupt
4	Interrupt requested	4	**CADS**: Reset interrupt requested
5	0 (Not used)		**BCCA**: Set buffer chaining mode
6	0 (Not used)	5	Set CS request read (from CA to CCU)
7	0 (Not used)	6	Set CS request write (from CCU to CA)
		7	**CADS**: Set interrupt requested
			BCCA: Set direct/indirect mode

Input/Output X'19': TA Register

See “R2 Contents at TA Time” on page 7-14.

Byte 0	Name	Byte 1	Name
0	0: IOC1, 1: IOC2	0	Command 1•••
1	Not used, must be 0	1	Command •1••
2	Not used, must be 0	2	Command ••1•
3	Not used, must be 0	3	Command •••1
4	1: Command is for a CA	4	0: CCU, 1: MOSS
5	Command 1••	5	Not used, must be 0
6	Command •1•	6	0: Normal, 1: Storage
7	Command ••1	7	0: Write, 1: Read

Input/Output X'1A': TD Register

See “Bus Contents at TD Time (R1 Register)” on page 7-15.

Byte 0	Name	Byte 1	Name
0-7	Data from UC bus byte 0	0-7	Data from UC bus byte 1

Input/Output X'1B': UC Bus Tag Out

Byte 0	Name	Byte 1	Name
0	I/O	0	Halt
1	TA	1	Reset
2	TD	2-7	0 (Not used)
3	CSG		
4	CSG thru in		
5	CSG bypass in		
6	Out		
7	VFA in (valid feed auto)		

Input/Output X'1C': UC Bus Tag In - MOSS Interface

Byte 0	Name	Byte 1	Name
0	VH (valid halfword)	0	Nohold
1	0 (Not used)	1	CA MOSS Reset
2	EOC (end of chain)	2	CA MOSS POR
3	VB/M	3	Sample in
4	CRS	4	Sample in bypass
5	VFA out	5-7	0 (Not used)
6	PV (parity valid)		
7	CSG out latch		

Input/Output X'1D': Miscellaneous 1

Byte 0	Name	Byte 1	Name
0	TA register loaded	0	DMA 2 bytes lat 1
1	TD register loaded	1	DMA 2 bytes lat 2
2	TD register B0 loaded	2	Validation reg loaded
3	TD register B1 loaded	3	PIO Interrupt remember
4	TD register decoded	4	AIO Interrupt remember
5	CS in progress	5	CA temporary selected
6	DMA validation	6	Change priority
7	PIO in progress	7	Inhibit sample

Input/Output X'1E': Miscellaneous 2 or CS Buffer Counter (BCCA)

Byte 0	Name	Byte 1	Name
0	Autoselect in progress	0-7	**BCCA:** CS buffer counter
1	High priority		
2	Low priority		
3	Simulated POR remember		
4	TA parity check		
5	Validation reg parity check		
6	**BCCA:** Inhibit interval timer		
7	0 (not used)		

Input/Output X'1F': CS Interval Timer

These instructions are used with **BCCA** only.

Byte 0	Name	Byte 1	Name
0-3	0 (not used)	0-2	0 (not used)
4-7	CS interval timer	3	First AIO state Q0
		4	First AIO state Q1
		5	CS pointer state Q0
		6	CS pointer state Q1
		7	CS pointer state Q2

Input/Output X'20/30': Channel A/B Control Module Interrupts

Byte 0	Name	Byte 1	Name
0	Data transfer interrupt	0-7	0 (not used)
1	Status transfer interrupt		
2	Initial selection interrupt		
3	Host reset interrupt		
4	Panel interrupt		
5	Interface setting interrupt		
6	Channel module logic error interrupt		
7	Timer interrupt		

Input/Output X'21/31': Data Registers

Byte 0	Name	Byte 1	Name
0-7	• Address when address out (host initiated operation) • Address when address in (CCU initiated operation) • If data streaming: Data when data out Data when data in	0-7	• Command when command out (host initiated operation) • Status when status in (host or CCU initiated) • Data when service out • Data when service in

Input/Output X'22/32': NSC Address - Host Interface Features

Byte 0	Name	Byte 1	Name
0-7	NSC Address	0	Channel priority
		1	High speed feature
		2	I/O error alert feature
		3	Interface disable on I/O error alert [16]
		4	Data streaming feature
		5-7	Data Streaming Frequency: 010: 3-MB or 4.5-MB channel 011: 2-MB channel 111: 1-MB channel

Input/Output X'23/33': ESC Address Range

These instructions are not used for **BCCA.**

Byte 0	Name	Byte 1	Name
0-7	ESC range high address	0-7	ESC range low address

[16] When this bit is set to 1, the CA disables its host interface after an I/O error alert initiated by the CP.

Input/Output X'24/34': CADR Card EC - Channel Control Module EC

Byte 0	Name	Byte 1	Name
0	CADR raw card EC bit 0	0	Force error register and counter
1	CADR raw card EC bit 1	1	Force bus in bad parity
2	CADR raw card EC bit 2	2	Inhibit bus out check
3	CADR installed	3	Wrap external
4	Channel module EC bit 0	4	Wrap on CADR card
5	Channel module EC bit 1	5	Force micro bus bad parity
6	Channel module EC bit 2	6	Inhibit channel module error interrupt
7	Channel module EC bit 3	7	Diagnostic mode

Input/Output X'25/35': Logic Error in Channel Control Module

Byte 0	Name	Byte 1	Name
0	SIDI counter check	0	Micro bus parity check
1	SODO counter check	1	DMA acknowledgment too late check
2	RAM address check	2	Internal data parity error
3	Residual byte counter check	3	0 (not used)
4	Timer counters check	4	Bus in external parity error
5	Bus in channel module parity error	5	0 (not used)
6	Character decode check **(CADS)**	6	Bus out channel module parity error
7	Not used	7	0 (not used)

Input/Output X'26/36': SIDI and SODO Counters

Byte 0	Name	Byte 1	Name
0-7	SIDI counter (number of bytes to transfer)	0-7	SODO counter (number of bytes transferred)

Input/Output X'27/37': Residual Byte Counter - RAM Address Pointer

Byte 0	Name	Byte 1	Name
0-7	Residual byte counter	0-7	RAM address pointer (last address low part: 1111 1111)

Input/Output X'28/38': RAM Index

Byte 0	Name	Byte 1	Name
0-3	0 (not used)	0-7	0 (not used)
4	RAM address bit 0 (1••• •••• ••••)		
5	RAM address bit 1 (•1•• •••• ••••)		
6	RAM address bit 2 (••1• •••• ••••)		
7	RAM address bit 3 (•••1 •••• ••••)		

Input/Output X'29/39': Timer Counters

Byte 0	Name	Byte 1	Name
0-7	Timer counter 1 (high speed)	0-7	Timer counter 2 (low speed)

Input/Output X'2A/3A': μP Commands - MOSS Commands

Byte 0	Name	Byte 1	Name
0	0: Allow interface disable	0	No hold
	1: Allow interface enable	1	CA n MOSS reset
1	Must be 1	2	CA n MOSS power ON reset
2	Set ESC address active [17]	3	MOSS interface enable
3	Reset ESC address active [18]	4	Channel module selected
4	Set start timer	5	Set channel control module
5	Set stop timer		(0: module A, 1: module B)
6	CA programmed reset	6	0 (not used)
7	Reset interrupt request	7	0 (not used)

Input/Output X'2B/3B': μP Commands - Character Monitoring

Byte 0	Name	Byte 1	Name
0	Outbound data transfer	0	Circle B monitor (out X'02') [17]
1	Inbound data transfer	1	2848 ETX monitor (out X'02') [17]
2	Status transfer	2	SYN monitor (AIO: out X'0C') [17]
3	I/O error alert	3	DLE remember (AIO: out X'0C') [17]
4	Suppress out monitor	4	USASCII monitor (AIO: out X'0C') [17]
5	0: Force request to switch	5	EBCDIC monitor (AIO: out X'0C') [17]
	1: No request to switch	6	Suppressible status
6	Short busy status transfer	7	Start on service in
7	Inhibit transfer in DS mode		

Input/Output X'2C/3C': Data/Status Transfer States

Byte 0	Name	Byte 1	Name
0	Bus out check	0	0 (not used)
1	Data selective reset	1	Status selective reset
2	Character recognized[17]	2	Command chaining indicated
3	Count stop	3	Status stacked
4	DS time out	4	Status accepted
5	Channel stop	5	Select out active
6	DLE remember [17]	6	Sup out monitor interrupt
7	Data halt I/O	7	Status halt I/O

[17] This bit must be 0 with **BCCA.**

[18] This bit must be 1 with **BCCA.**

Input/Output X'2D/3D': Initial Selection State - Miscellaneous States

Byte 0	Name	Byte 1	Name
0	Bus out check	0	System reset active
1	Initial selection selective reset	1	System reset inactive
2	0 (not used)	2	Panel switch active
3	Request to be switched	3	Panel switch inactive
4	NSC address valid	4	Interface enabled
5	ESC address valid [19]	5	Interface disabled
6	0 (not used)	6	Selective reset
7	Initial selection halt I/O	7	Halt I/O

Input/Output X'2E/3E': Tags Out - Tags In

Byte 0	Name	Byte 1	Name
0	Suppress out	0	Request in
1	Operational out	1	Operational in
2	Address out	2	Address in
3	Command out	3	Status in
4	Service out	4	Service in
5	Data out	5	Data in
6	Hold out	6	Disconnect in
7	Select out (incoming)	7	Select in (outgoing)

Input/Output X'2F/3F': Miscellaneous

Byte 0	Name	Byte 1	Name
0	Bypass sel out relay driver	0	SYN counter (1) [19]
1	Sel out load driver	1	SYN counter (2) [19]
2	Enable NPL driver	2	Address in remember
3	Select line trapped	3	CS request 1 (DI/DO)
4	Data transfer run	4	CS request 2 (SI/SO)
5	0 (not used)	5	0 (reserved)
6	Bus in gate data in (DI)	6	Operational out
7	Bus in gate select in (SI)	7	Interrupt request

[19] This bit must be 0 with **BCCA.**

Input/Output X'40': CP Address

This command is used to initialize the CA with its CP address. (For CA numbering, see Table 7-1 on page 7-6.)

Byte 0	Name	Byte 1	Name
0	CP address available	0	No stop trace
1	(Reserved, must be 0)	1	(Reserved, must be 0)
2	(Reserved, must be 0)	2	(Reserved, must be 0)
3	(Reserved, must be 0)	3	(Reserved, must be 0)
4-6	Selected CA Address:	4	(Reserved, must be 0)
	000: CA 1/5 100: CA 9/13	5	(Reserved, must be 0)
	001: CA 2/6 101: CA 10/14	6	(Reserved, must be 0)
	010: CA 3/7 110: CA 11/15	7	(Reserved, must be 0)
	011: CA 4/8 111: CA 12/16		
7	(Reserved, must be 0)		

Input/Output X'41' or X'42': Interface A or B Host Parameters

Command X'41' is used to initialize host interface A with the NSC address and host features.

Command X'42' is used to initialize host interface B with the NSC address and host features.

Byte 0	Name	Byte 1	Name
0	NSC Address bit 0	0	Channel priority (0=low, 1=high)
1	NSC Address bit 1	1	High speed data transfer feature
2	NSC Address bit 2	2	I/O error alert feature present
3	NSC Address bit 3	3	Interface disable on I/O error alert [20]
4	NSC Address bit 4	4	Data streaming transfer feature present
5	NSC Address bit 5	5-7	)-- Data Streaming Frequency:
6	NSC Address bit 6		) 010: 3-MB or 4.5-MB channel
7	NSC Address bit 7		) 011: 2-MB channel
			) 111: 1-MB channel

Input/Output X'43' or X'44': Interface A or B Burst Length

Command X'43' is for channel interface A.

Command X'44' is for channel interface B.

Byte 0	Name	Byte 1	Name
0		0	(Reserved, must be 0)
1	This byte gives the number of	1	(Reserved, must be 0)
2	data bytes which can be	2	(Reserved, must be 0)
3	exchanged over the channel	3	(Reserved, must be 0)
4	interface, for each connection,	4	(Reserved, must be 0)
5	when the channel is a byte	5	(Reserved, must be 0)
6	multiplexer.	6	(Reserved, must be 0)
7		7	(Reserved, must be 0)

[20] When this bit is set to 1, the CA disables its host interface after an I/O error alert initiated by the CP.

Input/Output X'45' or X'46': A or B Interface ESC Range

Command X'45' is for channel A.
Command X'46' is for channel B.
These instructions are invalid for **BCCA.**

Byte 0	Name	Byte 1	Name
0-7	ESC range lower address	0-7	ESC range higher address

Input/Output X'47': Cycle Steal Burst Length

Byte 0	Name	Byte 1	Name
0-7	(This byte gives the maximum number of halfwords that can be exchanged in CS over the IOC bus.)	0 1 2 3 4-7	CA type (0 = **CADS**, 1 = **BCCA**) CA type (must be 1 for 3745) TPS installed (Not used) CS interval timer [21] **(BCCA)**

Input/Output X'48': Channel Driver/Receiver Enabling/Disabling

This command allows the connection of the CA to the channel without disturbing the interface (as with a switch, for instance).

Byte 0	Name	Byte 1	Name
0 1 2-7	Enable drivers/receivers on interface A Disable drivers/receivers on interface A (Reserved, must be 0)	0 1 2-7	Enable drivers/receivers on interface B Disable drivers/receivers on interface B (Reserved, must be 0)

Input X'49': Basic CAL Card EC Sense

Byte 0	Name	Byte 1	Name
0-2 3 4-7	CAL raw card EC number Channel B control module installed Adapter bus control module EC number	0-2 3 4-7	Interface A CADR raw card EC number Interface A CADR card installed Channel A control module EC number

Input X'4A': Microcode Level and TPS EC number

Byte 0	Name	Byte 1	Name
0-7	Microcode EC number	0-2 3 4-7	Interface B CADR raw card EC number Interface B CADR card installed Channel B control module EC number

[21] With **BCCA**, these bits give the time between two AIO transfers when the buffer chaining mode is set (x 1.2 μs).

Input X'4B': Checkout Result

This instruction gives the result of the checkout procedure.
A result of X'9F00' means checkout complete without error if **CADS**, a result of X'BF00' means checkout complete without error if **BCCA**.

Byte 0	Name	Byte 1	Name
0	Checkout complete [22]	0-5	CAL/CADR card in error [25]
1	Checkout error [23]	6-7	(Not used, must be 00)
2	Buffer chaining **CA** type (0 = **CADS**, 1 = **BCCA**)		
3-7	Checkout routine identifier [24]		

Input/Output X'4C': Diagnostics

These instructions are invalid for **BCCA.**

Byte 0	Name	Byte 1	Name
0	Force error on IOC bus control module counter	0	External wrap on interface A [28]
1	Force error on channel A control module registers	1	External wrap on interface B [29]
2	Force error on channel B control module registers	2-7	(Not used)
3	Wrap channel A on CADR [26]		
4	Wrap channel B on CADR [27]		
5-7	(Reserved, must be 000)		

Input X'4D': Sense ID 1 (Vital Product Data)

This instruction gives the first two bytes of the machine type and model number.

Input X'4E': Sense ID 2 (Vital Product Data)

This instruction gives the last two bytes of the machine type and model number.

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[22] When set, this bit means that the CA is in operational mode.

[23] This bit is reset at checkout start.

[24] These five bits give the binary value of the last test routine executed. This field allows up to 32 values. When an error is detected, this field indicates the routine which caused the error. When the checkout runs error free, this routine number takes the maximum value X'1F'.

[25] Anyone of these five bits set to one indicates an error. These bits are reset at the checkout start.

[26] Interface A tags and buses are wrapped on the CADR card A.

[27] Interface B tags and buses are wrapped on the CADR card B.

[28] Interface A tags and buses are wrapped at the channel tailgate.

[29] Interface B tags and buses are wrapped at the channel tailgate.

Input/output X'4F': Channel Monitoring

Byte 0	Name	Byte 1	Name
0	Set channel monitoring	0	Set trace ON
1	Reset channel monitoring	1	Set trace OFF
2	Force CA disable	2-7	(Not used)
3	Set not initialized mode		
4	Set intervention required mode		
5	Set inhibit write IPL		
6	Reset inhibit write IPL		
7	0 (Not used)		

Input X'50': Adapter Bus Control Module Check

This instruction gives added information when there is a CA logic check due to the adapter bus control module (CAL card).

Byte 0	Name	Byte 1	Name
0	CS burst counter check	0	Halt sense
1	Data memory address counter check	1	Parity outbound check
2	Data bus parity check	2	Output exception check
3	Receiver check	3	Invalid command
4	ESC address active	4	Module check
	BCCA: CS buffer count check	5	Set autoselect sense
5	CP hardware address 1••	6	Autoselect error
6	CP hardware address •1•	7	Reset autoselect sense
7	CP hardware address ••1		

Input X'51' or X'52': Channel A or B Control Module Check

This instruction gives added information when there is a CA logic check due to the channel control module (CAL card).

Command X'51' is for channel A.
Command X'52' is for channel B.

Byte 0	Name	Byte 1	Name
0	SIDI counter check	0	Micro bus parity error
1	SODO counter check	1	DMA acknowledgment too late
2	Data memory address check	2	Internal data parity error
3	Residual byte counter check	3	(Reserved, must be 0)
4	Timer counter check	4	Bus-in external parity error
5	Bus-in parity error	5	(Reserved, must be 0)
6	Character decode check **(CADS)**	6	Bus-out parity error
7	Not used	7	(Reserved, must be 0)

Input X'60': Microcode-Detected Error Code

Byte 0 of this register gives a microcode-detected error code.
Byte 1 gives additional information about microcode-detected errors.

Byte 0	Byte 1	Description
02	IN2D-1	ITFE : Panel interrupt - invalid FE1B register
03	IN2D-1	ITFE : Interface setting interrupt - invalid FE1B reg
05	IN12-0	ITMUC: Error sense register MUC04 invalid
0A	IN20-0	ITFE : Invalid FE00(0,1,2) bit combination
0B	OUT02-0	OUT02: OUT X'02'occurs and DS interrupt raised
11	OUT02-0	DATA : Invalid OUT X'02'-0(0,1,2) bit combination
16	OUT02-0	DATA : NSC address inactive for a data transfer
1B	IN18-0	ITMUC: Unknown MUC10 (interrupt from MUC)
21	IN2D-1	CHMFE: Panel interrupt - invalid FE1B register
22	IN2D-1	CHMFE: Interface setting interrupt - invalid FE1B reg
24	IN20-0	CHMFE: More than one bit in FE00(0,1,2)
25	-	IT : spurious interrupt
26	Ckt nb	IDERR: error during checkout idle diag
29	OUT18-1	There is no code handling a PIO command
2D	IN65-0	Unexcpected FE state on IS + status interrupt
2E	IN67-1	Unexpected chaining flag on IS + status interrupt
2F	IN67-1	Unexpected chaining flag on IS + status interrupt
31	-	IO error alert command received when feature not set
32	-	IO error alert command received when no interf enabled
33	-	IO error alert command received in TPS when no alleg
34 (1)	IN03-0	OUT X'03' received with UNITSZ value = 0
35 (1)	OUT01-0	OUT X'01' received with offset-I>= NCP buffer length
36 (1)	IN65-0	Status intp with hio or sel reset in buffer chaining
38 (1)	IN2C-0	FE intp of data transfer in buffer chaining
39 (1)	IN65-0	FE intp os status transfer in buffer chaining
3A (1)	IN67-1	FE intp os status + IS in buffer chaining

Note: (1) BCCA only

In/Out X'61' through X'7F': Microcode Information Registers

The following are microcode information registers:
X'61', X'62', X'63', X'64', X'65', X'66', X'67', X'74', X'75', X'76', X'7F'.

X'61':

Byte 0	Name	Byte 1	Name
0	Channel end remember	0	Other data/status interrupt raised (program request interrupt/suppress out monitor)
1	NSC address active		
2	Allow interface enable receive	1	ESC address active
3	0: not selected, 1: selected	2	Asynchronous NSC status
4	ESC active (not command free)	3	Answer temporary busy to an initial selection
5	ESC test I/O status available	4	Channel end sent
6	NSC status available	5	Contention type (if bit 7 on): 0: channel control module, 1: out X'02'
7	Write IPL pending	6	TPS feature used (0: TCS, 1: TPS)
		7	Initial selection and data/status contention

X'62':

Byte 0	Name	Byte 1	Name
0	Adapter bus control module busy with cycle steal	0	System reset interrupt raised
1	Adapter bus control module ready for next burst	1	Must be 0
2	Set channel monitor received	2	Force level 1 pending
3	Reset channel monitor received	3	Program request interrupt pending
4	0: NI mode, 1: IR mode	4	Suppress out monitor request pending
5	Initial selection interrupt raised	5	Initial selection interrupt request pending
6	Data/status interrupt raised	6	Data/ status interrupt request pending
7	Level 1 interrupt raised	7	Level 1 interrupt request pending

X'63':

Byte 0	Name	Byte 1	Name
0-7	System reset pending (see X'65' or X'75' byte 0)	0 1 2 3 4 5 6 7	Status with unit check end Front end control module ready for next burst Initial selection pending temporary busy Program request interrupt/suppress out monitor pending (or selective reset temporary busy) System reset interrupt raised Not used Channel control module interrupt has been raised Defer PIO interrupt reset

X'64' or X'74':

Command X'64' is for channel A. Command X'74' is for channel B.

Byte 0	Name	Byte 1	Name
0-7	Interface state: 0 = neutral 1 = request to switch pending 2 = instantaneous allegiance 3 = long term allegiance	0 1 2 3 4 5 6 7	DE TPS pending System reset active 0, Not used Force busy received Busy status sent 0: disabled, 1: enabled Disable request pending Panel switch active

X'65' or X'75':

Command X'65' is for channel A. Command X'75' is for channel B.

Byte 0	Name	Byte 1	Name
0-7	Channel control module state (see trace)	0-7	Channel burst length

X'66' or X'76':

Command X'66' is for channel A. Command X'76' is for channel B.
Not used for **BCCA**

Byte 0	Name	Byte 1	Name
0-7	ESC range lower address	0-7	ESC range higher address

X'67':

Byte 0	Name	Byte 1	Name
0	Halt sense	0-7	Chaining flag:
1	Channel control module logic error		0 = no chaining
2	IOC bus adapter logic error		1 = chaining with NOOP command
3	Selective reset		2 = chaining with ESC status
4	Data streaming time out, or bus out check		4 = chaining with NSC status
5	Remember halt I/O		5 = chaining with TEST I/O
6	Remember selective reset		6 = chaining with adapter generated status **(BCCA)**
7	Force ending data transfer		

X'7F': Cycle Steal Control Word

Byte 0	Name	Byte 1	Name
0-4	Not used	0	0 = Write operation (IOC to CA)
5	0 = CA (1 = LA)		1 = Read operation (CA to IOC)
6	0 = Mode determined by bit 1.1	1	0 = Indirect, 1 = Direct
	1 = Direct/Indirect		(Must be 0 if bit 0.6 is 1)
7	0 = Short address	2-3	Not used
	1 = Long address	4	CP logical address 1••
	(Must be 0 if bit 0.6 and	5	CP logical address •1•
	bit 1.1 are 0.)	6	CP logical address ••1
		7	Not used

Autoselection

In order to work with a CA, the control program must first select that CA. Two methods are available: output X'07' giving the CA address, or autoselection.

Autoselection Mechanism

To perform autoselection, a CA must already be selected, and an output X'07' with bit 0.0 = 1 (enable autoselection) must be executed.

Autoselection will be effective on an input X'0F' execution. At that time, the CA having the highest priority pending level 3 interrupt becomes automatically selected, and the currently selected CA will deselect. If no CA has a level 3 interrupt request, the previously selected CA remains selected.

The priority for the level 3 autoselection mechanism is as follows (from highest to lowest):

1. Priority outbound data transfer L3 interrupt (ouput X'02' bit 1.4 = 1).
2. Other level 3 interrupts (see “Level 3 Interrupt Request” on page 7-48).

Autoselection (AS) Chain

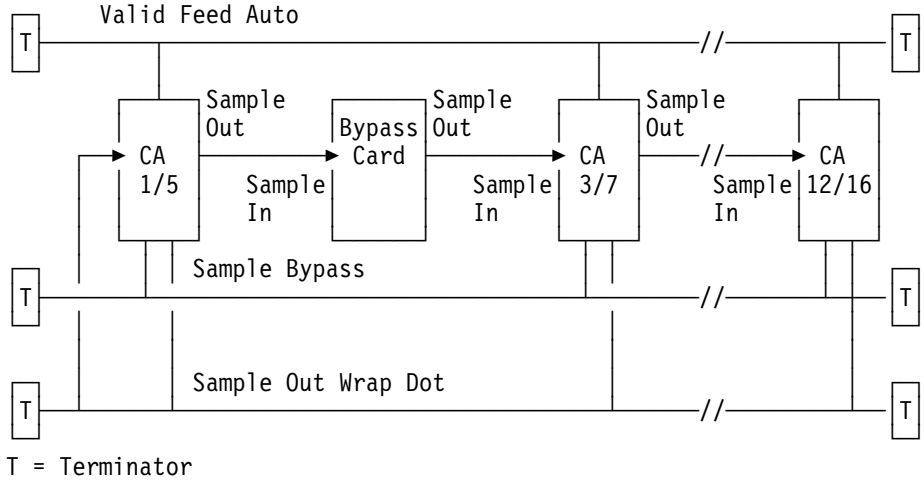

Figure 7-5. Example of Autoselection Chain

The AS chain allows up to eight CAs to be installed without specific jumpering, that would be configuration-dependent. The AS chain carries the following signals:

- Valid Feed Auto: A bi-directional line is used to synchronize the IOC bus 'Valid Tag' line for all PIO broadcast commands.
- Sample Out: Unidirectional line going out from the CA. This line is addressed to the next installed CA in the loop if it has not been removed from the AS chain. The 'Sample Out' line is connected to the 'Sample In' line of the next installed CA.
- Sample In: If the previous CA is installed, this line is connected to 'Sample Out' of the previous CA.
- Sample Bypass: Bidirectional line used to bypass the CA if the previous CA, or the next installed CA, has been removed.
- Sample Out Wrap Dot: Unidirectional line going out from the CA, used by the last CA installed and returned to the first CA (CA 1/5).

'CA Sample Out' connects all CAs. This line enables the circular-poll function of the AS sequence. That is, polling for the highest priority interrupt starts with the CA following the previously selected CA (or the one after that, if it is no longer in the AS chain): CA 1/5 follows CA 12/16, CA 2/6 follows CA 1/5, ... (see Table 7-1 on page 7-6 for CA numbering).

Autoselection Error

When the hardware detects a problem on the 'sample' chain, no CA will answer at 'TD' time, and an IOC bus time out will be set.

The control program must determine the failing CA.

Removing a CA from the Autoselection Chain

One power supply (PS) powers two CAs, so only the two CAs powered by the same PS can be removed from the autoselection chain.

The control program must remove the CA's from the autoselection chain.

Cycle Steal

Cycle Steal Control Word (CSCW)

In CS operation, the first halfword sent by the CA is the CSCW, in order to make the following information known to the IOC:

- Adapter type
- Adapter address
- Read/Write operation
- Cycle steal mode.

Byte 0	Name	Byte 1	Name
0-4	Not used	0	0 = Write operation (IOC to CA)
5	0 = CA (1 = LA)		1 = Read operation (CA to IOC)
6	0 = Mode determined by bit 1.1	1	0 = Indirect, 1 = Direct
	1 = Direct/Indirect		(Must be 0 if bit 0.6 is 1)
7	0 = Short address	2-3	00
	1 = Long address	4-6	CP address (given by output X'40')
	(Must be 0 if bits 0.6 and 1.1 are 0.)		This address will be sent to the CCU registers 30 to 37 for IOC1, and to registers 60 to 67 for IOC2.
		7	0

Cycle Steal (CS) Chain

Depending on whether the CA is the first installed, or a previous CA is in the CS chain, the CA will have to monitor either:

- 'CS grant low priority' (CSG-L), or
- 'CS grant low-thru-out' (CSG-T), or
- 'CS grant low-bypass-out' (CSG-B).

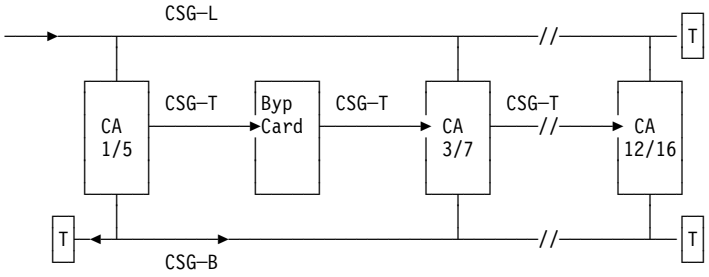

Figure 7-6. Example of Cycle Steal Chain

Removing a CA from the Cycle Steal Chain

To avoid potential host system hangup, no data transfer must be in progress for the CA which has to be removed from the CS chain. The control program must remove the CA from the cycle steal chain.

CA Interface Enabling/Disabling

The channel interface for each CA must be enabled before communications can take place with a host channel to which the CA is attached, and the 'select out' signal must be available from the host. The output X'48' instruction allows the connection of the CA to the channel (see input/output X'48' on page 7-38). the drivers/receivers).

Notes:

1. Enabling the drivers/receivers will not enable an interface unless an IOH/IOHI output X'07' with byte 1, bit 4 ON has been issued by the CP to set the 'allow channel interface enable' latch. Furthermore, an IOH output X'07' with byte 1, bit 5 ON must be executed to enable the ESC addresses.
2. If a CA has a TPS and is attached to a loosely coupled host, or hosts, only one interface may be enabled at a time on the affected CA.

CA/MOSS Connection

A 56-line link connects the MAC card to the channel adapters.

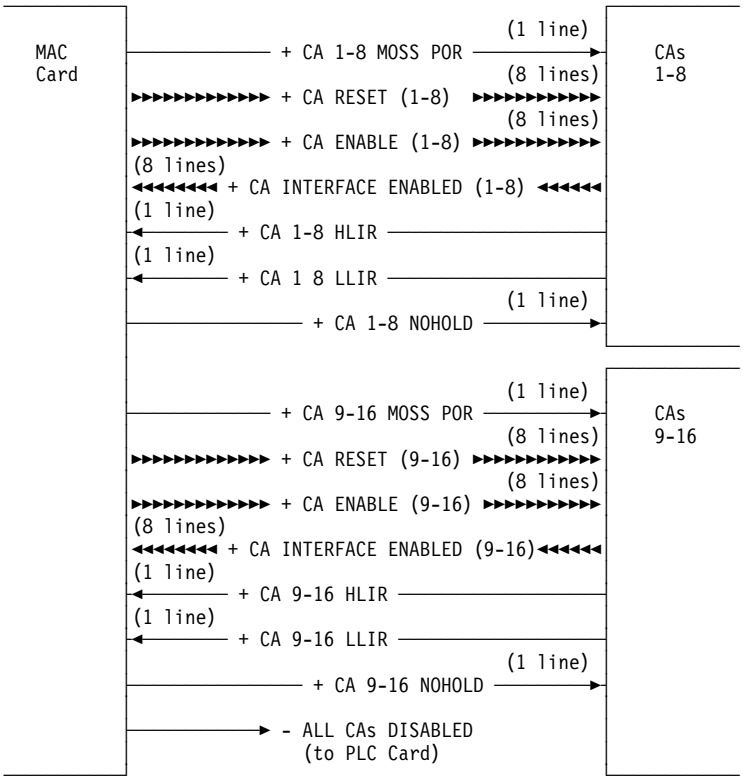

Figure 7-7. CA link to MOSS

Note: The 'CA NOHOLD' line coming from the MOSS (broadcast line) is used to validate the 'CA MOSS POR', 'CA x RESET', and 'CA x ENABLE' lines.

Interrupt Requests

The CA generates two major classes of interrupt: CA level 1 and CA level 3 interrupt requests.

Level 1 Interrupt Request

This request is associated with hardware detection of errors in the CA. When an error condition is detected in the CA, a bit is set in the CA level 1 interrupt check bit register X'0D', as shown under “CA Error Condition” on page 7-54.

These errors raise a level 1 interrupt request to the CCU by activating IOC bus byte 0, bit 5 (if register X'09' bit 0.4, 'interrupt request disabled', is OFF).

Level 3 Interrupt Request

A CA raises a level 3 interrupt request to the CCU by activating IOC bus byte 1, bit 0 when the I/O is not active (if register X'09' bit 0.4, 'interrupt request disabled', is OFF). There are two types of level 3 interrupt request:

1. CA initial selection request:
   - An initial selection sequence occurs if buffer chaining is not set
   - An initial selection sequence occurs for commands other than Read, TIO or NO-OP when buffer chaining outbound is set
   - An initial selection sequence occurs for commands other than Write, Write-Break, TIO ot NO-OP when buffer chaining inbound is set
   - NSC status cleared if buffer chaining is not set
   - A system reset sequence occurs
   - ESC TIO status cleared
   - Selective reset
   - Interface disconnect
   - Channel bus out check
2. Data/status transfer request:
   - End of an inbound data transfer if buffer chaining is not set
   - End of an outbound data transfer if buffer chaining is not set
   - End of a status transfer if buffer chaining is not set
   - End of the last inbound data transfer if buffer chaining is set (for example end of PIU)
   - End of the last outbound data transfer if buffer chaining is set (for example end of PIU chain)
   - Suppress out monitor interrupt.
   - A program requested interrupt occurs.
   - Any CA level 1 check occurs when the adapter is in a data/status transfer sequence.
   - A data streaming time out interrupt occurs
   - A channel bus out check
   - A selective reset or an interface disconnect when the CA is in data/status/IO error alert sequence.

Control Character Recognition

Certain control characters from the host channel are recognized by the CA hardware, which sets corresponding bits in register X'0C'. The control program modifies its monitoring action according to these bits.

Name	EBCDIC	ASCII
Circle B	3D or BD	
2848 ETX	03	
DLE	10	10 or 90
STX	02	02 or 82
ETB	26	17 or 97
ETX	03	03 or 83
SYN	32	16 or 96

Circle B monitoring is started by an output X'02' with byte 1, bit 0 ON and 2848 ETX with byte 1, bit 2 ON. BSC EBCDIC and ASCII DLE, STX, ETB and ETX monitoring are initiated by an output X'0C' with byte 0, bit 2 or 3 ON. Both bits cannot be set at the same time. SYN monitoring requires output X'0C' byte 0, bit 0 to be ON along with byte 0, either bit 2 or 3.

For a circle B, 2848 ETX, EBCDIC or ASCII, ETB or ETX, the CA hardware does not accept any further data from the host after receiving the control character, and sets a CA level 3 interrupt request with channel stop indicated in register X'02'.

When a DLE is immediately followed by an STX, the CA resets all monitoring for EBCDIC or ASCII characters. The DLE STX sequence indicates that BSC transparency mode has been activated. In transparency mode, data may be sent that has the same bit pattern as a control character, which is why monitoring must be stopped.

If a DLE is the last character received before a level 3 interrupt occurs due to the CA byte count reaching zero, the CA hardware sets the DLE remember bit in register X'0C' byte 0, bit 1. When the control program initiates the continuation of the command, this bit must be set with an output X'0C'. If the first character received is an STX, the CA resets control character monitoring.

Four consecutive SYN characters received at the start of an inbound transfer cause a level 3 interrupt request and set the channel stop condition X'02' byte 0, bit 5. Any non-SYN character resets monitoring for SYN characters.

Two-Processor Switch (TPS)

To be operational, the channel interfaces must be enabled. Both channel interfaces may be enabled, but simultaneous operation over the two interfaces is not permitted. Emulator subchannels are not available when both CA interfaces are enabled.

Any interface may be enabled or disabled from the MOSS. If a channel adapter has a TPS and is attached to a loosely-coupled host, or hosts, only one interface may be enabled at a time on the affected channel adapter. Only ESC operation is allowed in this partitioned mode.

TPS/TCS Mode

When the TPS feature is present, either TPS or TCS mode can be selected in the 3745.

- In **TPS mode** the A and B interfaces are connected to the **same host** and can be enabled at the same time.
- In **TCS mode** the A and B interfaces are connected to **two different hosts** and cannot work at the same time.

Loosely Coupled Host Attachment

The term 'loosely coupled' means either:

1. Two separate hosts each running its own access method (VTAM) with each host attached to an interface of a CA with TPS, or
2. A single host running different access methods, one access method associated with one interface of a CA via a TPS, and the other access method associated with the other interface of the same CA.

When running in a loosely coupled environment, only one of the interfaces may be enabled.

Alternate Path Host Attachment

'Alternate path attachment' is a single access method in a single host having access to both interfaces of a CA with TPS. With alternate path, if the access method issues a start I/O over one channel and that channel is busy with another device, the start I/O can then be issued over the alternate channel.

Note: More than one access method can operate in alternate path hosts, but only one can access both interfaces of a CA with TPS.

When running in an alternate path environment, both CA interfaces can be enabled.

Alternate Path Host Operations

The following TPS definitions must be understood:

1. **Neutral**: The CA is not in communication with either interface, and no active commands exist in the CA.
2. **Switched**: The CA is actively communicating with an interface. If the CA is active with a command, all additional communications are to be made through this interface. The switched state comprises three substates:

a. **Instantaneous Allegiance**: The CA enters this state when it traps 'select out' during a channel-initiated sequence, or a poll during a control unit-initiated sequence. If the CA presents DE without unit check (UC) during initial selection, and chaining is not indicated, the CA returns to the neutral state.

b. **Long-Term** or **Implicit Allegiance**: The CA enters this state when accepting a command without presenting DE, or when a No-Op is chained to the next command. This state lasts until the CA presents DE without UC to the channel. The CA remains switched to the same interface throughout. If chaining is not indicated and DE is not stacked, the CA returns to the neutral state.

c. **Contingent Allegiance**: This state is an extension of long-term allegiance. When a command ends with a UC status (because of some error), the CA enters this state, even though DE is presented to the command. The CA remains switched to the same interface, and does not return to neutral. The host, on receiving the UC status, issues a sense command to determine the cause of the error. The CA returns to neutral when receiving a command other than No-Op or Test I/O.

State	Substate	Meaning
Neutral		No allegiance.
Switched	Instantaneous Allegiance	Initial selection sequence, present async status, present tagged DE.
	Long-Term	From the initial selection till the end of the CCW chain execution.
	Contingent	UC status presented to host during initial selection or final status.
Return Neutral		At command end with DE acceptance and no chaining, DE accepted or stacked after busy, async status accepted or stacked, command other than No-Op or Test I/O in contingent state.

Ending statuses to the host are as follows:

1. **Normal Tagged Status.** This status is presented to the host in response to an initial selection command. The CA remains switched in long-term allegiance to the interface until the control program presents the normal ending status tagged for that interface.
2. **Tagged DE Status.** When the CA has presented a busy status to an interface because the other was in long-term or contingent state, that interface presents the DE status to the host when the CA returns to the neutral state. This DE status is tagged for that interface by the hardware to clear the busy status previously presented to the host. The tagged DE status frees the host so that it can issue the next command.
3. **Untagged Asynchronous Status.** When operating with tightly coupled processors, the control program can present asynchronous status to the host to initiate a command. This occurs when the CA is in the neutral state with no commands active.

   'Request in' is raised to both interfaces, and both interfaces compete for service. The first channel to poll the CA wins. Acceptance of the status

causes a level 3 interrupt request, and the CA returns to neutral. If the channel stacks the status, the CA returns to neutral and interrupts the control program. The untagged asynchronous status is then re-offered to both interfaces by the CA when the interrupt is serviced by the control program.

Presentation of Status

Although the CA has two channel interfaces, simultaneous operation of both interfaces is impossible. Therefore, when the CA is switched to one interface, they cannot operate simultaneously. The other interface refuses all channel-initiated sequences. When the CA is in long-term or contingent allegiance on one interface, the other interface presents the status X'10' (short busy sequence) to the channel: When 'select out' is trapped by the non-switched interface, it raises 'status in' and presents X'10'. The host channel responds by dropping 'hold out' or 'select out' and 'address out', thereby disconnecting the interface. The host does not issue further commands until a tagged DE status is received. This status is presented when the active CA interface returns to the neutral state. The CA hardware raises 'request in' and presents the DE status. If the DE status is stacked instead of accepted, the CA automatically tries to present the status again, independently of the control program.

Effect of System Reset

System Reset over Interface with Allegiance: When the CA recognizes the system reset, the CA is completely reset, ending any allegiance condition, and sets an initial selection interrupt request on level 3. However, if a DE status resulting from a previous busy status on the opposite interface is still pending, the CA is not reset.***:*** During system reset, if the opposite channel polls the CA in response to a 'request in' from some other control unit, the resulting 'select out' tag is bypassed. Similarly, any channel-initiated initial selection sequence to either interface causes the CA to switch to that interface, to present the busy status, and to return to the neutral state.

System Reset over Interface without Allegiance: When a system reset occurs on the interface without allegiance, any tagged DE status pending is reset. The rest of the CA is not reset, and no level 3 initial selection interrupt request is made.

System Reset when the CA is in Neutral: When a system reset occurs on a neutral CA, only the pending tagged DE status is reset on the interface, if any. The rest of the CA hardware is not reset, and no level 3 initial selection interrupt request is made.

Note: If a system reset is presented to both interfaces simultaneously, the CA is completely reset, and a level 3 interrupt request is made.

Effect of Selective Reset

Selective Reset over Interface without Allegiance: A selective reset cannot occur on the interface without allegiance. Therefore, the CA hardware is not reset, and no level 3 initial selection interrupt request is made.

Selective Reset over Interface with Allegiance: When the CA recognizes the selective reset, it returns to the neutral state, and issues a level 3 initial selection interrupt request.

No hardware reset occurs, except for a tagged DE status caused by a previous busy status on the opposite interface.

During the initial selection, if the opposite channel polls the CA in response to 'request in' from some other control unit, the resulting 'select out' tag is bypassed.

Similarly, if a channel-initiated initial selection sequence occurs on either interface, the CA switches to that interface, enters the instantaneous allegiance state, presents control unit busy X'70' as the initial status, and returns to the neutral state.

CA Error Condition

Any CA-detected error sets the appropriate bit ON in register X'0D'.

IOC bus parity error, operation in progress, interface setting, output exception check, PIO halt, and cycle steal halt do not cause CA level interrupts. Instead, the CA forces an IOC line error, the IOC bus hardware in the CCU requests a level 1 interrupt, indicated by CCU Input X'7E' bit 0.7 with a further definition of the IOC bus error in CCU register X'76'.

CA input X'0D' can be accessed to determine the cause of the interrupt. All other CA error conditions described cause level 1 interrupts.

Byte 0	Error Description	Level 1 Interrupt	Byte 1	Error Description	Level 1 Interrupt
0	IOC bus parity error (outbound from CCU)	No	0	Output exception	No
			1	PIO halt remember latch	No
1	Microcode detected error	Yes	2	Cycle steal halt remember latch	No
2	CA logic check	Yes			
3	(Not used)		3	Channel bus-in check (interface A)	Yes
4	(Not used)				
5	ESC address compare **(CADS)** or error/EP access **(BCCA)**	Yes	4	(Not used)	
			5	Channel bus-in check (interface B)	Yes
6	Operation in progress	No	6	(Not used)	
7	(Not used)		7	(Not used)	

IOC Bus Parity Error

This error is caused by bad parity on the IOC bus (outbound from CCU) during byte 0 and byte 1 transfers.

Microcode Detected Error

If this bit is a 1, the CA microcode has detected should-not-occur conditions (additional information can be found in input X'60').

CA Logic Check

When the hardware detects bad parity on the internal bus in the CA logic, it sets a logic check and causes a CA level 1 interrupt request. The control program should question the CA error register, (input X'0D', bit 0.2 = 1). Note this condition, and then reset the level 1 interrupt.

If the adapter was active on the channel in a data/status transfer state when the error occurred, the hardware will immediately terminate the transfer. The control program must reissue the output instructions to allow reselection of the channel interface. A status transfer of CE, DE, and UC should be issued to terminate the command.

ESC Address Compare Error (CADS) or Emulation Program Access (BCCA)

For **CADS**, if this bit is a 1, the program has issued an address for an emulator subchannel which is outside the initialized address range for this CA (out X'03'), or an out X'02' has been executed with bit 0.3 ON ('ESC operation') while output X'07' bit 1.5 ('Set ESC address active') was not set.

For **BCCA**, this bit is set to 1 when CP performs an output X'03' after it has set 'ESC address active'. This error condition will prevent the Emulation Program to access **BCCA.**

The CCU resets the error indication and the interrupt.

Operation in Progress

The bit is set ON at the start of data or status transfer by an output X'02' initiated by the control program. It means that the CA is in the process of initiating a control unit-initiated sequence by raising 'request-in' to the host, or that the CA is actually transferring data or status to the host.

This bit is reset when the data/status L3 is presented to the CCU or when interrupt request level 1 is reset by the control program.

Note: Bit 0.6 itself does not indicate that an error has occurred, nor does it correspond to a particular error condition.

Output Exception Check

The CA checks for CCU output commands that may interfere with a host data or status transfer. If this bit is set to 1, the hardware has detected an invalid output instruction.

Output instructions (with the exception of output X'07', output X'09', and ouput X'0A'), are not allowed while an input X'0D' operation is in progress (bit 0.6 = 1) and there is no initial selection interrupt. Output X'0B' (CADS only) is allowed only in response to any initial selection interrupt.

No level 1 interrupt request is raised.

PIO Halt Remember Latch

If this bit is a 1, the IOC has detected an error during an input or output PIO operation and has activated the halt signal. No level 1 Interrupt request is raised.

Cycle Steal Halt Remember Latch

If this bit is a 1, the IOC has detected an error during cycle steal and has activated the halt signal in the interface. Input X'02' can be executed to determine if the data was being transferred to an ESC or NSC address.

No level 1 interrupt request is raised.

Bus-In Check (Interface A or B)

If this bit is a 1, a hardware failure in the channel adapter bus-in logic has occurred during a data or address transfer to the host.

Bad parity during initial selection has no effect and initial selection terminates normally. Status transfers are not parity checked.

When this bit is ON, a level 1 interrupt request has been raised.

Channel Stop

Channel stop is on error if it occurs during an outbound data transfer. This sequence is detected by the CA hardware when passing bytes over the channel interface. The host processor responds to the CA tag lines 'service in' or 'data in' by raising the 'command out' tag line.

If operating on a byte multiplexer channel, the hardware will disconnect from the channel interface and cause a CA data/status L3 interrupt request.

If operating on a block or selector channel, the hardware will present channel end and request a data/status L3 interrupt. When an input X'02' is executed, bit 0.5 = 1 (channel stop/interface disconnect) will be active.

Interface Disconnect

This condition is detected by the CA hardware when the adapter is either in an initial selection, data transfer or status transfer sequence. 'Operation in' is up, and the host CPU has the 'address out' tag line up, and the 'select out' (hold out) tag line down before the completion of either of the above sequences.

The hardware will then cause either a CA initial L3 interrupt request, or a CA data/status L3 interrupt request, depending on when this condition was detected. Also, the CA will disconnect from the channel interface when working on the channel.

If this condition occurred during an initial selection sequence, the hardware will set 'interface disconnect' which is accessible by an input X'00' instruction (bit 0.1 = 1). If it occurs during a data/status transfer, the hardware will set 'channel stop/interface disconnect' which is accessible by an input X'02' instruction (bit 0.5 = 1).

I/O Error Alert

I/O error alert is a channel interface feature that detects a CA malfunction ('disconnect in' tag line raised).

I/O Error Alert from the CP: The I/O error alert sequence is executed when the CP cannot disable a host interface with an Out X'07' bit 1.7 (set allow channel interface disable). The I/O error alert feature must be present and enabled (out X'02' bit 0.7 = 1).

I/O Error Alert from MOSS: The sequence is executed by the CA when the MOSS raises the 'CA MOSS reset' line and the 'CA nohold' line.

Note: When a CA is enabled from the MOSS console but a HOST connected to the channel hasn't IPLed, the I/O Error Alert sequence may be executed.

CA Concurrent Maintenance (CACM)

Without impacting the CP, CACM allows a console operator to:

- Run diagnostics on a given CA
- Replace a failing CA
- Modify a CA configuration (add, delete, ...).

Starting CACM: The concurrent maintenance is started by the 'Shutdown for repair' command or by the 'Install new CA' command (refer to Chapter 10 (CA services) of the *Service Functions*)*.:* The above commands request the CP to:

1. Disconnect from the CA, which is left with its host interface(s) disabled and its level 1 and level 3 disabled.
2. Remove the CA from the AS and CS chains.

Concurrent maintenance is indicated by 'concurrent mode' active (MOSS CA output X'07'). The CA is no longer used nor addressed by the control program and can be reset, diagnosed (see the *Service Functions*), powered off, removed and replaced.

Note: The two CAs powered by a same power supply must be put in CACM mode before being diagnosed in concurrent mode, or before turning the power off.

Ending CACM: The concurrent maintenance is normally ended by the 'Restore CA after repair' command which performs the following:

1. Resets the CA
2. Initializes the CA
3. Requests the CP to connect to the CA, and to insert it into AS and CS chains.

Testing and Checking Hardware

The channel adapter contains hardware which allows exercising the checking logic that controls the various error indicators accessible by program with input X'0D', and channel bus checkout which is accessible by inputs X'00' and X'02'.

An imbedded checkout microcode already insures a partial test of the hardware. The checkout result is read via the command 'MOSS in X'4B'. Some functions must be checked by diagnostic program.

Autodiagnostics

Autodiagnostics are routines which are run sequentially whenever the microcode is not processing an interrupt.

If an autodiagnostic routine is interrupted, it will not be resumed at the point of interruption, but the next routine will be interrupted instead. This is to avoid a complex save/restore mechanism.

Functions Provided by Diagnostic Program

Selection Modes

Two selection modes ('concurrent' or 'non-concurrent') are available via the command 'MOSS out X'07'. The difference between these two modes resides in the validation of the commands received over the IOC interface. Interrupt requests for these two modes are routed to the CCU or MOSS, as specified in the definition of command 'MOSS out X'07'.

Channel Wrap Possibilities:

Refer to the *MIP* for test procedures.

- **Internal Wrap**

  A wrap possibility (on the CADR card) exists which helps the diagnostics in FRU detection. This may also be used to simulate some channel interface sequences. This function is executed via the command 'MOSS out X'4C'.

- **External Wrap**

  This function is executed via the command 'MOSS out X'4C'. Two external wrap connectors must be provided in order to wrap the CAs at the channel tailgate, one to wrap tags-out to tags-in, and one to wrap bus-out to bus-in. The CA tag wrap connector P/N 03F4300 or 26F1754, and the bus wrap connector P/N 03F4301 or 26F1755 must be used (see Figure 7-8 on page 7-59 through Figure 7-11 on page 7-60).

  Bus and tag terminators must be plugged in the controller out connectors (light gray). This external wrap possibility is provided only to test the drivers/receivers and tailgate wiring of the channel interface.

Tag Wrap Plug P/N 03F4300

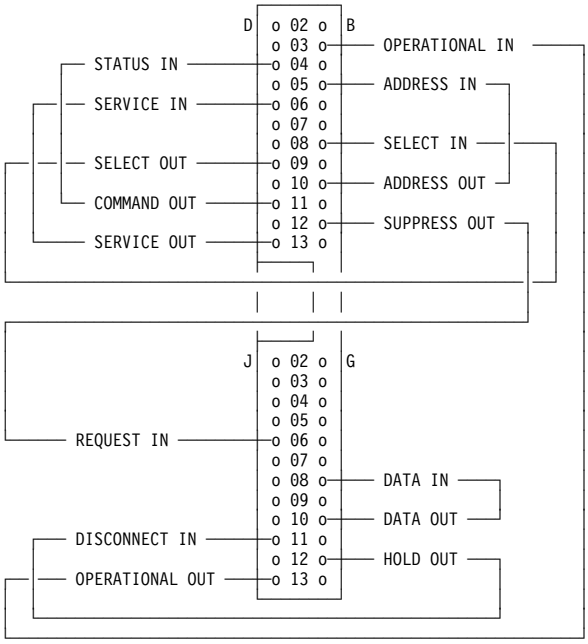

Figure 7-8. Tag Wrap Plug Wiring (P/N 03F4300 - Mating Side)

Bus Wrap Plug P/N 03F4301

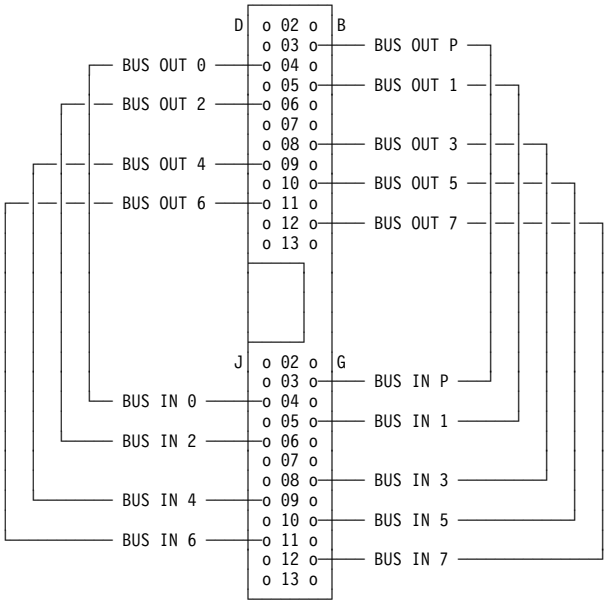

Figure 7-9. Bus Wrap Plug Wiring (P/N 03F4301 - Mating Side)

Tag Wrap Plug P/N 26F1754

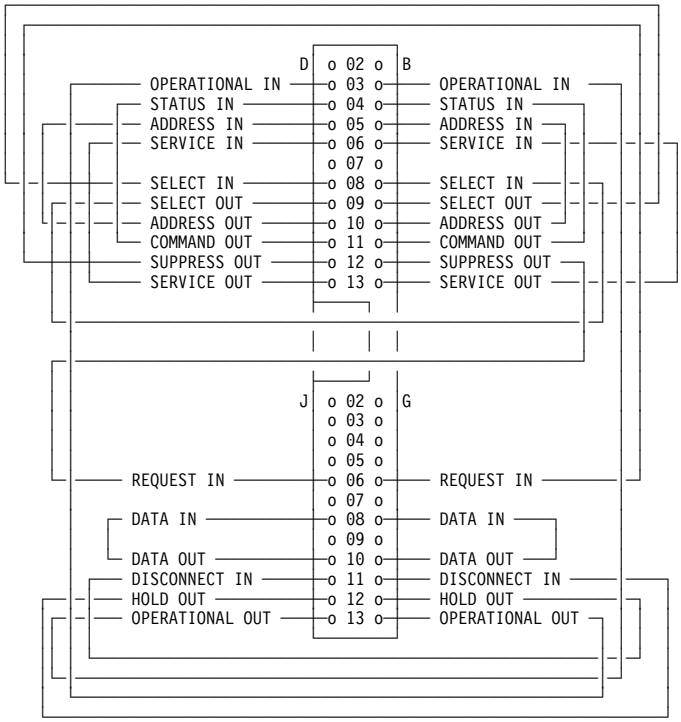

Figure 7-10. Tag Wrap Plug Wiring (P/N 26F1754 - Mating Side)

Bus Wrap Plug P/N 26F1755

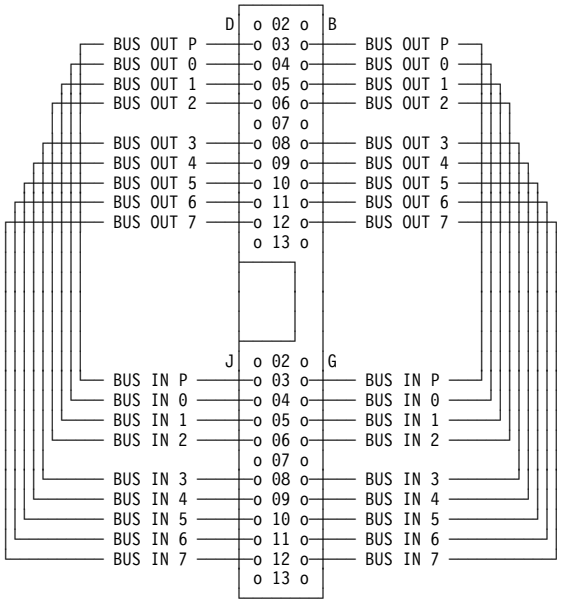

Figure 7-11. Bus Wrap Plug Wiring (P/N 26F1755 - Mating Side)

CA Services

Refer to the *Services Function*, SY33-2055, for more details.

The command Out X'07' from MOSS with bit 0.2 = 1 is provided to select a specified CA in order to enable CA services from MOSS. This function allows to:

- Display CA status.
- Display interface test points.
- Enter host attachment information at installation time.
- Issue specific commands to the CA, such as:
  - Start/stop trace
  - Dump
  - Display storage and registers
  - Reset
  - Initialization.
- Use the CA concurrent maintenance (CACM) commands.

CA Interface Display

Refer to the *Advanced Operations Guide*, SA33-0097, for more details.

As soon as the local console is powered ON, the CA interface display screen appears. This screen can also be displayed by selecting the channel interface display (CID) function from MOSS menu 2.

The information displayed is:

- Host attachment information
- NSC address
- MOSS enable/disable request
- Interface status (enabled/disbabled).

The CID screen also allows to modify the enable/disable request.

Channel Monitoring

Purpose of Channel Monitoring

In the 3745, when a CCU comes down, the time necessary to switch from the failing CCU to the other one and during which the MOSS is unavailable for channel monitoring, is about 90 seconds. During this time, new host requests or previous requests left pending cannot be processed, and may result in channel time outs which are not acceptable. To avoid those conditions, the channel monitoring function has been implemented in the CA microcode.

- The CA will enter channel monitoring mode either when the 'adapter reset' line is active from the MOSS, or when it receives an out X'4F' with bit 0.0 = 1 (set channel monitoring).
- The CA exits from channel monitoring when it receives either an Out X'4F' with bit 0.1 = 1 (reset channel monitoring), or an Out X'4F' with bit 0.2 = 1 (force interface disable).

CA Initialization

The CA initialization is performed when a CA receives a POR signal, either at general power ON, or through the MOSS 'Reset' command.

Initialization First Part (Checkout)

At checkout completion, the CA is in the following state:

1. IOC bus interconnection enabled.
2. MOSS interconnection enabled.
3. Host interfaces disabled.

The results of the checkout are available to the MOSS microcode.

Initialization Second Part

This part is performed during IPL phase 1A, or during fallback, or during the 'Restore' CACM command. The MOSS microcode initializes each CA.

Initialization Third Part (Chaining)

Only those CAs that passed the first and second parts of the initialization can be installed in autoselection and cycle steal chains. Chaining process is performed during IPL and fallback.

Chapter 8. Maintenance and Operator Subsystem (MOSS)

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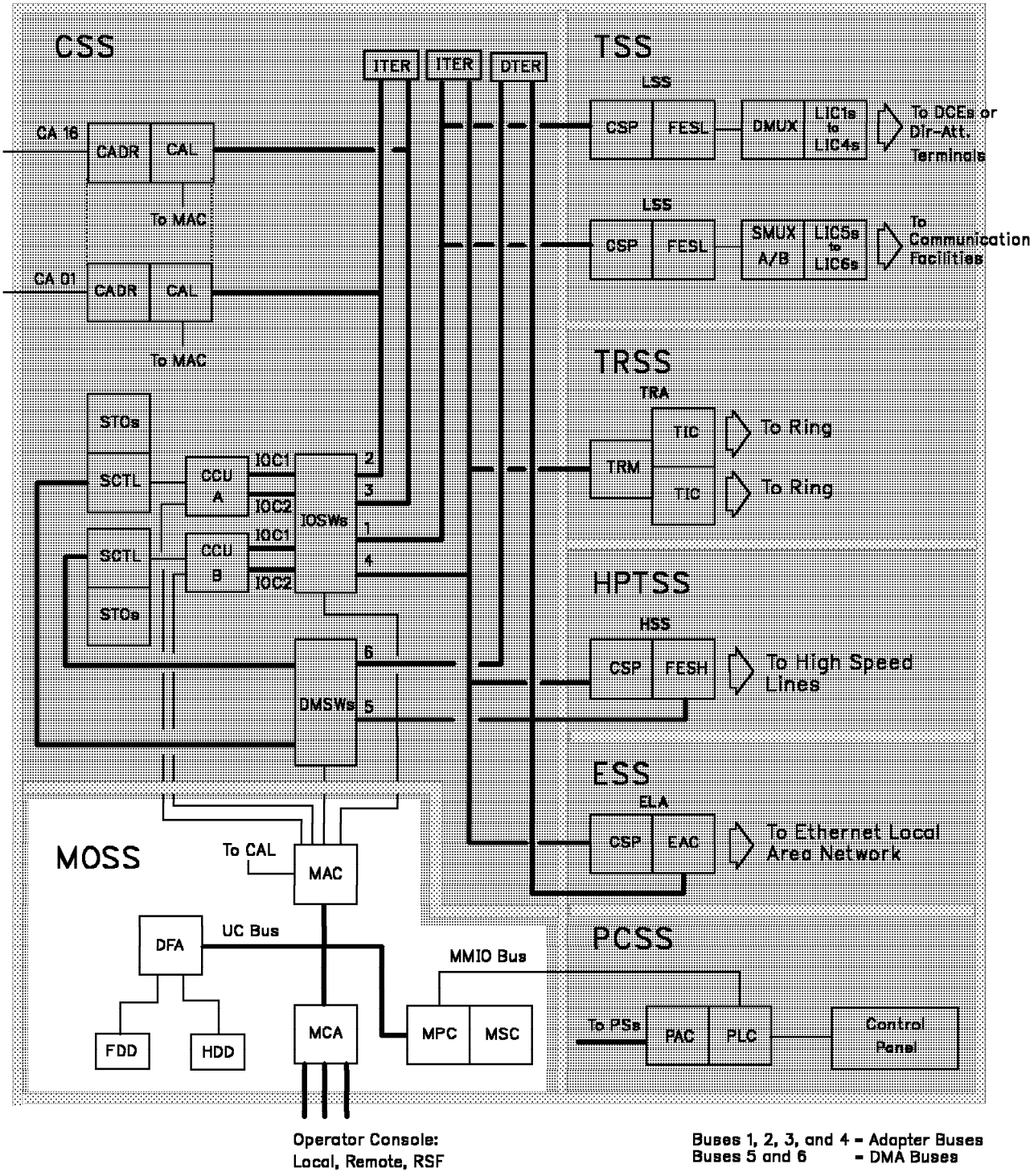


Figure 8-1. MOSS in 3745 Data Flow. For models 21A-61A, DMA and IOC buses are connected to the CBC in the 3746-900. The MCA card is replaced by the MLA card which interfaces to the MPC card through the MMIO bus. This MLA card links the MOSS to the Service Processor through a LAN.

Introduction

MOSS is the service processor of the communication controller. It performs IPL functions, machine initialization, and provides the operator with tools for problem determination.

The 3745 MOSS is based on a microprocessor which controls a 1-MB main storage on 3745 Models 210-610 or 2-MB storage on 3745 Models 21A-61A, the MIOC buses, the channel adapters, the consoles (local, remote/alternate, and RSF) on 3745 Models 210-610 or the service processor through a LAN for 3745 Models 21A-61A, the disks (hard disk and flexible disk), and the switching of adapter buses (CCUs in twin configuration).

MOSS interconnects with the power logic card which drives the control panel. The MOSS logic, the flexible disk drive, and the hard disk drive are powered by a specific power supply, so that removing power from the MOSS board does not impair the operation of the system.

On 3745 Models 21A-61A, the MLA card links the MOSS to the service processor via the LAN. The MLA card interfaces to the MOSS processor (MPC card) via the MMIO bus.

MOSS Processor

The MOSS processor drives the MOSS. It has its own instruction set, and does the usual processing activities: instruction fetching, instruction decoding, and instruction execution.

The MOSS processor responds to interrupts from the CCU and its attached adapters (LAs, CAs), and from its own error detection circuits. It controls access to the MOSS storage. The MOSS processor is packaged on the MPC card.

Packaging

Refer to Figure 8-3 on page 8-5 for MOSS structure on 3745 Models 210-610 and to Figure 8-4 on page 8-6 for MOSS structure on 3745 Models 21A-61A. The MOSS board includes:

- A MOSS processor card (MPC) with a 32-kB ROS, a time-of-day (TOD) clock, a storage error correction and checking circuit. The MPC card connects UC buses, the MSC card and the power logic card (PLC).

  Note: Each time that the MOSS is reset, a led is lit on the MPC card. This led is turned OFF by the ROS microcode when the connection with the PLC card is established.

- A 1-MB RAM MOSS storage, on 3745 Models 210-610, or a 2-MB RAM MOSS storage, on 3745 Models 21A-61A, card (MSC card).
- A power logic card (PLC), which interconnects the MOSS control panel to the MPC card. The PLC card is powered by a specific MOSS power supply, in order to allow the remote power function, and manages the whole power control subsystem (see Chapter 10 for details).
- A power analog card (PAC) to manage the analog signals coming from all the power supplies.
- A MOSS adapter card (MAC) with four modules:

  - One adapter module for CCU-A bus (MCCU-A)
  - One adapter module for CCU-B bus (MCCU-B)
  - One adapter module for 16 channel adapters (MCAD)
  - One module to connect the two 3745 switching devices (SWAD).
- On 3745 Models 210-610, a MOSS console adapter card (MCA), with one oscillator, drivers/receivers (EIA V.28/RS-232-C), and three console adapter modules providing three ports for:
  - A local console
  - A remote/alternate console
  - An RSF console.

  On 3745 Models 21A-61A, a MOSS LAN adapter card (MLA) which links the MOSS to the service processor through the LAN.
- A disk file adapter card to attach:
  - One flexible disk drive (FDD),
  - One hard disk drive (HDD).

Note: See pages YZ-031 for MOSS card and connector locations, and pages YZ-331 for test points.

MOSS Reset

When a MOSS reset occurs, the led on the top of the MPC card is turned ON. The panel displays code 001, a read MMIO bus is started by the MOSS code. If the result is good, the led is turned OFF and the display code goes to 002. If the result is not good after a two-second time out, the led starts blinking.

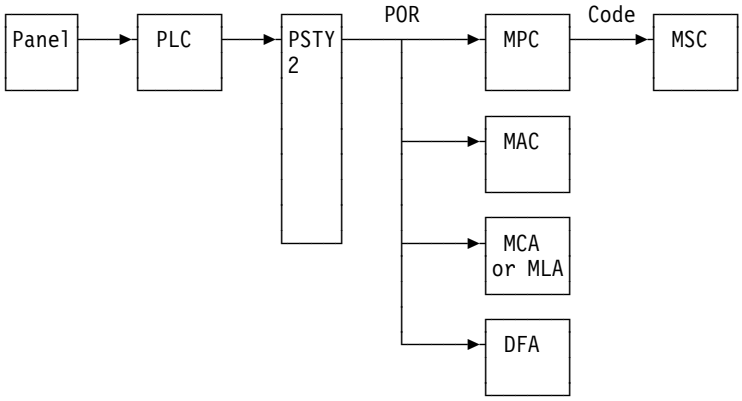


Figure 8-2. MOSS POR Flowchart

- MPC reset consists of terminating the operation in progress and initializing internal registers. The reset sequence does not initialize main storage, or register space. Those are initialized by storing into them with good parity. Several specific control areas are also initialized by the IML program.
- A MOSS reset (ONLY) is performed with *Function = 1* (MOSS IML) at the control panel and either POR or VALIDATE.

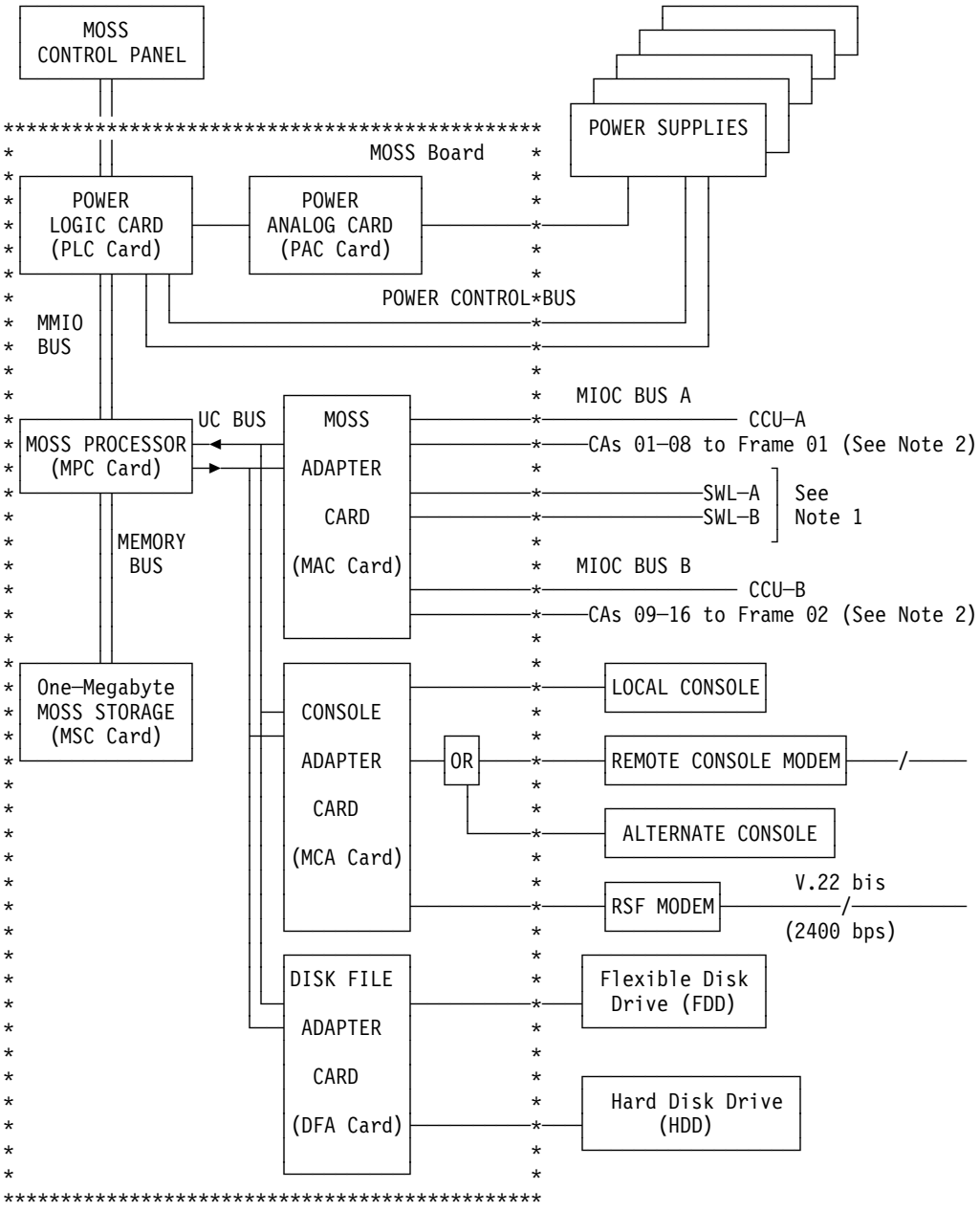


Figure 8-3. MOSS Structure for 3745 Models 210-610

Note 1: 'SWL-A' or 'SWL-B' allow bus switching to CCU-A or CCU-B.
Note 2: 'CAs 01-08' and 'CAs 09-16' are control lines only. They allow enabling/disabling or resetting the CAs.

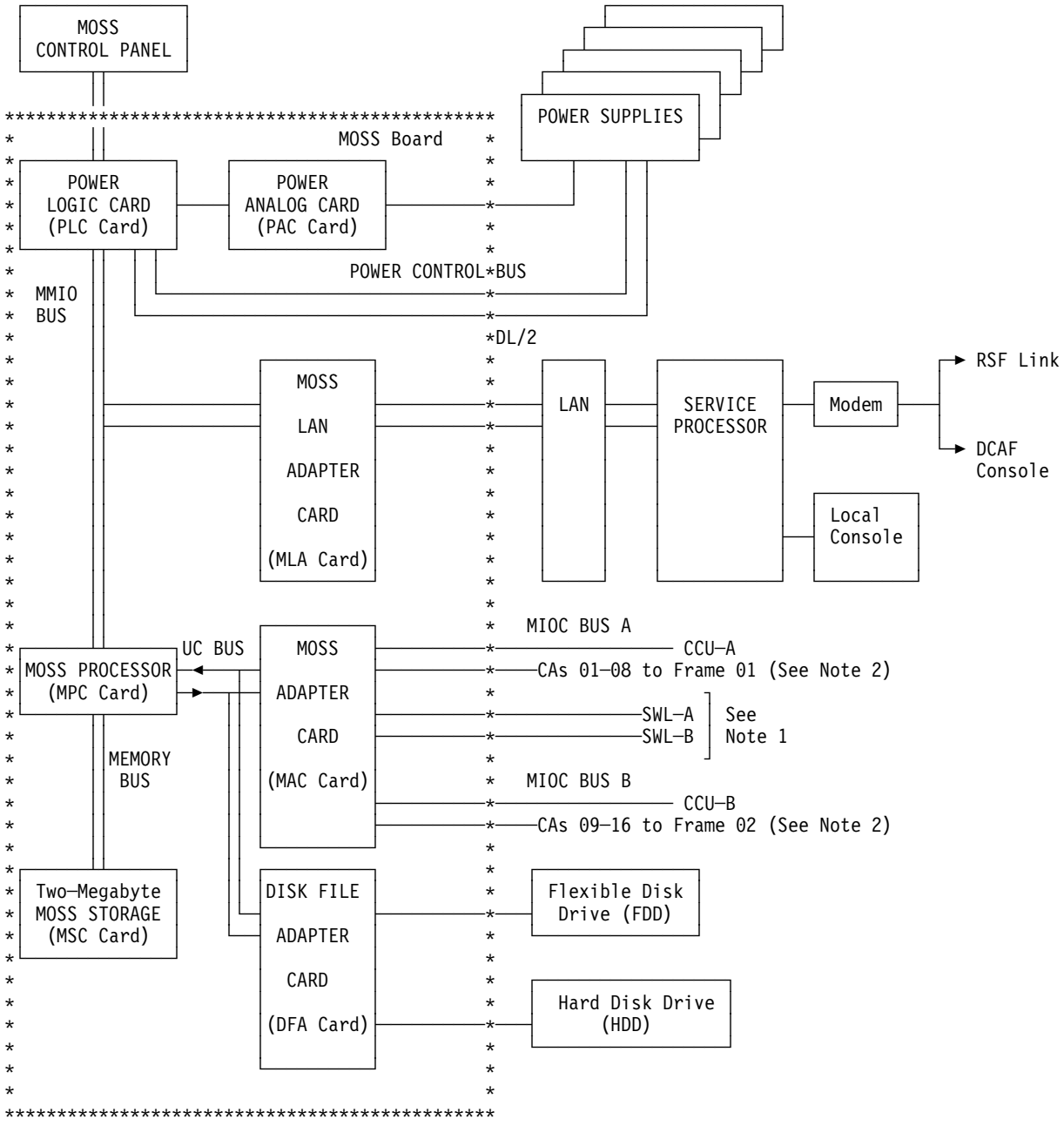


Figure 8-4. MOSS Structure on 3745 Models 21A-61A

Note 1: 'SWL-A' or 'SWL-B' allow bus switching to CCU-A or CCU-B.
Note 2: 'CAs 01-08' and 'CAs 09-16' are control lines only. They allow enabling/disabling or resetting the CAs.

MOSS Functions

The maintenance and operator subsystem (MOSS) provides access to the 3745 and makes the following components easier to maintain:

- Control program (NCP, PEP).
- Central control unit (CCU).
- Channel adapters (CA).
- Line adapters (TSS, HPTSS, TRSS, ESS, and LA microcode).
- Line interface cards (LICs/TICs).
- The MOSS processor itself, its microcode, and the I/O adapters used to attach the control panel, the operation consoles, the flexible and hard disk drives, the CCUs, the switches and the channel controls.
- Controller operating mode (single, twin stanby, twin backup, twin dual).

Using the MOSS, the service personnel can:

1. Initialize the 3745 with:
   - Standalone IPL from disk
   - Hardware checkout diagnostics
   - IML/IPL from the control panel or the console
   - CCU IPL
   - Line adapter IML.
2. Maintain the 3745 with:
   - Remote support facility (RSF) on 3745 Models 210-610
   - Concurrent diagnostics and concurrent maintenance
   - Box event handling (error recording, analysis and display, alert/alarm generation)
   - Line services (line wrap tests, line interface display, token-ring interface display, ESS interface display)
   - CCU control program procedures
   - Machine history files: configuration data file (CDF), machine level table (MLT), IPL port table
   - Password management on 3745 Models 210-610
   - Microcode utilities (dumps and file transfer to host, MCF, RECFMS)
   - CA control/status display from the console
   - Machine status area display.
3. Use 3745 services such as:
   - CCU services
   - TSS services
   - TRSS services
   - CA services
   - Power services
   - Time services.

MOSS States

Some states are viewed by the NCP or PEP (DOWN, INOPERATIVE, OFFLINE, ONLINE). Other states exist when the NCP or PEP is not loaded in the CCU (DOWN, ALONE).

There is one MOSS state for each CCU.

- **MOSS DOWN or MOSS INOPERATIVE** indicates that no program is running in the MOSS or that MOSS IML is in progress. In this state the 'MOSS Inoperative' line is up and the CCU interface is disabled.
- **MOSS ALONE** indicates that the MOSS microcode is loaded and operational (CP not loaded).
- **MOSS OFFLINE** indicates that the MOSS microcode is running in the MOSS, but that communication cannot be established with the NCP/PEP (except for exchange with CLDP, and NCP/PEP initialization, which are part of the 3745 system IPL). In this state, the CCU is enabled.
- **MOSS ONLINE** indicates that the MOSS microcode is running and allows communications with the NCP/PEP. In this state, the CCU interface is enabled.

(Numbers refer to the steps of "MOSS Changes of State")

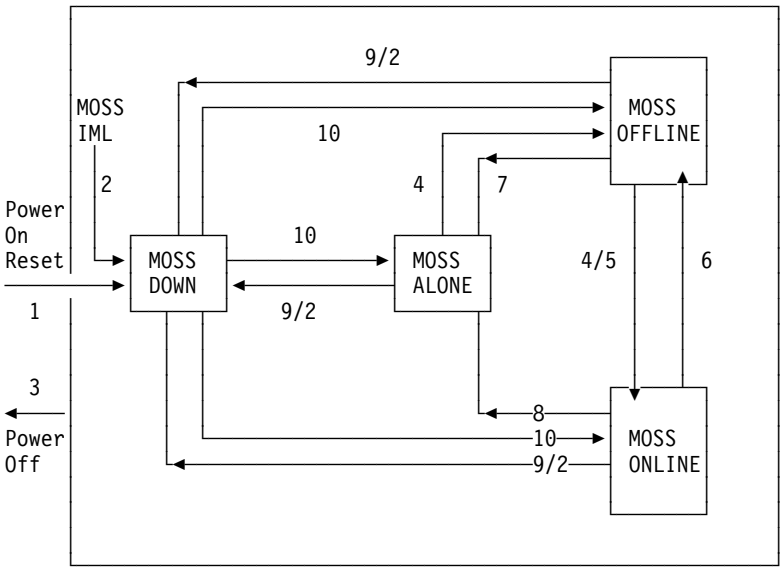


Figure 8-5. MOSS Changes of State

MOSS Changes of State

The following is a description of the events and actions that cause a MOSS state change. Step numbers identify events and actions in Figure 8-5.

Step 1. POWER ON RESET, according to panel option:

- Panel option = MOSS IML ('Function' = 1). The MOSS DOWN state is entered during the time MOSS IML is performed, then MOSS ALONE [10] is entered and is kept until further action.
- Panel option = NORMAL or DISKETTE MODE. The MOSS DOWN state is entered during the time MOSS IML is performed, then MOSS

ALONE [10] is entered, then MOSS OFFLINE [4], then MOSS ONLINE [5]. This is the full system IPL.

Step 2. MOSS IML request at panel (Function = 1). The same sequence occurs as in step 1 above, according to the panel option.

Step 3. POWER OFF. The full system leaves its current state.

Notes:

- If the MOSS is powered OFF after an 'IPL Complete', the connection MOSS to control program is not broken. At MOSS power ON, the MOSS will be automatically connected to the control program.
- If the MOSS is powered OFF during phase 1 of the IPL, the CCU status may be wrong at power ON. For example, IPL-REQ, RESET, or POWER DOWN status may be replaced by the READY status.

Step 4.

- A NORMAL IPL has been requested, [1] or [2].
- 3745 IPL has been requested from the console menu.

Step 5.

- A NORMAL IPL has been requested, [1] or [2].
- 3745 IPL has been requested from the console menu.
- The MOSS operator enters a MOSS ONLINE command from the console to exit from the OFFLINE MODE.

Step 6.

- The MOSS operator enters a console MOSS OFFLINE command.
- In case of hardware error on the MOSS/CCU interface during the processing of a mailbox.
- In case of a timeout occuring while processing exchanges from the NCP.

Step 7.

- During a NORMAL IPL the process aborts and cannot be completed successfully.
- A channel or program IPL request is presented to MOSS.
- A CCU hard check is presented to MOSS.

Step 8.

- A channel or program IPL request is presented to MOSS.
- A CCU hard check is presented to MOSS.

Step 9.

- A MOSS abend occurred.
- START panel request while the MOSS was in the OFFLINE, ONLINE, or ALONE state.
- IML command entered at the console.

Step 10.

- If the reason to enter the MOSS DOWN state was an abend or an IML command entered at the console, after MOSS re-IML the final state is the one which was interrupted by the abend.
- If the reason to enter the MOSS DOWN state was a START panel request or an IML command entered at the console, after MOSS re-IML the final state depends on the function option selected. In case of START IML MOSS, the final state is the same as the one which was interrupted, except for MOSS ONLINE which is forced to MOSS OFFLINE.

MOSS Microcode

The MOSS microcode provides the basic functions of the different MOSS applications. These applications schedule the various tasks, and communicate with the adapters controlled by the MOSS (the CCU is considered as an adapter by the MOSS) and with the devices.

Three types of microcode application must be considered:

System Applications

System applications are resident and provide information on the system state, or record events occurring in the system (machine status area, BER recording/alert, CCU re-IPL, loop detection, power task, channel monitoring, LA re-IML, automaint) and on 3745 Models 21A-61A, MOSS-E View, MOSS-E command responder).

MOSS Operator-Controlled Applications

One application at a time is under the control of the operator to provide interactive functions. These applications may address one or two CCUs.

Background Applications

This host operator-controlled task allows the host system to initiate the transfer of a dump data set: NCP, MOSS, LA and associated data set (BERs, patches, MCF, CDF, port swap ...). Transfer through both CCUs can take place in parallel.

Transfer NCP dump from MOSS disk to MOSS-E disk when dump has just been taken during re-IPL.

MOSS Interrupt Levels

The MOSS processor has eight interrupt levels. Level 0 has the highest priority.

Table 8-1 summarizes the functions of each level, which are explained below.

Table 8-1. MOSS Interrupt Level Summary

Level	Functions
0	MOSS IML Errors stored in EIRV register Dump requests MIOC interface errors Switch interface errors Power MMIO errors MOSS hang detection
1	Error EIRV processing CCU high-level interrupt requests MOSS 100-ms timer interrupts CA high level interrupt requests CCU power off interrupt
2	Power adapter requests
3	Console adapter requests on 3745 Models 210-610 or LAN adapter requests on 3745 Models 21A-61A
4	CCU low-level interrupt requests Line adapter interrupt requests CA low level interrupt
5	Disk/Diskette adapter requests
6	MOSS supervisor
7	MOSS tasks

Control Information

Control information can be accessed only through the use of the control immediate (KI) instruction[1], and consists of the following areas:

- Current Priority Level (CPL)
- Last Priority Level (LPL)
- Master Mask (MM)
- Common Mask (CM)
- DMA Mask (DMM)
- Programmed Interrupt Request Vector (PIRV)
- I/O Interrupt Request Vector (IOIRV)
- Error Interrupt Request Vector (EIRV)
- Primary Register Set Number (PRS)
- Secondary Register Set Number (SRS)
- Channel Mask (CHM)
- Condition Indicators (CI)
- Instruction Address (IA)
- Diagnostic Information Vector (DIV)

[1] Except for the IA Register which is accessed with BALR R1,0.

Detection of MOSS Errors

Hardware Checking

- Errors detected by the MOSS processor are reported via the EIRV and DIV registers. Any bit set in the EIRV register causes a level 0 interrupt to the processor.
- Errors detected by the adapters are reported via the specific IOIRV register. The error type is posted in the basic status register of each adapter.
- Error correction and checking by MSC:
  - Single error correction
  - Double error detection

(See Table 8-2 on page 8-13, Table 8-3 on page 8-14, and Table 8-4 on page 8-14.)

Software Checking

Software checking, performed by the MOSS microcode, consists in verifying the consistency of the data exchanged between the different components (applications, supervisor, or adapter processors) or within each component itself.

Software checking also consists in integrating the elementary errors on each component (counts and thresholds), before deciding that the corresponding component is out of service.

These errors are reported at level 0 via PIRV. (See Table 8-5 on page 8-14.)

Loop Detection

The loop detection device watches for loops in the MOSS microcode. This is done at two levels:

1. By software, the time counters are reset at regular intervals.
2. By hardware, MOSS INOP is set when a loop is actually detected.

Error Detection and Reporting

Severe MOSS/System errors are detected by MOSS level 0 and 1 interruptions. MOSS can detect errors in the following areas:

- Storage/Data ECC errors
- I/O checks and PIO errors
- Adapter check errors
- Processor errors
- Microcode program errors.

The hardware-detected errors are reported through the following registers:

- EIRV register
- DIV register
- IOIRV register
- Status registers of the MOSS adapters.

If any one of the six EIRV bits 0-5, or IOIRV bit 0 is set to 1 by a detected error, an interrupt is initiated to level 0.

The microcode-detected errors are reported through:

- PIRV register if PIRV bit 0 is set to 1 (an interrupt is initiated to level 0).
- Abend codes set up by the microcode program.

Error Interrupt Request Vector (EIRV) Register

Table 8-2. EIRV Register

Bit	Function
0	I/O control check
1	I/O timeout check
2	Storage data/ECC check
3	Exception check
4	Channel I/O check
5	Internal control check
6	Instruction address modifier check
7	0

Diagnostic Information Vector (DIV) Register

Table 8-3. DIV Register	
Bit	**Function**
16-17	00
18	Main storage operation error
19	Register backing store operation error
20-23	Identify the MMIO device in error
24	Specification exception (Memory subsystem detected invalid address)
25	PSV swap error
26	Operation exception (Attempt to execute an invalid instruction)
27	Register precision exception
28	Address exception (Address > X'7FFFFF' or wrapped 0)
29	Instruction fetch error
30	Fixed point overflow
31	External error loaded in EIRV/DIV registers

I/O Interrupt Request Vector (IOIRV) Register

Table 8-4. IOIRV Register	
Bit	**Function**
0	MAC/MIOC or MAC/SWITCH checks
1	MAC CCU HLIR/CA HLIR/Timer
2	Power control interrupt request
3	MCA interrupt request
4	MAC low-level interrupt request
5	DFA interrupt request
6	Not used
7	Not used

Programmed Interrupt Request Vector (PIRV) Register

Table 8-5. PIRV Register	
Bit	**Function**
0	MOSS error level 0 handler
1	MOSS error level 0 process
2	Power control interrupt request
3	MOSS MCA level 3 handler
4	MOSS MAC level 4 handler
5	MOSS DFA level 5 handler
6	MOSS supervisor level 6 and task scheduler
7	MOSS tasks level 7 programs

MOSS/CCU Communication

The MOSS communicates with the CCU(s) by reading/writing information from/in the MIOC direct registers (MCCU A or MCCU B):

These registers appear as external registers to the MOSS. Some of them can be addressed by the CCU using its own register address definition. There is no relationship between the MOSS and CCU register addresses.

The MOSS executes direct or indirect operations via the MOSS/CCU connection.

Direct Operations

During direct operations, without interrupting the CCU, the MOSS reads or writes any MIOC register to:

- Check the CCU status (carry or zero flags, current interrupt level)
- Place the CCU in the diagnostic mode
- Prepare the branch trace/address compare circuits
- Control LSSD operations
- Prepare indirect operations.

Indirect Operations

During indirect operations, the MOSS reads or writes any CCU data flow register, working register, local store, or CCU X'7x' register. Indirect operations take several CCU cycles to run. Indirect looped operations allow storage diagnostics (storage scan).

MOSS/CCU Adapter (MCCU) Registers

The contents of the following registers may be retrieved from the MOSS BERs. MCCU-A adapter address: X'12', MCCU-B adapter address: X'13'. Adapter reset: Command X'02'.

Status 0 (STAT0) Register

X'04': Reset STAT0 register under mask.
X'06': Set STAT0 register under mask. X'07': Read STAT0 register.

Table 8-6. Status 0 Register

Byte 0		**Byte 1**	
Bit	Name	Bit	Name
0	MOSS inoperative	0	Invalid PIO command
1	Step 1 μs counter (parity predict)	1	UC bus parity check
2	MIOC/CCU counter (parity predict)	2	(Not used)
3	HW/Burst counter (parity predict)	3	MIOC busy
4	CCU busy timeout	4	CHIO halt
5	MIOC timeout	5	Equipment check
6	MIOC parity check in	6	Enable interrupt level 0
7	MIOC parity check out	7	Level 0 interrupt

Status 1 (STAT1) Register

X'14': Reset STAT1 register under mask.
X'16': Set STAT1 register under mask. X'17': Read STAT1 register.

Table 8-7. Status 1 Register

Byte 0	**Byte 1**		
Bit	Name	Bit	Name
0-3	0000	0-3	0000
4	Enable CCU power OFF	4	CCU power OFF
5	Enable CCU HLIR	5	CCU HLIR (read only)
6-7	00	6	Enable all interrupts
		7	Level 1 interrupt

Status 4 (STAT4) Register

X'24': Reset STAT4 register under mask.
X'26': Set STAT4 register under mask. X'27': Read STAT4 register.

Table 8-8 (Page 1 of 2). Status 4 Register

Byte 0	**Byte 1**		
Bit	Name	Bit	Name

Table 8-8 (Page 2 of 2). Status 4 Register			
Byte 0	**Byte 1**		
0-2	000	0	Program wait
3	Enable cycle steal end	1-2	00
4	Enable CCU LLIR	3	Cycle steal end
5	Enable LA IOC1 interrupt	4	CCU LLIR
6	Enable LA IOC2 interrupt	5	LA IOC1 interrupt
7	0	6	LA IOC2 interrupt
		7	Level 4 interrupt

MOSS Mode (MMOD) Register

X'3A': Write MMOD register
X'3B': Read MMOD register

Table 8-9. MMOD Register (MCCU)

Byte 0		**Byte 1**	
Bit	Name	Bit	Name
0	0 (Not used)	0	Parity prediction diag 1 [3]
1	Step 0 [2]	1	Parity prediction diag 0 [3]
2	Step 1 [2]	2	MIOC diag 2 [4]
3	Freeze [2]	3	MIOC diag 1 [4]
4	MIOC direct operation mode [2]	4	MIOC diag 0 [4]
5	MIOC write mode (CHIO) [2]	5	MOSS diag 2 [5]
6	MIOC read mode (CHIO) [2]	6	MOSS diag 1 [5]
7	D register full [2]	7	MOSS diag 0 [5]

---

[2] Bits 0.1 to 0.7 are sense only (bring-up or diagnostic purpose).

[3] Bits 1.0-1.1 decode:

00 = No force error 01 = Force step/Hw/MIOC parity predict
11 = No force error 10 = Force 1 us/burst/CCU busy parity predict

[4] Bits 1.2-1.4 decode:

000 = No force error
001 = Force wrong parity on the MIOC address bus
010 = Force wrong parity on the MIOC data bus
011 = Invert parity from the MIOC
100 = Inhibit read/write strobe (MIOC timeout checking)
101 = Force CCU busy bit (CCU busy timeout checking)
110 = Force data register byte 0 on MIOC address bus,
and data register byte 1 on MIOC data bus.
111 = No force error

[5] Bits 1.5-1.7 decode:

000 = No force error
001 = Force CCU HLIR and CCU power OFF interrupts.
010 = Force 'program wait' and CCU/LAs LLIR interrupt lines.
011 = Invert module identification.
100 = Invert both parities generated during a read command
(except read MMOD register or status registers).
101 = Invert UC bus B0 parity generated at TD time in write mode.
110 = Invert UC bus B1 parity generated at TD time in write mode.
111 = No force error

COUNT Register

COUNT and CHCV registers are used to transfer data to/from CCU storage to/from MOSS storage.

X'6A': Write COUNT register
X'6B': Read COUNT register

Table 8-10. Count Register

Byte 0		**Byte 1**	
Bit	Function	Bit	Function
0	Burst 0	0	Halfword count 6
1	Burst 1	1	Halfword count 7
2	Halfword count 0	2	Halfword count 8
3	Halfword count 1	3	Halfword count 9
4	Halfword count 2	4	Halfword count 10
5	Halfword count 3	5	Halfword count 11
6	Halfword count 4	6	Halfword count 12
7	Halfword count 5	7	Halfword count 13

Channel Control Vector (CHCV) Register

X'6C': Write CHCV register
X'6D': Read CHCV register

Table 8-11. CHCV Register

Byte 0		**Byte 1**	
Bit	Function	Bit	Function
0-4	00000	0	0 = Write
5	Channel pointer number:		1 = Read
	0 = CPR within set 12-15	1	0 = Indirect mode
	1 = CPR within set 8-11		(Must be 0 if bit 0.6 is 1)
6	0 = Mode determined by bit 1.1		1 = Direct mode
	1 = Indirect mode	2-6	CHCV pointer number
7	0 = Short address	7	0 = CHCV 0-6 used
	1 = Long address		1 = CHCV 0-6 not used

MOSS/CA Adapter (MCAD) Registers

Adapter address: X'22'
Adapter reset: Command X'02'

Interrupt 1 (INTP1) Register

X'04': Reset INTP1 register under mask.
X'06': Set INTP1 register under mask.
X'07': Read INTP1 register.

Table 8-12. INTP1 Register

Bit	Function
0	Invalid PIO command
1	UC bus parity check
2-4	000
5	Equipment check
6	Enable interrupt level 1
7	Level 1 interrupt

Extended Interrupt 1 (EINTP1) Register

X'14': Reset EINTP1 register under mask.
X'16': Set EINTP1 register under mask.
X'17': Read EINTP1 register.

Table 8-13. EINTP1 Register

Bit	Function
0	Enable timer
1	Enable CAs 1-8 HLIR
2	Enable CAs 9-16 HLIR
3	0
4	100 ms timer
5	CAs 1-8 HLIR
6	CAs 9-16 HLIR
7	0

Interrupt 4 (INTP4) Register

X'24': Reset INTP4 register under mask.
X'26': Set INTP4 register under mask.
X'27': Read INTP4 register.

Table 8-14. INTP4 Register

Bit	Function
0	Enable fault flags
1	Enable CAs 1-8 LLIR
2	Enable CAs 9-16 LLIR
3	0
4	Fault flags
5	CAs 1-8 LLIR
6	CAs 9-16 LLIR
7	Level 4 interrupt

Sense Fault Flag Register

Table 8-15. Sense Fault Flag Register	
Bit	**Function**
0	Fault Enable/Reset 1-2
1	Fault Enable/Reset 3-4
2	Fault Enable/Reset 5-6
3	Fault Enable/Reset 7-8
4	Fault Enable/Reset 9-10
5	Fault Enable/Reset 11-12
6	Fault Enable/Reset 13-14
7	Fault Enable/Reset 15-16

DIAG Register

X'3A': Write DIAG register.
X'3B': Read DIAG register.

Table 8-16. DIAG Register	
Bit	**Function**
0	All CAs disabled [6]
1-3	Not used
4-7	Force error [7]

Sense CA Enabled Registers

X'4B': Sense CAs 1-8 enabled

Table 8-17. Sense CAs 1-8 Enabled	
Bit	**Function**
0	CA 1 enabled
1	CA 2 enabled
2	CA 3 enabled
3	CA 4 enabled
4	CA 5 enabled
5	CA 6 enabled
6	CA 7 enabled
7	CA 8 enabled

X'4D': Sense CAs 9-16 enabled

Table 8-18. Sense CAs Enabled	
Bit	**Function**
0	CA 9 enabled
1	CA 10 enabled
2	CA 11 enabled
3	CA 12 enabled
4	CA 13 enabled
5	CA 14 enabled
6	CA 15 enabled
7	CA 16 enabled

---

6 Sense only

7 Bits 4-7 decode:

0000: No force error
0001: Force CAs HLIR interrupt lines.
0010: Force CAs LLIR interrupt lines.
0011: Force 'CA enabled' lines.
0100: Invert module identification.
0101: Force UC parity check error, except in write diag register.
0110: Force UC parity generate error, except in read diag register.
0111: No force error.
1000 to 1111: No force error.

CA MOSS Power-On-Reset (CAMPOR) Register

X'44': Reset CAMPOR register.
X'46': Set CAMPOR register.
X'47': Read CAMPOR register.

Table 8-19. CA MOSS Power-On-Reset Register

Bit	Function
0-3	Spare
4	CAs 1-8 nohold [8]
5	CAs 9-16 nohold [8]
6	CAs 1-8 MOSS power-ON-reset
7	CAs 9-16 MOSS power-ON-reset

Enable CA (ENCA) Registers

X'A4': Reset ENCA 1-8 register under mask.
X'A6': Set ENCA 1-8 register under mask.
X'A7': Read ENCA 1-8 register.

X'B4': Reset ENCA 9-16 register under mask.
X'B6': Set ENCA 9-16 register under mask.
X'B7': Read ENCA 9-16 register.

Table 8-20. ENCA Register 1-8

Bit	Function
0	CA 1 enable
1	CA 2 enable
2	CA 3 enable
3	CA 4 enable
4	CA 5 enable
5	CA 6 enable
6	CA 7 enable
7	CA 8 enable

Table 8-21. ENCA Register 9-16

Bit	Function
0	CA 9 enable
1	CA 10 enable
2	CA 11 enable
3	CA 12 enable
4	CA 13 enable
5	CA 14 enable
6	CA 15 enable
7	CA 16 enable

CA Reset (CARST) Registers

X'C4': Reset CARST 1-8 register under mask.
X'C6': Set CARST 1-8 register under mask.
X'C7': Read CARST 1-8 register.

X'D4': Reset CARST 9-16 register under mask.
X'D6': Set CARST 9-16 register under mask.
X'D7': Read CARST 9-16 register.

Table 8-22. CAs 1-8 Reset Registers

Bit	Function
0	CA 1 reset
1	CA 2 reset
2	CA 3 reset
3	CA 4 reset
4	CA 5 reset
5	CA 6 reset
6	CA 7 reset
7	CA 8 reset

Table 8-23. CAs 9-16 Reset Registers

Bit	Function
0	CA 9 reset
1	CA 10 reset
2	CA 11 reset
3	CA 12 reset
4	CA 13 reset
5	CA 14 reset
6	CA 15 reset
7	CA 16 reset

[8] The 'CA nohold' line coming from the MOSS is used to validate the 'CA MOSS POR', 'CA Reset', and 'CA Enable' lines. Bits 4 and 5 are reset by the 'reset adapter' command.

MOSS/SWL Adapter (SWAD) Registers

Adapter address: X'33'
Adapter reset: Command X'02'

Basic Status (BSTAT) Register

X'04': Reset under mask command
X'06': Set under mask command
X'07': Read command

Table 8-24. BSTAT Register

Bit	Function
0-2	Device address
3	Command reject (invalid PIO)
4	UC bus parity check
5	Equipment check
6	Enable interrupt on level 0
7	Interrupt level 0

Extended Basic Status (EBSTAT) Register

This register extends the basic-status register.

X'14': Reset under mask command
X'16': Set under mask command
X'17': Read command

Table 8-25. EBSTAT Register

Bit	Function
0	Overrun (EIRV error)
1	State counter parity check
2	Shift counter parity check
3	Ground fault detection
4	Time-of-day (TOD) interrupt
5	Interconnection check
6	Interconnection timeout
7	Interconnection parity check

Note: This register must be at zero before an operation with a switching device is issued. As this register contains error bits, any bit at 1 will cause the state counter to remain in the idle state.

Device Status Register

X'24': Reset under mask command
X'26': Set under mask command
X'27': Read command

Table 8-26. Device Status Register

Bit	Function
0-2	Switching device address
3	Phase 2: Switching device interconnection error
4	Phase 2: Switching device driver fault
5	Phase 2: Serial link parity check
6	Phase 2: Switching device invalid command
7	Phase 1/2 status

Disconnect Register

X'34': Reset under mask command
X'36': Set under mask command
X'37': Read command

Table 8-27. Disconnect Register

Bit	Function
0	SW/MOSS inoperative
1	Sense disconnect SWL-A
2	Sense disconnect SWL-B
3	Sense SW/MOSS inoperative
4	Internal clock check 1
5	Internal clock check 2
6	Disconnect SWL-A
7	Disconnect SWL-B

Confirm Disconnect Register

X'38': Reset under mask command
X'39': Set under mask command
X'3A': Read command

Table 8-28. Confirm Disconnect Register

Bit	Function
0	Request
1	Acknowledge
2-5	0000
6	Confirm disconnect A
7	Confirm disconnect B

MOSS Mode (MMOD) Status Register

The MMOD status register is used for service purposes.

X'3B': Read command
X'3C': Write command

Table 8-29. MMOD Status Register (SWAD)

Bit	Function
0-3	State counter bits (See “Bits 0 to 3 Decode.”)
4-7	Diagnostic bits (See “Bits 4 to 7 Decode.”)

Bits 0 to 3 Decode

State	Bits 0 1 2 3	Meaning
0	1 0 0 0	SWAD not busy with a switching device (idle state).
1	0 1 0 0	Start of operation, test acknowledge signal being OFF.
2	1 1 1 0	Set request signal for Phase-1 monitoring for acknowledge signal turned ON.
3	0 0 1 0	Phase-1 data transfer.
4	1 0 1 1	Request signal is OFF, monitoring for acknowledge signal turned OFF. Phase-1 data checking.
5	0 1 1 1	Set request signal for Phase-2 monitoring for acknowledge signal turned ON.
6	1 1 0 1	Phase-2 data transfer.
7	0 0 0 1	Request signal is OFF, monitoring for acknowledge signal turned OFF. Phase-2 data checking.
0	1 0 0 0	Operation ended without any abnormal condition.

Bits 4 to 7 Decode

Bits 4 5 6 7	Meaning
0 0 0 0	No force error
0 0 0 1	Force a parity error on the data sent at TD time on the UC bus during a read data register PIO operation, thus allowing to check the parity tester in the UC channel.
0 0 1 0	Force a parity error on the data received from the UC channel during a write data register PIO operation, thus allowing to check the parity tester and set B-status register, bit 4.
0 0 1 1	Force a parity error on the received data from SWL, thus allowing to check the parity tester and set EB-status register, bit 7.
0 1 0 0	Causes SWAD to set the two identification bits on the output lines 'SWAD module ID'.
0 1 0 1	Force an interconnection timeout by inhibiting the line 'Request' to raise during an operation with a SWL.
0 1 1 0	Force a parity error on the first byte of the transmitted message to the switching device.
0 1 1 1	Force a parity error on the second byte of the transmitted message (data) to the switching device, during an operation that writes data into a register.
1 0 0 0	Force a local wrap test.
1 0 0 1	Force a wrap test including a link.
1 0 1 0	Force a state counter parity error during an operation.
1 0 1 1	Force a shift pulse counter parity error during an operation with a switching device.
1 1 0 0	Force an error on the first frequency divider.
1 1 0 1	Force an error on the second frequency divider.
1 1 1 0	Force a parity error on the status received from SWL.
1 1 1 1	No force error.

Branch Trace

The branch trace facility allows the CCU hardware to record the non-sequential operations occurring in the flow of the CCU control program, into a predefined buffer.

Any time a branch actually occurs in the CCU, the 'come from' and the 'go to' addresses are stored into the buffer, as well as the corresponding 'come from' and 'go to' program level(s).

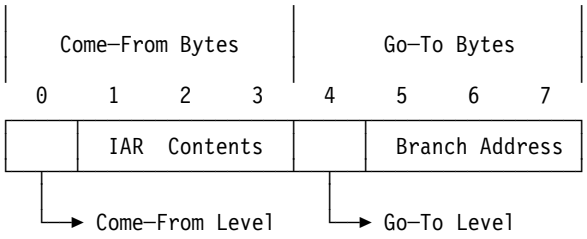
A non-sequential operation takes place when:

- A conditional or unconditional branch instruction is executed.
- An instruction modifies the IAR (reg 0 of the active program level).
- A new program level is entered, due either to a PCI issued by the CCU control program, or to an external interrupt caused by any adapter, or to an EXIT instruction.

When requested, the MOSS loads the branch trace registers with the upper and lower branch trace limits, and with the branch trace table definition (address in main storage and length). The branch trace registers are located in CCU local storage.

The MOSS then requests the CCU to record the 'come from' and 'go to' information of any actual branch in the branch trace buffer.

The branch trace information is stored in two contiguous storage positions as follows:



Branch Trace Buffer

The branch trace buffer allocation is made at Control Program generation time, by providing the buffer starting address and the buffer length as system generation parameters. When IPL is performed on the CCU, the buffer allocation values are passed over to MOSS.

The MOSS defines the branch trace buffer with MOSS Write LS (indirect operations). When the buffer is full, either the CCU is stopped and the MOSS is interrupted, or the MOSS only is interrupted.

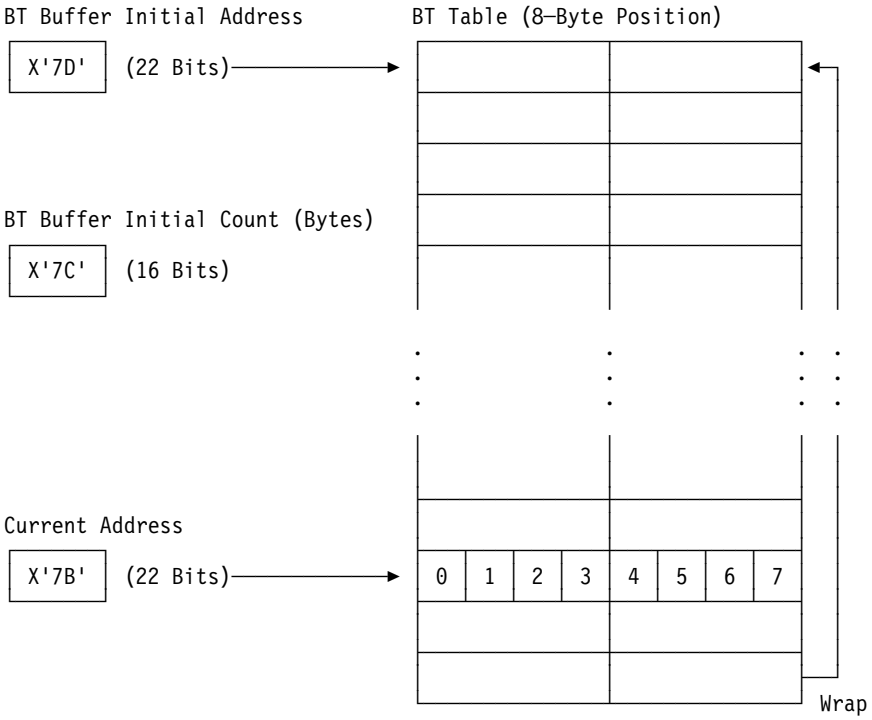


Figure 8-6. Branch Trace Buffer

If wrap is specified, 'branch trace buffer full' causes the branch trace count to be reinitialized, and the branch information to overlay the start of the branch trace buffer.

Under certain circumstances, the branch trace buffer may contain extra records showing the entry and the exit of the CCU through some program level, without instruction execution at that level.

Address Compare

The address compare (AC) function allows the comparison of up to two main storage addresses (addresses used during instruction fetch, data read or write, or cycle steal operation) with the address(es) to be compared (stored in AC registers 1 and 2). Via the MOSS, the operator can request one single, two single, or one double address compare. The type of address that is compared is defined in the AC control register.

Table 8-30. Address Compare Control Register (X'03')

Bit	Function
0	First AC on cycle steal
1	First AC instruction fetch
2	First AC on storage read
3	First AC on storage write
4	Second AC on cycle steal
5	Second AC instruction fetch
6	Second AC on storage read
7	Second AC on storage write

Bits 0 through 3 control the first address compare; the compare address is stored in AC register 1.
Bits 4 through 7 control the second address compare; the compare address is stored in AC register 2.
The possible actions taken by the CCU when addresses compare can be:

- CCU stop: CP is stopped.
- CCU level 1 interrupt: a CCU level 1 interrupt request is raised.
- MOSS signal: a level 4 interrupt request is raised to MOSS:

Single-Address Compare

The main storage address is compared with the contents of AC register 1, depending on bits 0 through 3 of the AC control register.

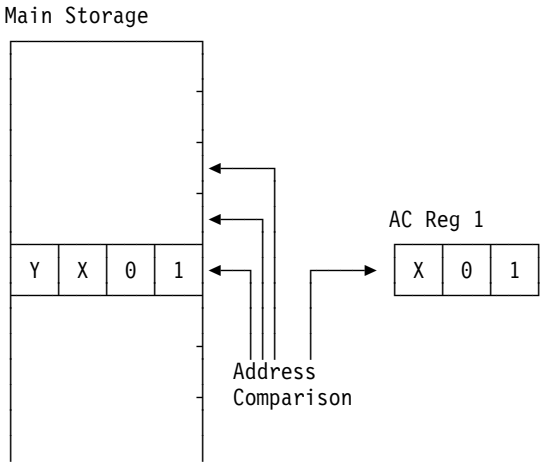


Figure 8-7. Single-Address Compare

Two Single-Address Compares

The main storage address is compared with the contents of AC registers 1 and 2, depending on bits 0 through 7 of the AC control register.

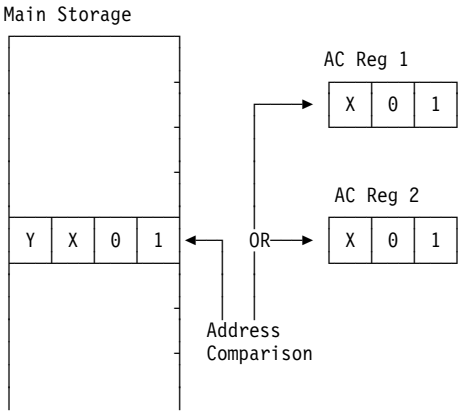


Figure 8-8. Two Single-Address Compares

Double-Address Compare

Two storage addresses must match the contents of AC registers 1 and 2 to cause a successful compare.

1. The main storage address used during instruction fetch must compare equal with the contents of AC register 1.
2. If the first compare is successful, and the instruction is 'load/ store', the storage address used during instruction execution is compared with the contents of AC register 2.

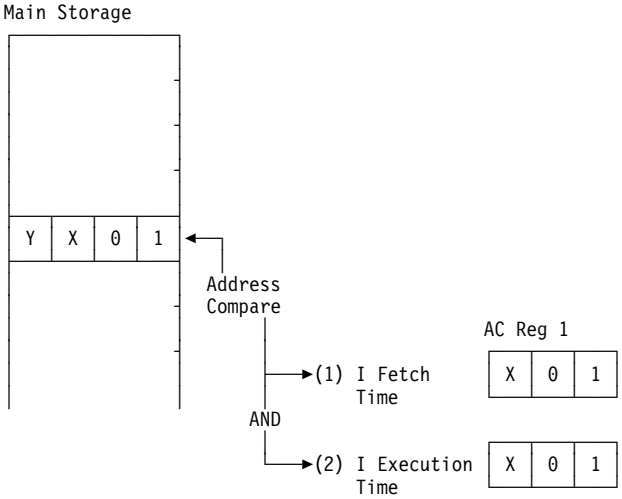


Figure 8-9. Double-Address Compare

Mode Control Register A (X'10')

The action to be taken on a successful address compare is defined by this register. It is not accessible to the CCU.

Table 8-31. Mode Control Register A (X'10')

Bit	Function
0	AC compare type bit 1
1	AC compare type bit 2
2	Branch trace active
3	Wrap trace
4	Stop branch trace on AC
5	CCU stop on AC or BT full
6	CCU L1 on AC
7	Low level interrupt to MOSS on AC or branch trace full

Branch Trace Level Control Register (X'04')

The MOSS sets bits in this register according to the level(s) to be traced. This register is not accessible to the CCU.

Table 8-32. Branch Trace Level Control Register (X'04')

Bit	Function
0	(Not used)
1	Trace level 1
2	Trace level 2
3	Trace level 3
4	Trace level 4
5	Trace level 5
6	(Not used)
7	(Not used)

CCU/MOSS Status Register A (CMSA: X'11')

The Control Program sets some of its latches with Out X'70', Out X'79', other bits are set by the hardware.

Any bit on, except bit 3, causes a high-level interrupt to the MOSS. The MOSS reads or resets this register using a MOSS read X'11' command.

Table 8-33. CCU/MOSS Status Register A (X'11')

Bit	Function
0	IOC error during MIOH
1	Program IPL request (out X'79' bit 0.2)
2	Channel IPL request
3	CCU hardstop (no HLIR)
4	CCU Out X'70' (data: not applicable)
5	Address exception check
6	CCU hardware check
7	MOSS operation check

CCU/MOSS Status Register B (CMSB: X'06')

The CCU sets this register with Out X'71', X'72', or X'76'. Any bit on, except bit 4, causes a low-level interrupt to the MOSS.

Table 8-34. CCU/MOSS Status Register B (X'06')

Bit	Function
0	(Not used)
1	(Not used)
2	CCU program request
3	CCU program response
4	CCU busy (no LLIR)
5	(Not used)
6	Program display 1 (CCU Out X'71')
7	Program display 2 (CCU Out X'72')

CCU/MOSS Status Register C (CMSC: X'07')

This register holds the branch trace/address compare results. It is read and reset by the MOSS via In X'07'.

Table 8-35. CCU/MOSS Status Register C (X'07')

Bit	Function
0	Branch trace buffer full
1	Successful address compare
2	CCU stop because BT full
3	CCU stop because successful AC
4	AC on Address 1 register
5	AC on Address 2 register
6	Program stop
7	(Not used)

Mailbox Description

The NCP/PEP and the MOSS communicate through CCU storage areas called mailboxes. These mailboxes are located in the 32-kB area reserved for MOSS use, at the top of CCU main storage (see Table 8-36).

Table 8-36. Mailbox Addressing in CCU Storage

CCU Storage (32K Top Area)	Address in 4-MB Storage	Address in 8-MB Storage	Address in 16-MB Storage
Spare (192 bytes)	X'3FFFFF' X'3FFF40'	X'7FFFFF' X'7FFF40'	X'FFFFFF' X'FFFF40'
NCP Out Mailboxes (32 bytes)	X'3FFF3F' X'3FFF20'	X'7FFF3F' X'7FFF20'	X'FFFF3F' X'FFFF20'
NCP In Mailboxes (32 bytes)	X'3FFF1F' X'3FFF00'	X'7FFF1F' X'7FFF00'	X'FFFF1F' X'FFFF00'
Unused	X'3FFEFF' X'3FA400'	X'7FFEFF' X'7FA400'	X'FFFEFF' X'FFA400'
MOSS to Line Adapter Data Area (8704 bytes)	X'3FA3FF' X'3F8200'	X'7FA3FF' X'7F8200'	X'FFA3FF' X'FF8200'
Line Adapter Mailboxes (512 bytes)	X'3F81FF' X'3F8000'	X'7F81FF' X'7F8000'	X'FF81FF' X'FF8000'
Top of Non-Reserved Storage	X'3F7FFF'	X'7F7FFF'	X'FF7FFF'

For a detailed description of the mailbox contents, see *3745 Principles of Operation,* GA33-0102.

Exchange Timeouts

The requestor fills in his mailbox and posts an interrupt to the receiver. The receiver grants the interrupt, decodes the mailbox contents, posts a status in the mailbox, and interrupts the requestor. Throughout this time, the mailbox is busy with the requestor. A timer is used to provide a protection against requests that are not answered.

On the NCP side, if a timeout occurs, the MOSS is considered down and an alert is sent to the host.

On the MOSS side, if a timeout occurs, a return code is passed to the requesting application to signal this situation. In this case, the NCP/PEP is probably down and operator intervention may be required.

CCU to MOSS Communication (Out Mailbox)

The out mailbox is used to pass requests from the NCP/PEP to the MOSS and for the MOSS to post the status response.

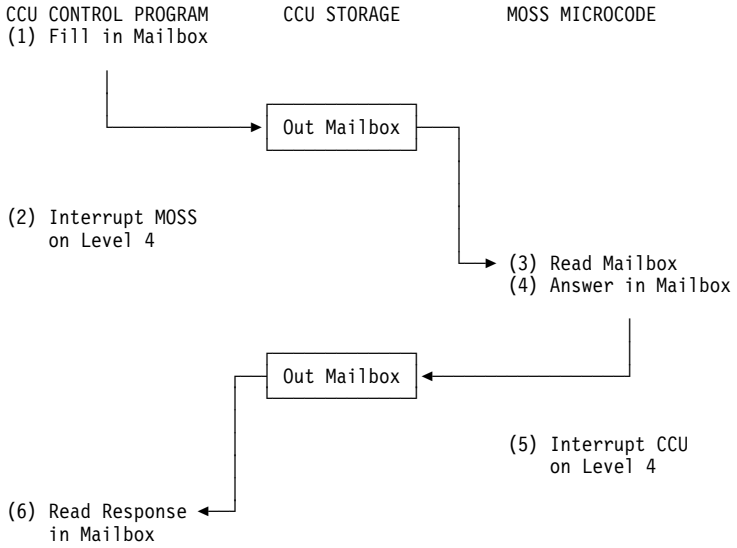


Figure 8-10. Out Mailbox Exchange Procedure

MOSS-to-CCU Communication (In Mailbox)

The in mailbox is used to pass MOSS requests to the NCP/PEP and for the NCP/PEP to post the status response.

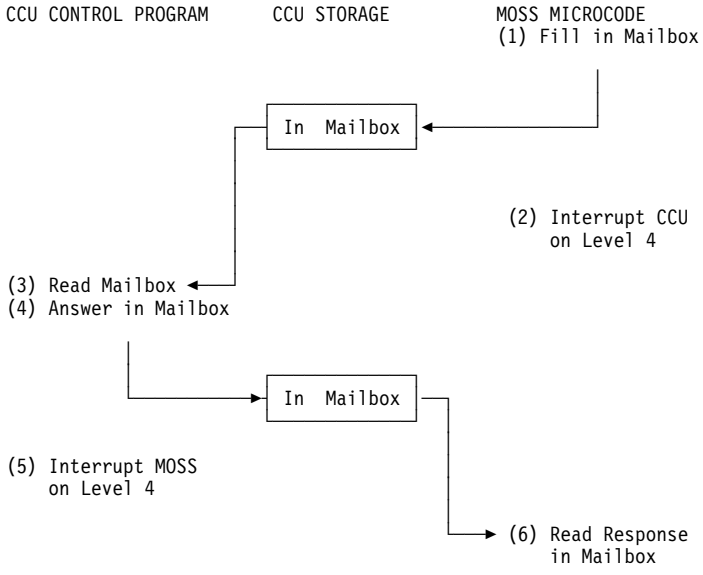


Figure 8-11. In Mailbox Exchange Procedure

Mailbox Commands

The following table (Table 8-37) shows the commands sent by the MOSS to the CCU control program (IN mailboxes), and in which functions they are involved.

Table 8-37. NCP Mailbox In Commands

Function	Hex	In Command
CLDP	C1	Line adapter IML complete
	C2	Roll in complete
	C3	IPL from disk complete
	C4	Control information response
	C5	Dump records saved
Initialization	A3	CP parameter saved
	A4	CDS information available
	B2	Reissue port swap
Normal	86	Transfer PIU: • Sollicited response • Unsollicited reply • Dump storage response
	89	Wrap test request
	8A	Stop wrap test
	8C	Connect line adapter
	8D	Reissue a 3746-900 port swap
	8E	Request buffer
	8F	Free buffer
	90	MOSS offline
	91	MOSS online
	92	Port swapped
Reconfiguration	81	Fallback requested
	82	Switchback requested
	83	Fallback portswap
	84	Update CDS 01: Delete ports, 02: Add ports 03: Delete line, 04: Add line 05: Change CDS header 06: Insert CA, 07: Delete CA, 08: Change CA
	85	Switchback complete
CA Services	93	Disconnect CA
	94	Connect CA 01: Initialize 02: Cancel CACM
	95	AS/SC chain update 01: Remove CA from AS chain 02: Remove CA from CS chain 03: Insert CA into AS chain 04: Insert CA into CS chain
	96	Install CA 01: Start INSTALL procedure (CACM) 02: Cancel INSTALL procedure (CACM)

The following table (Table 8-38) shows the commands sent by the CCU control program to the MOSS (OUT mailboxes), and in which functions they are involved.

Table 8-38. NCP Mailbox Out Commands

Function	Hex	Out Command
CLDP	41	CP loaded
	42	Roll in saved storage
	43	IPL from disk
	44	Control information
	45	Dump records built
Initialization	23	CP parameter
	24	Request hardware CDS
	25	CP initialization complete
	26	Request hardware CDS (swap)
	27	Request reissue port swap
Normal	01	Fallback complete
	03	Fallback request portswap
	06	Transfer PIU: The PIUs processed by MOSS are listed in Table 8-39.
	07	NCP/PEP BER transfer
	08	Buffers now available
	09	Wrap test results
	0C	Time/date valid
	0D	Request a 3746-900 port swap

Request Unit List

Request unit (RU) sent by SSCP and processed by the MOSS.

Table 8-39. Request Unit List

Hex	Meaning
010331	Display storage, answered by : 010334 record storage
410304	REQMS, answered by : 010334 RECFMS REQMS = Request of maintenance statistics RECFMS= Record formatted of maintenance statistics
010203	IPL Init (see note)
010204	IPL Text (see note)
010205	IPL Final (see note)
010206	Dump Init (see note)

Note: Answered by a positive response or a sense code when negative response. Refer to the Sense Code Appendix in the AOG.

MOSS/Line Adapter Communication

Here is the list of the commands the MOSS sends to a line adapter:

Table 8-40. MOSS to Line Adapter Commands

Command in Hex	Command Description	
02	Dump registers [9]	
06	Address compare reset	
08	Snapshot trace stop	
09	Initialization [9]	No data in mailbox with
0B	Line adapter stop	these commands
0C	Line adapter go	
0E	Checkpoint trace ON	
0F	Checkpoint trace OFF	
41	IPL [9]	
42	Dump control store [9]	
43	Display immediate	
44	Alter immediate	
63	Display delayed	Commands that use mailbox
64	Alter delayed	
85	Address compare set [10]	
87	Snapshot trace start [10]	

Communications between the MOSS and a line adapter use the dedicated line adapter mailbox area in the CCU storage. In all circumstances, the line adapters are subordinate to the MOSS and therefore cannot initiate any unexpected action. The line adapter communication area contains a number of parameter status areas (PSAs), one for each line adapter mailbox.

Each PSA contains entries for the command, the response, the data pointer, and the count.

1. The MOSS initializes the PSA.
2. The MOSS forces (through the MIOC) a PIO to the line adapter processor that indicates a MOSS operation.
3. Information is given in the PIO (R1, R2) or read from the PSA via cycle steal by the line adapter.
4. The line adapter stores the requested data in the communication area at the appropriate address via cycle steal.
5. The line adapter sets its PSA fields and interrupts the MOSS at level 4. An additional line in the IOC bus cable is used for this purpose.

[9] Command initiated by ROS.

[10] Command '85' or '87' may be pending on a line adapter together with command '63' or '64'.

LSSD Operation

Level sensitive scan design (LSSD) operations are powerful diagnostic tools used especially during IML, or when running CCU diagnostics.

In LSSD operations, the MOSS can verify or change the status of any discrete CCU latch. Such operations can be performed after any CCU cycle, by stopping the CCU clock.

Data Flow

Figure 8-12 on page 8-38 is a simplified representation of the data flow. Normally, the complete CCU can be represented with 12 strings each having an average of 100 SRL statuses.

The 'SRL out' lines present their status to the following combinational logic at clock pulse B. The resulting combinational logic values set the 'SRL In' lines at the next clock pulse C.

LSSD Testing Circuit

For testing purposes, the above 'SRL Out' are connected to 'SRL In' lines in a sequential string as follows (Figure 8-13 on page 8-38). The 'In' and 'Out' lines go to their combinational logics. 'Scan In' is the string input; 'Scan Out' is the string output.

With LSSD operations the MOSS can:

1. Read the CCU SRLs for diagnostic purposes ('scan out' to MOSS scan register).
2. Set/reset the CCU SRLs to a preset value for initial CCU reset (scan register to 'scan in').

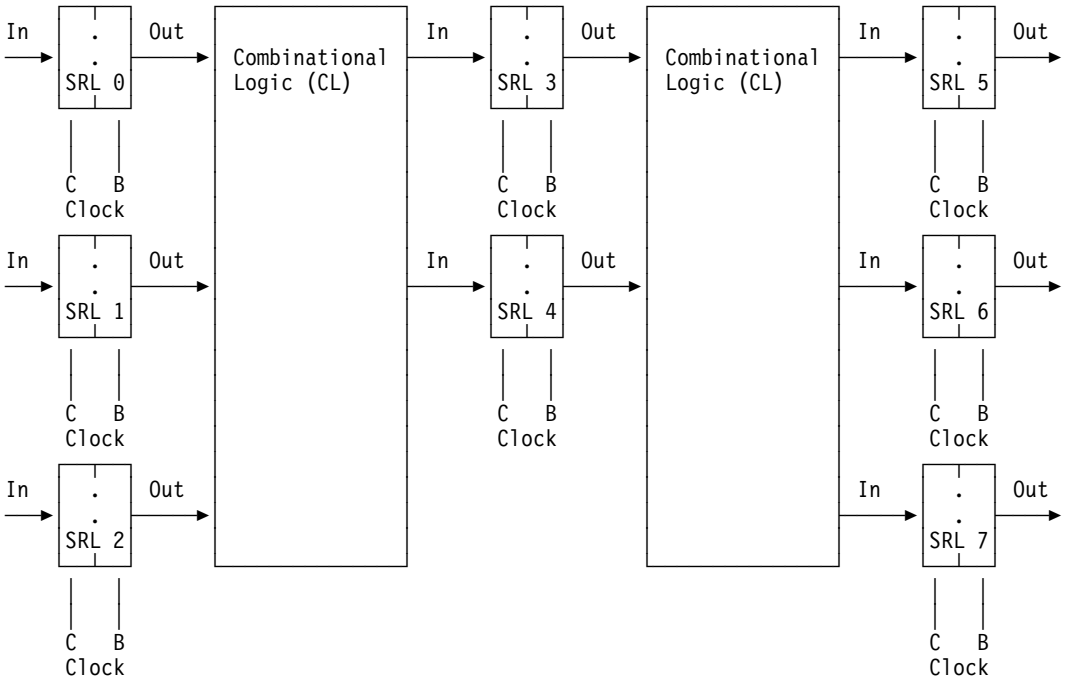


Figure 8-12. Simplified Data Flow

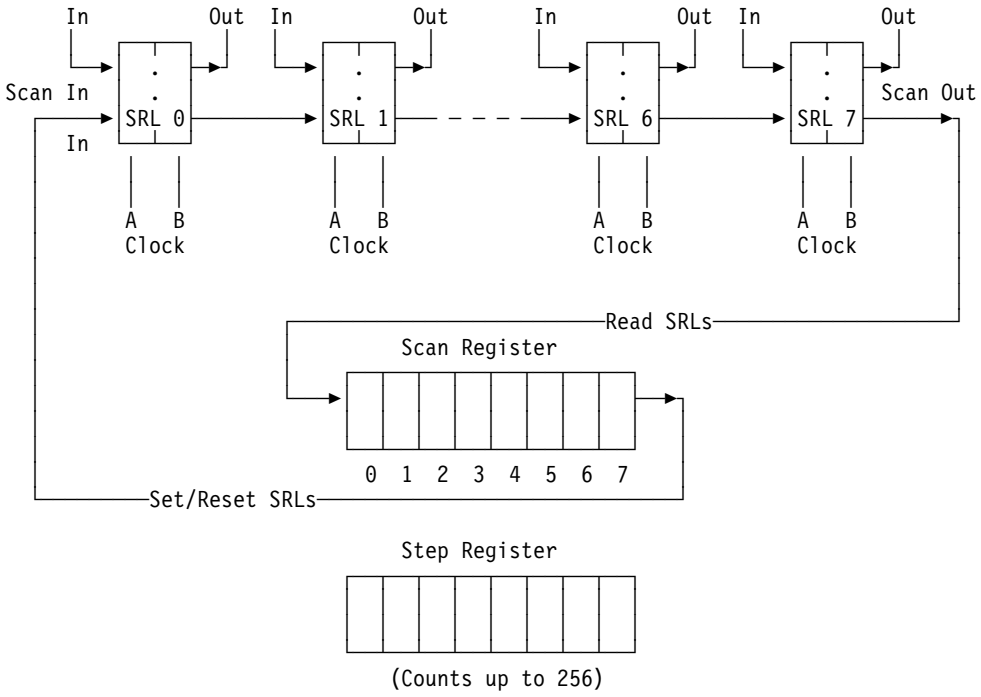


Figure 8-13. LSSD Testing Circuit

MOSS/Disk Drive Interaction

The hard/flexible disk drives are described in Chapter 9 of this manual.

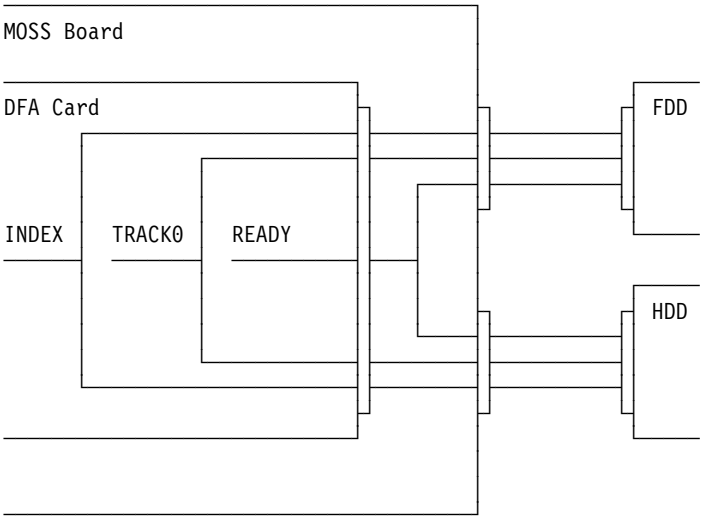
Disk Commands

The MOSS processor controls the disk file adapter (DFA) and its attached drives via program or channel I/O commands on the MOSS external UC bus. These commands allow the MOSS to:

1. Start or stop the flexible and hard disk drives.

   Notes:

   - DC voltages to disk drives are stopped when there is no activity on disks for 15 minutes (see "Disk and Diskette Drive On/Off Control" in Chapter 10 for details).
   - There are three lines READY, INDEX, and TRACK0 which are common to both the HHD and the FDD. READY line is doted on the MOSS board; INDEX and TRACK0 are doted on the DFA card.



2. Set or sense the file adapter registers.
3. Seek head carriage.
4. Engage the heads (position the heads close to the disk/diskette surface).
5. Read data from the disk/diskette.
6. Write data to the disk/diskette.
7. Read back the data for checking purposes.

The DFA rejects commands that are invalid, or have a bad parity. A command that temporarily cannot be serviced by the disk/diskette drive is considered invalid.

The command is not retried. It causes a machine check/program check end status indication.

Read/Write Operations

Read or write operations are initiated via PIO commands. Data is exchanged directly with the MOSS storage through the DFA. (Halfword cycle stealing operation.)

MOSS/Operator Console Connections

On 3745 Models 210-610 , the operator consoles can be attached to the processor via the MCA card. The MOSS can control only one console at a time.

Chapter 9 of this manual gives details on operator consoles themselves, and the *3745 Service Functions*, SY33-2055, describes how the service functions are used from the 3745 console.

For console connections and operations on
3745 Models 21A-61A, refer to *3746 Model 900 Installation Guide* and *Service Processor Installation and Maintenance* manuals.

Remote Support Facilities (RSF)

On 3745 Models 210-610, the MOSS-to-RETAIN connection is made with a BSC protocol at 1200/2400 bps (V.22 Bis or V.23 CCITT interface, depending on the country), via a duplex external modem with the auto-answer feature.

The IBM RSF Modem operating characteristics are as follows:

- Connection over a switched line
- Duplex transmission
- Synchronous transmission
- Auto-answer feature
- Transmission speed: 1200/2400 bps
- Clocking by the modem clock
- DSR control by the modem

For remote support facilities on 3745 Models 21A-61A, refer to *Service Processor Installation and Maintenance* manual.

Chapter 9. Control Panel, Operator Consoles, Disk/Diskette Drives

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3745 Control Panel

Overview

For 3746-900 control panel, refer to:

- The 3746 Model 900 HMR (online document) for detailled information.
- The MIP for details on the control panel functions.

The 3745 control panel consists of:

- A ten-digit alphanumeric display
- A key pad with seven keys
- A unit emergency power Off switch
- An overlay corresponding to national language requirements
- A power On lamp.

See “Control Panel Layout” on page 9-3 for details.

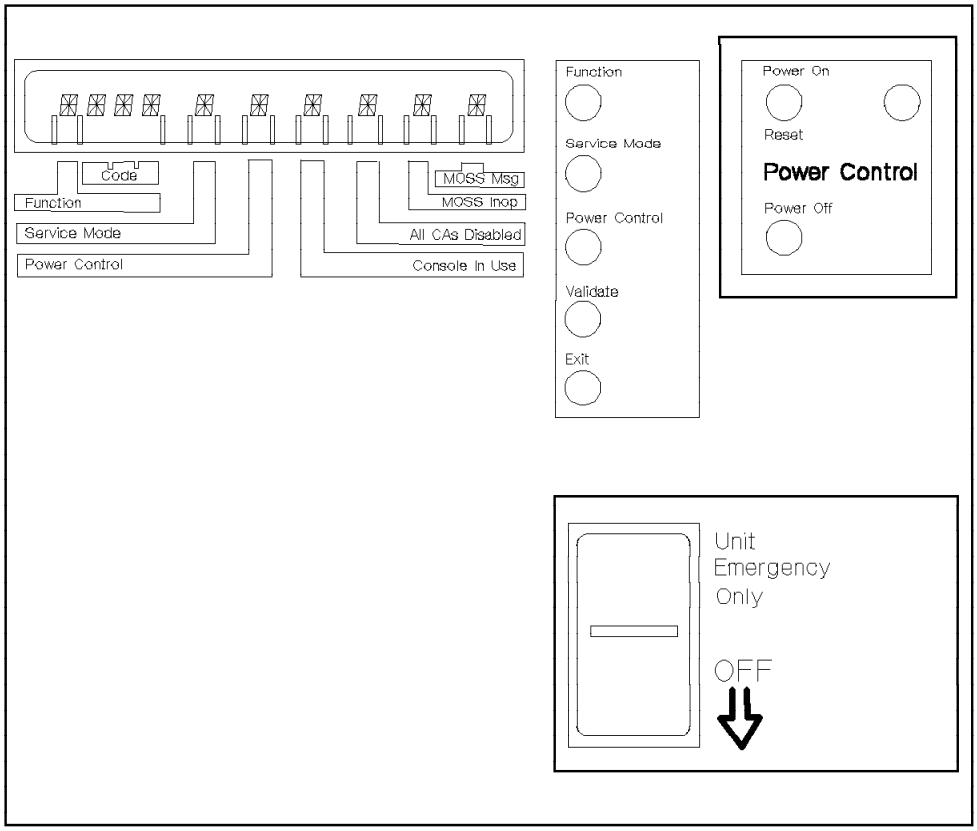
The control panel carries keys and indicators required for:

- Controlling the power system
- Activating MOSS functions, control panel test, power bus test
- Hexa display code to operator.

The 3745 control panel stays powered ON when the 3745 is powered OFF. This allows information on power control and service to be displayed.

The 'Function', 'Service' and 'Power control' keys allow the operator to scroll the different options. The option is performed by pressing the 'Validate' key, or cancelled by pressing the 'Exit' key. Refer to the *MIP* for more details on the control panel functions.

Control Panel Layout



(*) For code definitions, refer to Appendix A in the *MIP*.

Figure 9-1. Control Panel

Control Panel Reference Card

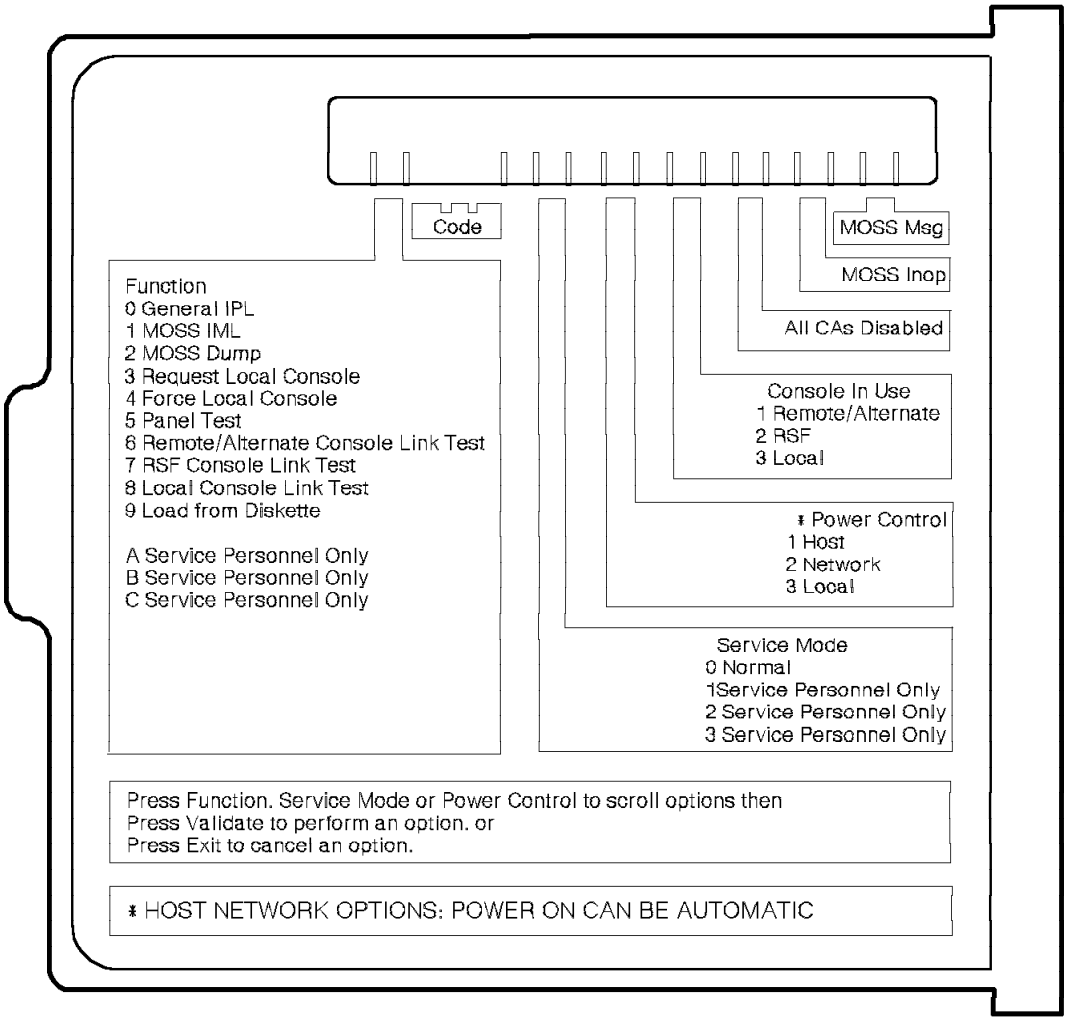


Figure 9-2. Control Panel Reference Card

Control Panel Connection

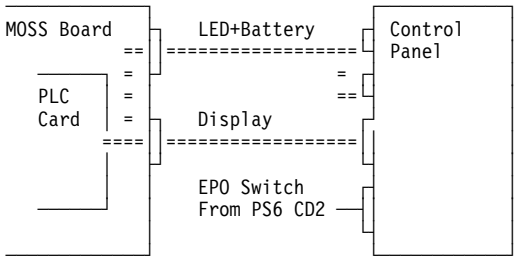
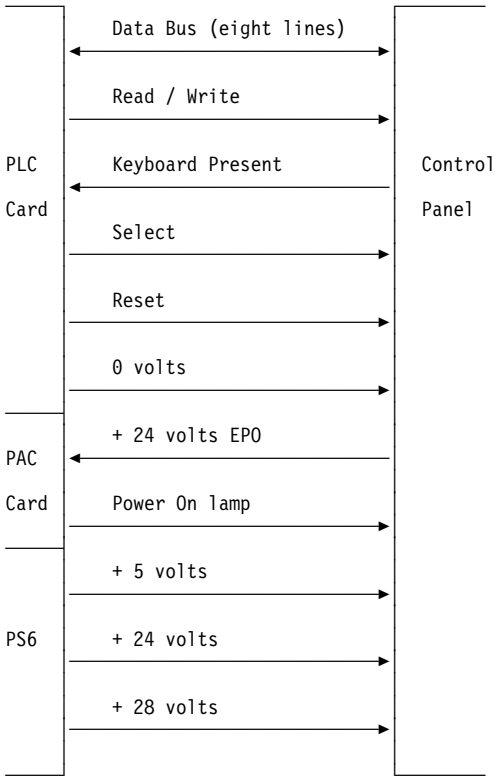


Figure 9-3. Control Panel Connection

For component locations on MOSS board and control panel, see YZ pages.



Control Panel Operation

For control panel operation and tests, refer to *MIP Chapter 1.*

Operator Consoles for Models 210-610

Highlights

The 3745 offers three different console interfaces. Activation of these attachments are under MOSS control via the MCA card. Only one of these attachments may be active at a time.

The consoles whose characteristics are listed below are used either by the customer or by IBM service personnel. See “Console Summary” on page 1-8.

For more details on console configuration, see *Console Setup Guide* SA33-0158.

Local Console and Alternate Console

The local console, which is mandatory, and the alternate console operate with interface CCITT V.24 in duplex start-stop mode at 2400 bps. The local or alternate console can be an:

- IBM 315x Model 110, 160, 310, 360, 410 or 460 Display Station in native mode or in IBM 3101 emulation mode.
- IBM 316x Display Station Model 11,12, 21 or 22 in IBM 3101 emulation mode.
- IBM PS/2* able to run under OS/2* extended edition with Communication Manager emulating the 3101.
- IBM 3727 Display Station (keyboard overlay provided in shipping group).
- Any equipment providing equivalent functions operating in IBM 3101 emulation mode.

For details about the consoles to be used on the 3745, refer to the *Console Setup Guide*.

Remote Console

Operates in duplex start-stop mode at 1200 bps. The remote console can be an :

- IBM 315x (in the USA and Canada only, and only if an IBM 5841, 5842, or 5853 modem for USA or 5853 modem for Canada is used at the 3745 end) in native mode or in IBM 3101 emulation mode.
- IBM 316x Display Station Model 11,12, 21 or 22 in IBM 3101 emulation mode.
- IBM PC in IBM 3101 emulation mode.
- IBM PS/2 able to run under OS/2 extended edition with Communication Manager emulating the 3101.
- Any equivalent equipment emulating the IBM 3101 and having an interface CCITT V.24, (EIA 232D).

For details about the consoles to be used on the 3745, refer to the *Console Setup Guide*.

Console Sharing Via IBM 7427

The IBM 7427 Console Switching Unit can be used with the 3745 for 31XX and 3727 consoles.

A maximum of four communication controllers can share a local console.
A maximum of six communication controllers can share an alternate console.

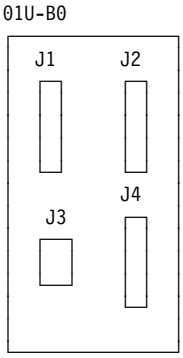
Remote Support Facility (RSF)

Attached to the 3745 over the public switched network via a modem.

For details, see 8-40.

Consoles and Customer Power Control Tail Gate

For 3745 Models 210-610

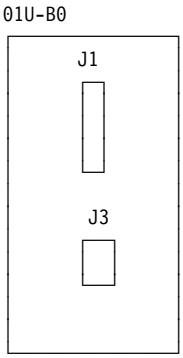


- The J1 connector is for the remote or alternate console.
- The J2 connector is for the RSF console.
- The J3 connector is for the customer and provides a normal-closed and a normal-open contact when the power is OFF, and reverse their state when the power is ON.

  Electrical Characteristic:
  30 volts AC or 42.4 volts peak or DC at 20 to 500 mA.

  For details, see page YZ543.
- The J4 connector is for the local console.

For 3745 Models 21A-61A



- The J1 connector is for service processor connection through the LAN.
- The J3 connector is for the customer and provides a normal-open contact when the power is OFF, and reverse its state when the power is ON.

  Electrical Characteristic:
  30 volts AC or 42.4 volts peak or DC at 20 to 500 mA.

  For details, see page YZ543.

Console Connection

For console connection, cable wiring, cable length, and cable part number, see *IBM External Cable References* manual, SY33-2075.

3161 Console 3727 Console Key Conversion

3161	**3727**
BREAK	ATTN
PF1	SELN AREA
PF2	CCU FNCTN
PF3	MSG
PF4	PF1
PF5	PF2
PF6	PF3
PF7	PF4
PF8	PF5

Adhesive keytop labels part number = 03F7773

Console Setup and Maintenance

See appropriate console documentation.

Operator Consoles and Service Processor for Models 21A-61A

To operate and maintain the 3745 21A-61A and 3746-900 a new operator console is required. The 3745/3746-900 operator console is a PS/2 based console fully configured and loaded with microcode called MOSS extended (MOSS-E). The operator console serves as service processor to the 3746-900 and the 3745 and must always powered On. The console can operate up to four 3745 but with two of them equipped with a 3746-900.

For more details on operator console configurations and installation refer to the "Operator and Service Processor" chapter in the *3746 Model 900 Hardware Maintenance Reference*, online documentation and the *3746 Model 900 Installation Guide*, SY33-2088.

Disk/Diskette Drive

Hard Disk Drive (HDD)

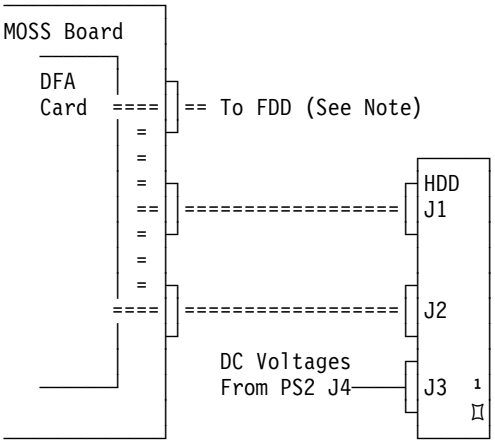
Description

The 3745 hard disk drive has the following characteristics:

- 5.25 in.
- 5 disks
- 7 heads on 3745 models 210-610. 8 heads on 3745 models 21A-61A.
- 733 tracks
- 17 sectors/track
- 512 bytes/sectors
- The maximum readiness time after power ON is about 25 s
- The average access (seek) time is about 75 ms.

If the disk drive has not been used within 15 minutes, it is powered OFF by the MOSS.
The heads are automatically parked in the landing zone when the power is Off.

The hard disk drive is a FRU.



1 = Jumper for drive select, set on position 1.

Note: Three Dot ORed lines (INDEX, READY, and TRACK 0) are common to the HDD and the FDD.

Figure 9-4. HDD Connection

For component locations, see YZ pages.
For connector pin assignment, see page YZ542.

Removal and Replacement Procedures

See *MIP*, and *Service Functions*, for HDD initialization.

Part Number
See *3745 Parts Catalog*, S135-2010.

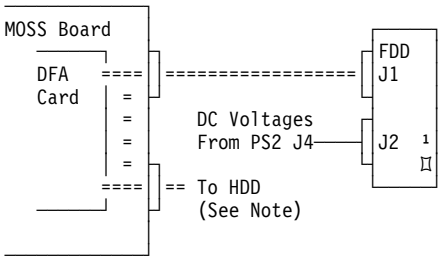
Diskette Drive (FDD)

Description
The 3745 diskette drive has the following characteristics:

- 5.25 in.
- 2 heads
- 154 tracks
- 15 sectors/track
- 512 bytes/sector
- The average readiness time after power ON is about 1 s
- The average access (seek) time is about 92 ms.

If the diskette drive has not been used within 15 minutes, it is powered OFF by the MOSS.

The diskette drive is a FRU with its own power supply.



Note: Three Dot ORed lines (INDEX, READY, and TRACK 0) are common to the HDD and the FDD.

Figure 9-5. FDD Connection

For component locations, see YZ pages.

For connector pin assignment, see page YZ541.

Removal and Replacement Procedure
See *MIP* Chapter 5.

Part Number
See *Parts Catalog*.

Chapter 10. 3745 Power System

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The Power System in 3745 Data Flow

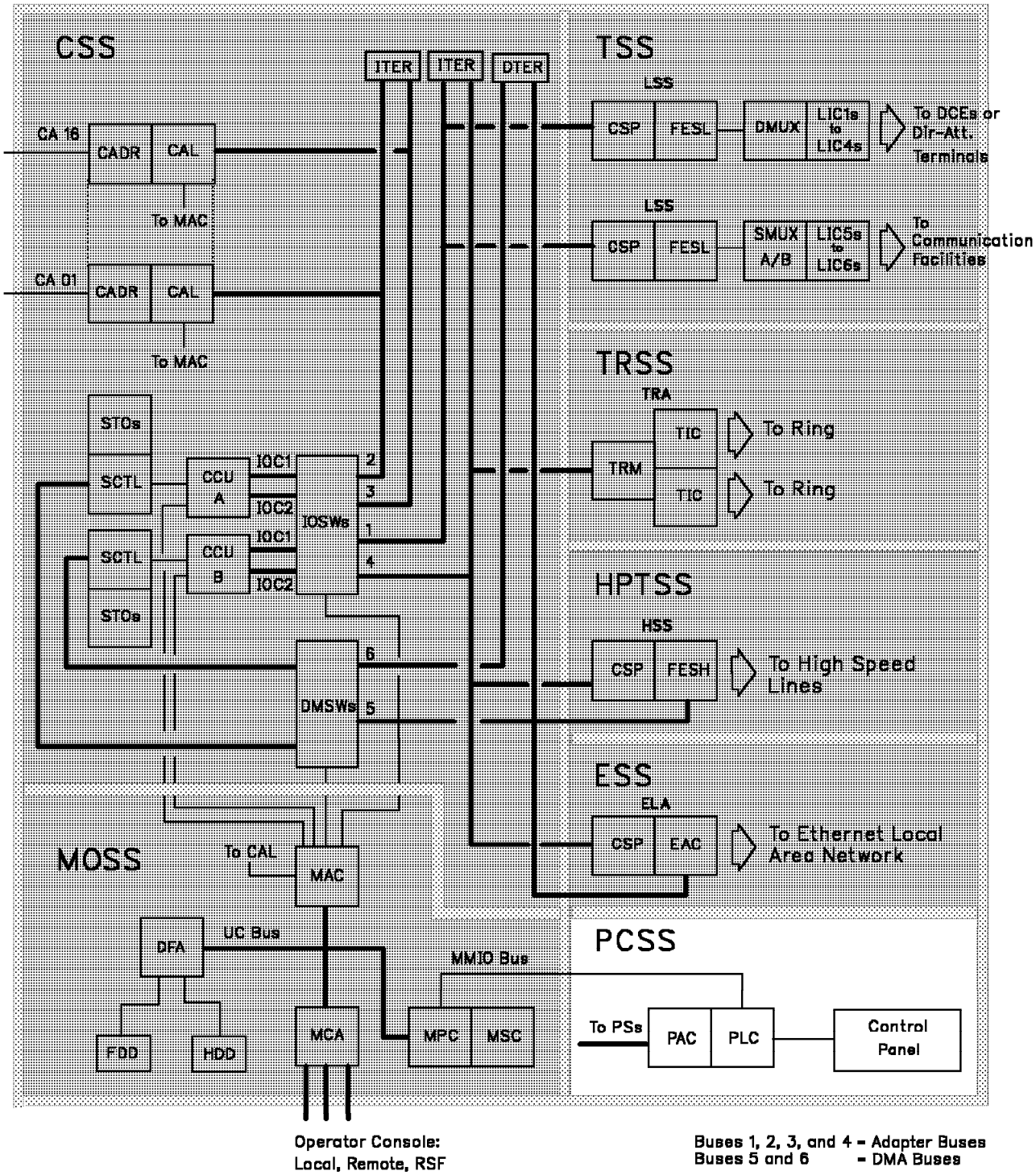


Figure 10-1. The Power System in 3745 Data Flow. For models 21A-61A, DMA and IOC buses are connected to the CBC in the 3746-900. The MCA card is replaced by the MLA card which interfaces to the MPC card through the MMIO bus. This MLA card links the MOSS to the Service Processor through a LAN.

Introduction

From the primary power box, the 3745 power system provides:

- AC voltages to the power control.
- AC voltages to PSs.
- AC and DC voltages to fans.
- AC voltages to frame 01 convenient outlets.

See “Primary Power Box AC Distribution” on page 10-7 for details.

A power control subsystem has in charge all the functions of the power system (powering ON/OFF in local, host, or remote mode, reporting power faults and fan faults to MOSS, power diagnostic).
See “Power Control Subsystem” on page 10-39 for details.

AC Voltages Input

The power system can operate either in:

- Delta 3-wire lines, or
- Wye 4-wire lines.

For changing from Delta to Wye connection, an MES is necessary.

AC Voltage Limits

The power system can operate within one of the following AC input phase-to-phase line voltages:

Table 10-1. AC Voltage Limits

Voltage	**Delta**	**Wye(1)**
Nominal	200 to 240	380 to 415
Minimum	180	333
Maximum	259	448

(1) Phase-to-neutral voltage must be within the 180 to 259 volts range.

WARNING: Voltage adjustment must be done on the:

- **Primary power box, see YZ page 561,**
- **Power supply type 6, see YZ page 576, and**
- **Power supply type 8, see YZ page 561/578.**

Frequency

The 3745 can operate at one of the following frequencies:

- 50 Hz +/- 1 Hz
- 60 Hz +/- 1 Hz.

Safety Statement

Input output cables must comply with the following safety statement:

For AC Voltage Input

Hazardous voltage circuits (with AC voltages input) comply with IEC 950 - Class I, reinforced insulation.

For DC Voltage Outputs

- LIC type 5 or 6 are TNV Circuits (Telecommunication Network Voltage)

Or

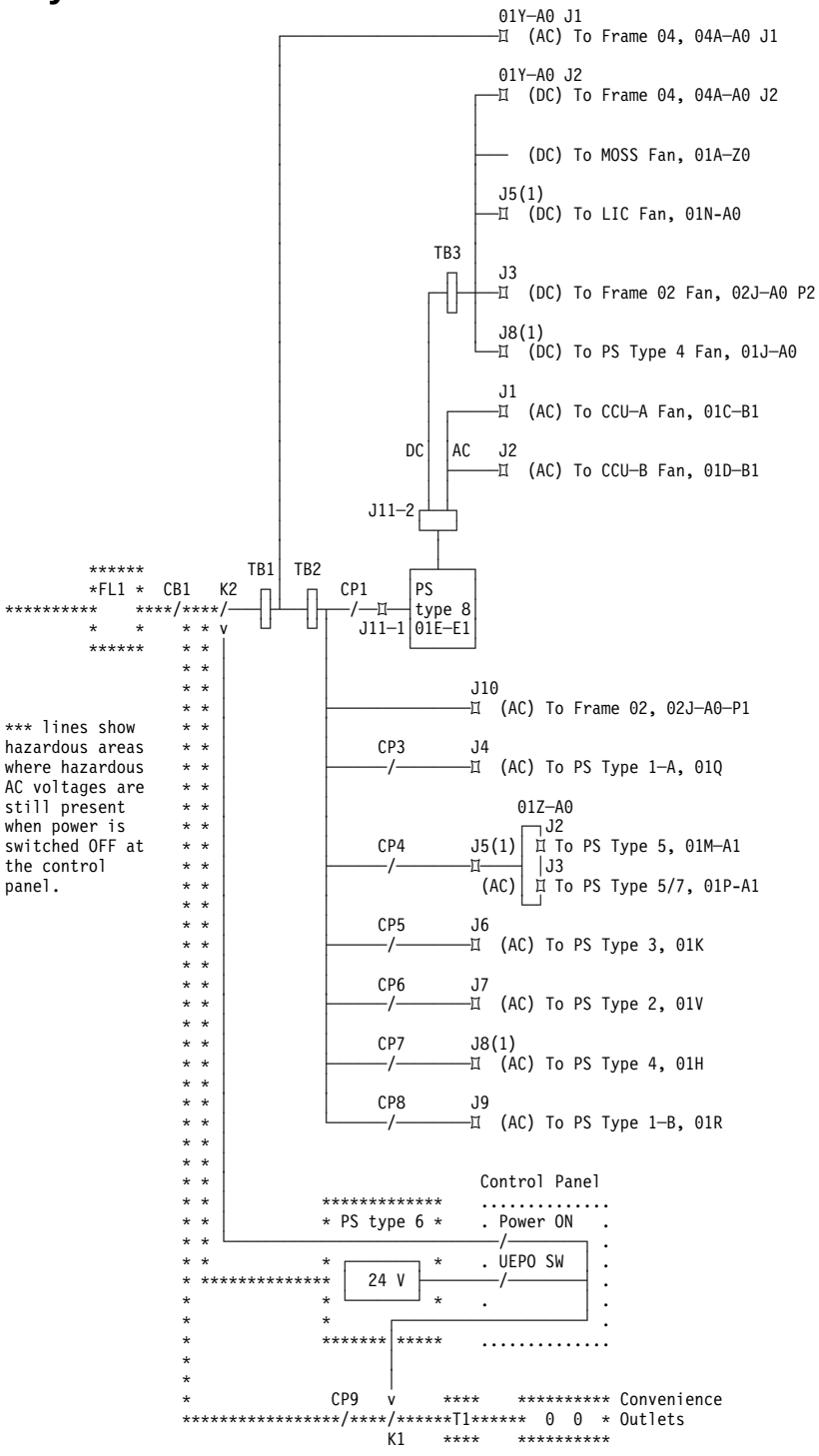
- All other are SELV Circuits (Safety Extra Low Voltage)

Power Supply Identification

Table 10-2. Power Supply Identification

ID Number Decimal	ID Number Hexa (from BER)	PS Type	Frame	Location	Attached Component	For details, go to:
01	01	2	01	01V	MOSS Board	page 10-15
02	02	1/1B	01	01Q	CCU-A	page 10-10 or page 10-13
03	03	1/1B	01	01R	CCU-B	page 10-10 or page 10-13
04	04	3	01	01K A1	CAs 1-2	page 10-18
05	05	3	01	01K B1	CAs 3-4	page 10-18
06	06	3	01	01K C1	CAs 5-6	page 10-18
07	07	3	01	01K D1	CAs 7-8	page 10-18
08	08	4	01	01H A1	LAs 1-2	page 10-21
09	09	4	01	01H B1	LAs 3-4	page 10-21
10	0A	4	01	01H C1	LAs 5-6	page 10-21
11	0B	4	01	01H D1	LAs 7-8	page 10-21
12	0C	5	01	01P A1	Lines 000-063	page 10-26
13	0D	5/7	01	01M A1	Lines 064-127	page 10-26 or 10-33
14	0E	3	02	02D A1	CAs 09-10	page 10-18
15	0F	3	02	02D B1	CAs 11-12	page 10-18
16	10	3	02	02D C1	CAs 13-14	page 10-18
17	11	3	02	02D D1	CAs 15-16	page 10-18
18	12	4	02	02B A1	LAs 09-10	page 10-21
19	13	4	02	02B B1	LAs 11-12	page 10-21
20	14	4	02	02B C1	LAs 13-14	page 10-21
21	15	4	02	02B D1	LAs 15-16	page 10-21
22	16	4	02	02G A1	LAs 17-18	page 10-21
23	17	4	02	02G B1	LAs 19-20	page 10-21
24	18	4	02	02G C1	LAs 21-22	page 10-21
25	19	4	02	02G D1	LAs 23-24	page 10-21
26	1A	4	03	03G A1	LAs 25-26	page 10-22
27	1B	4	03	03G B1	LAs 27-28	page 10-22
28	1C	4	03	03G C1	LAs 29-30	page 10-22
29	1D	4	03	03G D1	LAs 31-32	page 10-22
30	1E	5/7	04	04D A1	Lines 128-191	page 10-26 or page 10-33
31	1F	5/7	04	04G A1	Lines 192-255	page 10-26 or page 10-33
32	20	5/7	04	04B A1	Lines 256-319	page 10-26 or page 10-33
33	21	5/7	04	04E A1	Lines 320-383	page 10-26 or page 10-33
34	22	5/7	05	05D A1	Lines 384-447	page 10-27 or page 10-34
35	23	5/7	05	05G A1	Lines 448-511	page 10-27 or page 10-34
36	24	5/7	05	05B A1	Lines 512-575	page 10-27 or page 10-34
37	25	5/7	05	05E A1	Lines 576-639	page 10-27 or page 10-34
38	26	5/7	06	06D A1	Lines 640-703	page 10-27 or page 10-34
39	27	5/7	06	06G A1	Lines 704-767	page 10-27 or page 10-34
40	28	5/7	06	06B A1	Lines 768-831	page 10-27 or page 10-34
41	29	5/7	06	06E A1	Lines 832-895	page 10-27 or page 10-34

Primary Power Box AC Distribution



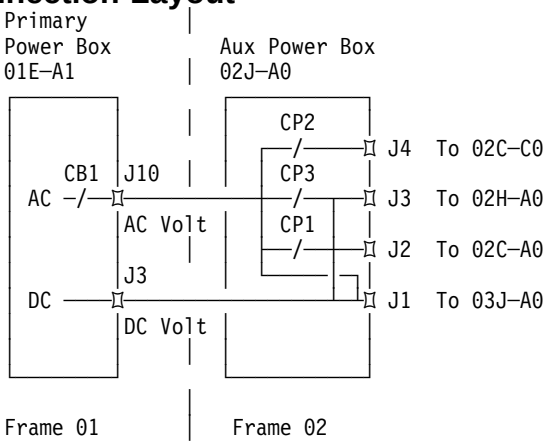
(1) J5 and J8 distribute AC and DC voltages.

Auxiliary Power Box Frame 02 (02J-A0)

Component Locations

See page YZ052.

Connection Layout



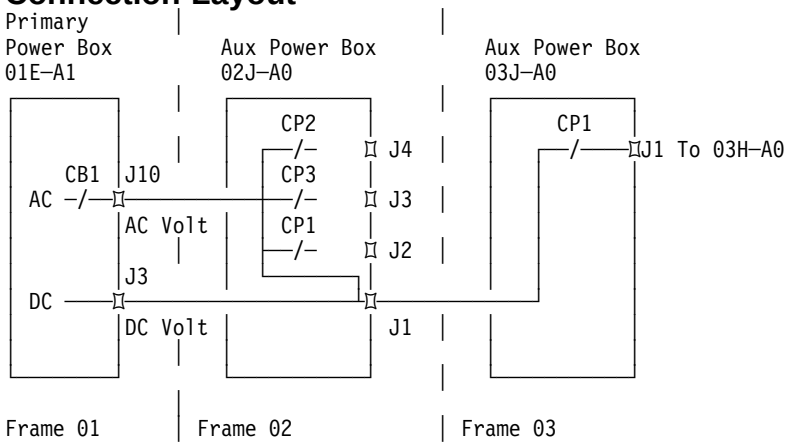
See page YZ552 for details.

Auxiliary Power Box Frame 03 (03J-A0)

Component Locations

See page YZ053.

Connection Layout

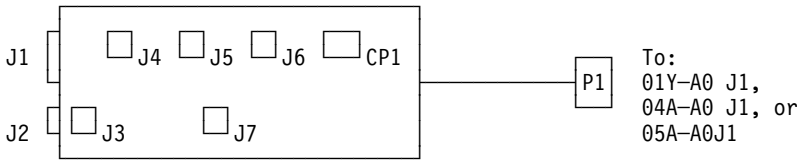


See page YZ553 for details.

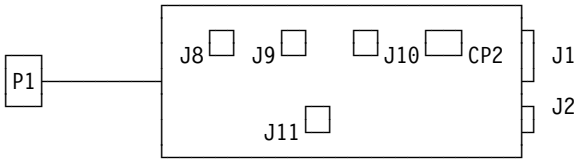
AC-DC Distribution (04A-A0, 05A-A0, 06A-A0)

Component Location

Front Side



Rear Side



CP1 For power supplies on the front side,
(04D-A1 and 04B-A1, or 05D-A1 an 05B-A1, or 06D-A1 and 06B-A1).
CP2 For power supplies on the rear side,
(04G-A1 and 04E-A1, or 05G-A1 and 05E-A1, or 06G-A1 and 06E-A1).
J1 For the cable from 05A-A0 on frame 04 or from 06A-A0 on frame 05 (P1).
J2 For the cable from 05A-A0 on frame 04 or from 06A-A0 on frame 05 (P2).
J3 Receives AFD from the next frame (P3).
J4 To front blower (04C-A0, 05C-A0, or 06C-A0).
J5 For cable from the lower power supply on the front side (04D-A1, 05D-A1, or 06D-A1).
J6 For cable from the upper power supply on the front side (04B-A1, 05B-A1, or 06B-A1).
J7 For AFD cable on front side (04C-A0, 05C-A0, or 06C-A0).
J8 To rear blower (04F-A0, 05F-A0, or 06F-A0).
J9 For cable from the lower power supply on the rear side (04G-A1, 05G-A1, or 06G-A1).
J10 For cable from the upper power supply on the rear side (04E-A1, 05E-A1, or 06E-A1).
J11 For AFD cable on the rear side (04F-A0, 05F-A0, or 06F-A0).
P1 AC power.

See page YZ054 for details.

For connection layout , see:

- “PS Type 5 Frame 04 Connection Layout” on page 10-26 for frame 04,
“PS Type 5 Frame 05 Connection Layout” on page 10-27 for frame 05,
“PS Type 5 Frame 06 Connection Layout” on page 10-27 for frame 06.
- “PS Type 7 Frame 04 Connection Layout” on page 10-33 for frame 04,
“PS Type 7 Frame 05 Connection Layout” on page 10-34 for frame 05,
“PS Type 7 Frame 06 Connection Layout” on page 10-34 for frame 06.

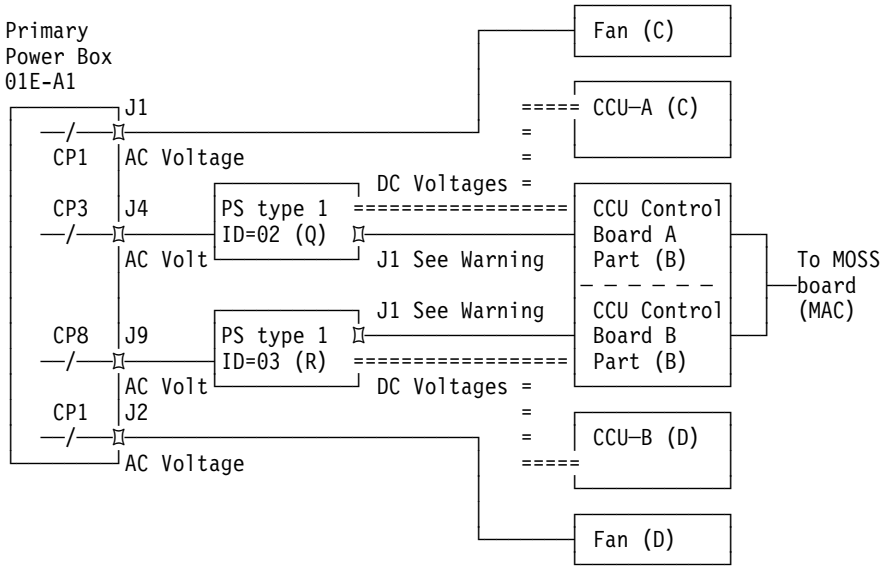
Power Supply Type 1 (PS Type 1)

The PS type 1 is used on 3745 Models 21x and 41x, for 3745 Model 31x and 61x, see “Power Supply Type 1B (PS Type 1B)” on page 10-13.

IMPORTANT

Maintenance inside the power supply assembly PS type 1 is prohibited.

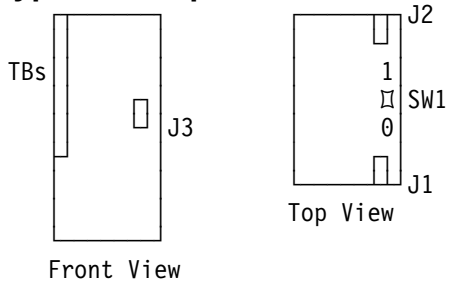
PS Type 1 Connection Layout



Warning: In case of PS type 1 destruction, check that the remote sense line from 01Q/01R–A0 J1 to 01C/01D–A1 C4 is not open.

See page YZ071 for details.

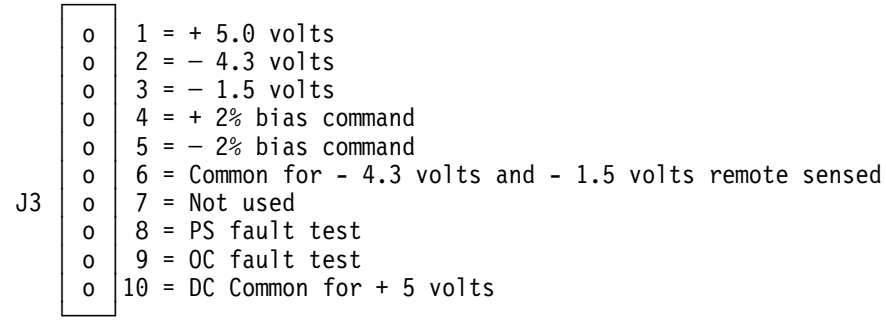
PS Type 1 Component Locations



Connectors J1 and J2, see page YZ071 for details.
Test connector J3, see “PS Type 1 DC Test Points” on page 10-11 for pin assignment.
Switch SW1: This switch, used for power supply addressing, is set to 0 when PS type 1 is connected to CCU-A. It is set to 1 when PS type 1 is connected to CCU-B.

See page YZ071 for details.

PS Type 1 DC Test Points



PS Type 1 DC Voltages and Tolerances

Test points on the power supply are for DC voltage Vmin or Vmax measurement only. Ripple measurement must be made on the board's test point.

Table 10-3. PS Type 1 Voltages and Tolerances

VDC	Vmin	Vmax	Ripple	J3 Test Point
+ 5.0	+ 4.85[1]	+ 5.25	0.10 p-p	1[2]
- 4.3	- 4.27	- 4.44	0.02 p-p	2[3]
- 1.5	- 1.47	- 1.53	0.01 p-p	3[3]

[1] This value is +4.75 volts on CCU control board or CCU-A or B test points.

[2] These values are referenced to test point 10.

[3] These values are referenced to test point 6.

Note: When PS type 1 is powered down with the POS function (other power supplies remain up) voltages at the test points will not go to 0 volt. Due to back circuits, approximately 1.5 volts may be present at + 5.0 volts test point.

CCU Control Board DC Voltage Test Points

Table 10-4. CCU Control Board DC Voltage Test Points

VDC	CCU-A Board Test Point[1] (PS ID = 02)	CCU-B Board Test Point[1] (PS ID = 03)
+ 5.00	01B-A2 Z3 05	01B-A2 Z3 08
- 4.30	01B-A2 Z3 04	01B-A2 Z3 09
- 1.50	01B-A2 Z3 03	01B-A2 Z3 10

[1] These values are referenced to 01B-A2 Z3 pin 07.

For pin location see page YZ333.

CCU-A and CCU-B DC Voltage Test Points

Table 10-5. CCU DC Voltage Test Points

VDC	CCU-A 01C-A1 Test Point[1] (PS ID = 02)	CCU-B 01D-A1 Test Point[1] (PS ID = 03)
- 4.30	C1 B	C1 B
- 1.50	C1 E	C1 E
Common	C1 D	C1 D

[1] These values are referenced to pin C1 D.

For pin location see page YZ333.

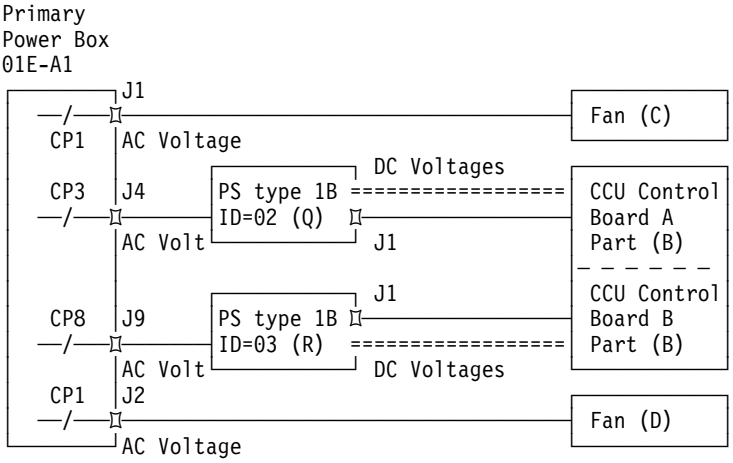
Power Supply Type 1B (PS Type 1B)

The PS type 1B is used on 3745 Models 31x and 61x, for 3745 Models 21x and 41x, see “Power Supply Type 1 (PS Type 1)” on page 10-10.

IMPORTANT

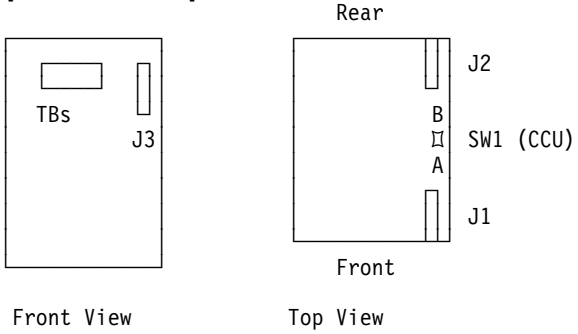
Maintenance inside the power supply assembly PS type 1B is prohibited.

PS Type 1B Connection Layout



See page YZ070 for details.

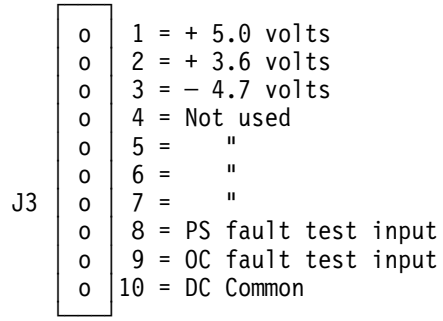
PS Type 1B Component Locations



Connectors J1 and J2, see page YZ070 for details.
Test connector J3, see “PS Type 1B DC Test Points” on page 10-14 for pin assignment.
Switch SW1: This switch, used for power supply addressing, is set to A when PS type 1B is connected to CCU-A. It is set to B when PS type 1B is connected to CCU-B.

See page YZ070 for details.

PS Type 1B DC Test Points



PS Type 1B DC Voltages and Tolerances

Test points on the power supply are for DC voltage Vmin or Vmax measurement only. Ripple measurement must be made on the board's test point.

Table 10-6. PS Type 1B Voltages and Tolerances

VDC	Vmin	Vmax	Ripple	J3 Test Point [2]
+ 5.0	+ 4.87[1]	+ 5.25	0.10 p-p	1
+ 3.6	+ 3.52	+ 3.80	0.05 p-p	2
- 4.7	- 4.55	- 4.95	0.05 p-p	3

[1] This value is +4.75 volts on CCU control board test points.

[2] These values are referenced to test point 10.

Note: When PS type 1B is powered down with the POS function (other power supplies remain up) voltages at the test points will not go to 0 volt. Due to back circuits, approximately 1.5 volts may be present at + 5.0 volts test point.

CCU Control Board DC Voltage Test Points

Table 10-7. CCU Control Board DC Voltage Test Points

VDC	CCU-A Board Test Point[1] (PS ID = 02)	CCU-B Board Test Point[1] (PS ID = 03)	Common Test Point
+ 5.00	01B-A1 Y3 B08 01B-A1 Z3 B08 01B-A2 Z3 D05	01B-A1 Y3 D05 01B-A1 Z3 D05 01B-A2 Z3 B08	01B-A1 Y3 B06 01B-A1 Z3 B06 01B-A2 Z3 D07
+ 3.60	01B-A1 Y3 B09 01B-A1 Z3 B09 01B-A2 Z3 D04	01B-A1 Y3 D04 01B-A1 Z3 D04 01B-A2 Z3 B09	01B-A1 Y3 B06 01B-A1 Z3 B06 01B-A1 Z3 D07
- 4.70	01B-A2 Z3 D03	01B-A2 Z3 B10	01B-A1 Z3 D07

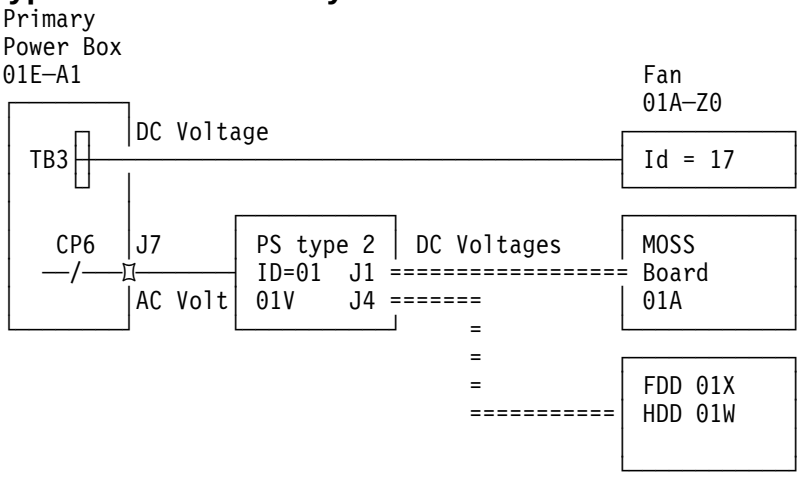
For pin location see page YZ333.

Power Supply Type 2 (PS Type 2)

IMPORTANT

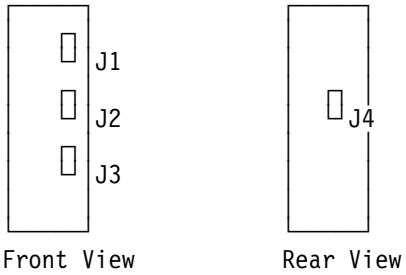
Maintenance inside power supply assembly PS type 2 is prohibited.

PS Type 2 Connection Layout



See page YZ561 for details.

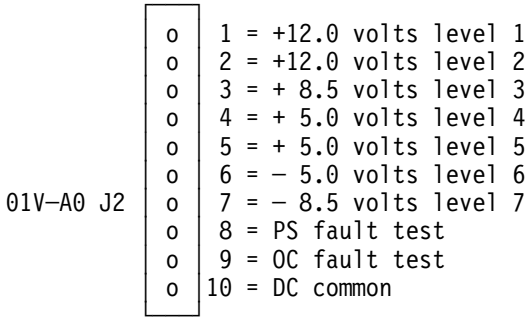
PS Type 2 Component Locations



J1: MOSS power
J2: Voltage test point
J3: Power control bus
J4: Power for disk and diskette

Connectors J1, J3 and J4, see page YZ072 for details.
Test connector J2, see “PS Type 2 DC Voltage Test Points.” on page 10-16 for pin assignment.

PS Type 2 DC Voltage Test Points.



PS Type 2 DC Voltages and Tolerances

Test points on the power supply are for DC voltage Vmin or Vmax measurement only.

Table 10-8. PS type 2 Voltages and Tolerances

VDC	Level	Vmin	Vmax	J2 Test Point[1]
+12.00	1	+11.00	+13.00	1
+12.00	2	+11.60	+12.60	2
+ 8.50	3	+ 7.90	+ 9.35	3
+ 5.00	4	+ 4.85	+ 5.25	4
+ 5.00	5	+ 4.85	+ 5.25	5
- 5.00	6	- 4.60	- 5.50	6
- 8.50	7	- 7.90	- 9.35	7

[1] = These values are referenced to test point 10.

MOSS Board DC Voltages and Tolerances (PS Type 2)

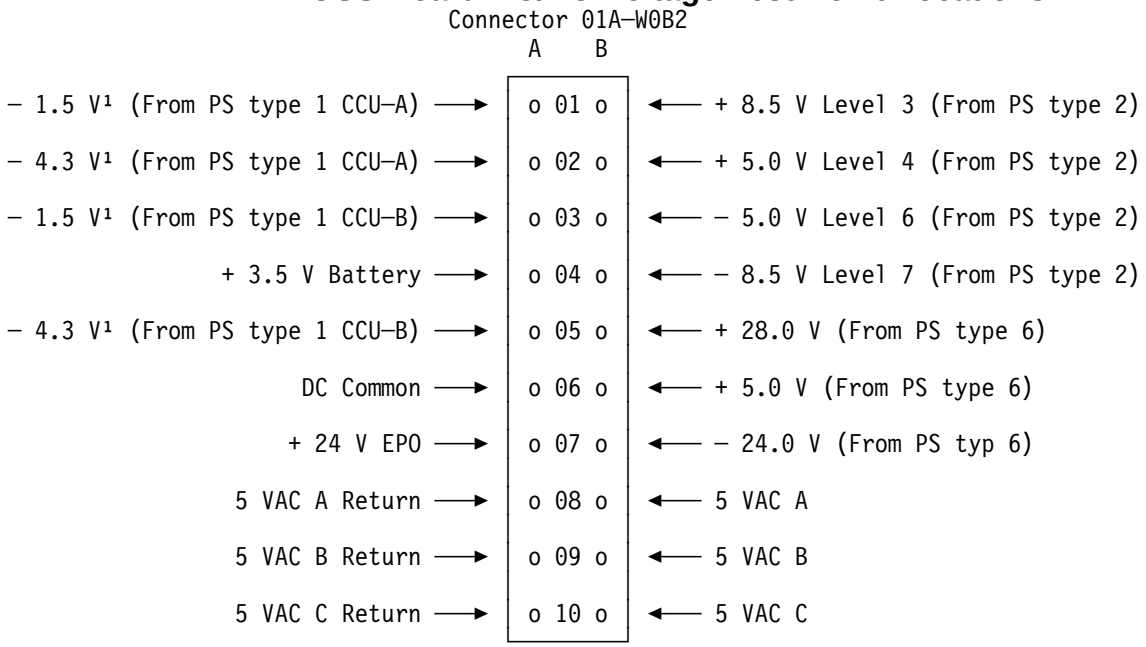
Ripple measurement must be made on the board's test point.

Table 10-9. MOSS Board Voltages and Tolerances (from PS Type 2)

VDC	Level	Vmin	Vmax	Ripple
+ 8.50	3	+ 7.65	+ 9.35	0.15 p-p
+ 5.00	4	+ 4.75	+ 5.25	0.10 p-p
- 5.00	6	- 4.50	- 5.50	0.10 p-p
- 8.50	7	- 7.65	- 9.35	0.15 p-p

For + 12 volts levels 1 and 2, and + 5 volts level 5, see “Disk Voltages and Tolerances (From PS Type 2)” on page 10-38.

MOSS Board DC/AC Voltage Test Point Locations



1 = For model 21x or 41x only. These voltage test points are available once the MOSS board with the PN 66X1534 (EC A47425) is installed. PN 66X1534 and EC A47425 are visible on board location 01A-W0A3.

For connector location, see page YZ031.

Battery Voltage Tolerances

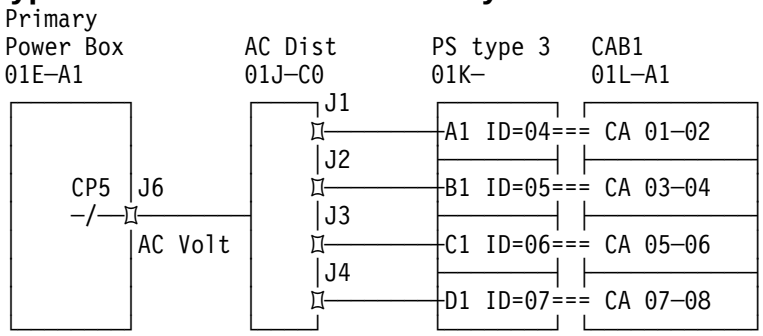
- Vmax = 3.7
- Vmin = 2.7

Power Supply Type 3 (PS Type 3)

IMPORTANT

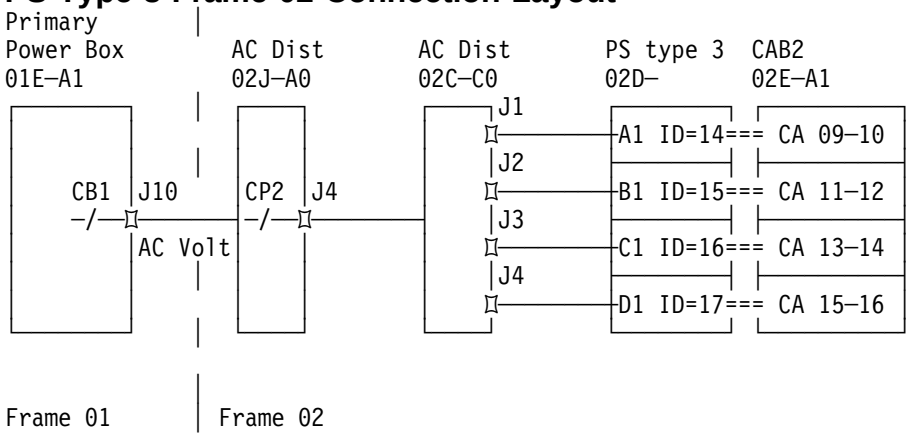
Maintenance inside power supply assembly PS type 3 is prohibited.

PS Type 3 Frame 01 Connection Layout



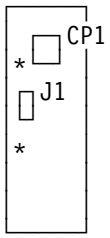
See page YZ551 for details.

PS Type 3 Frame 02 Connection Layout



See page YZ552 for details.

PS Type 3 Component Locations



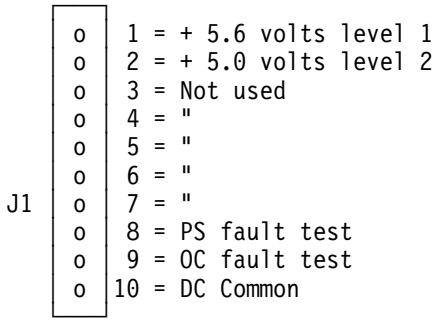
Front View

J1: Voltage test points

* = Screws, when installed insure a contact inside the PS type 3.

See page YZ073 for details.

PS Type 3 DC Voltage Test Points.



PS Type 3 DC Voltages and Tolerances

Test points on power supply are for DC voltage Vmin or Vmax measurement only. Ripple measurement must be done on the board's test point.

Table 10-10. PS Type 3 Voltages and Tolerances

VDC	Level	Vmin on J1	Vmin on Board	Vmax	Ripple	J1 Test Point[1]
+ 5.60	1	+ 5.43	+ 5.32	+ 5.88	0.10 p-p	1
+ 5.00	2	+ 4.85	+ 4.75	+ 5.25	0.10 p-p	2

[1] = These values are referenced to test point 10.

CA Board DC Voltage Test Points

On the following table the DC values are referenced to pin D08 of the same connector.

Table 10-11. CA Board DC Voltage Test Point

CA Number	PS Type 3 ID	PS Type 3 Location	Board Location	Board Test Point + 5.60	+ 5.00
01 and 02	04	01K-A1	01L-A1	YR D02	YR D03
03 and 04	05	01K-B1	01L-A1	YR D09	YR D10
05 and 06	06	01K-C1	01L-A1	YR B13	YR B12
07 and 08	07	01K-D1	01L-A1	YR B06	YR B05
09 and 10	14	02D-A1	02E-A1	YR D02	YR D03
11 and 12	15	02D-B1	02E-A1	YR D09	YR D10
13 and 14	16	02D-C1	02E-A1	YR B13	YR B12
15 and 16	17	02D-D1	02E-A1	YR B06	YR B05

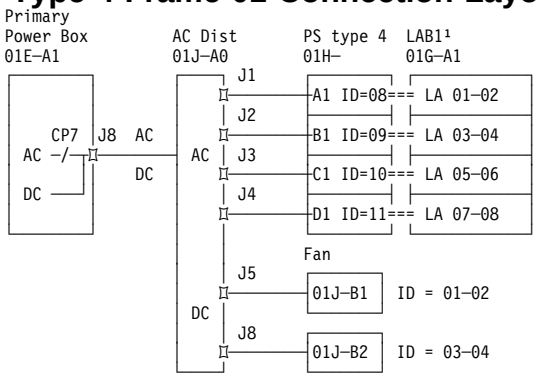
For connector and pin location see page YZ337.

Power Supply Type 4 (PS Type 4)

IMPORTANT

Maintenance inside power supply assembly PS type 4 is prohibited.

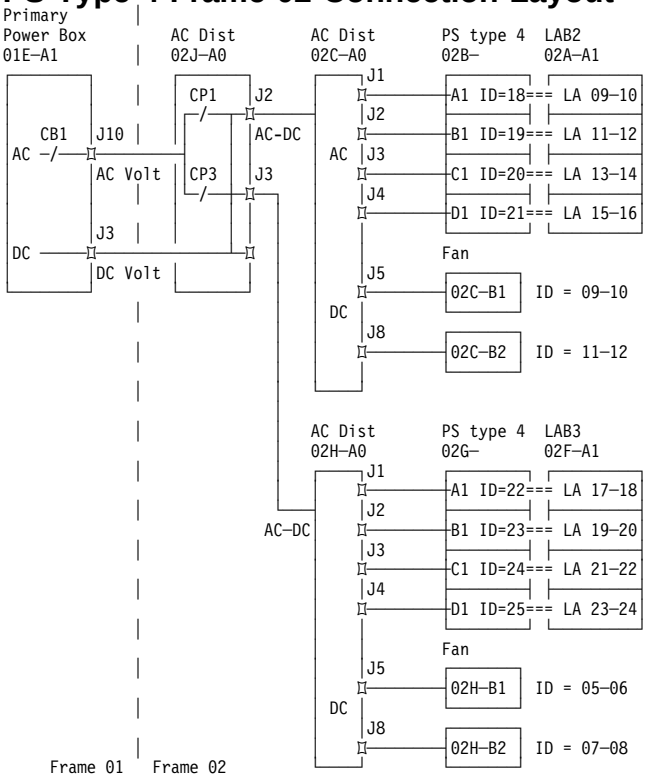
PS Type 4 Frame 01 Connection Layout



1 = LA on LAB1 can be a LSS, a TRA, or an HSS adapter.

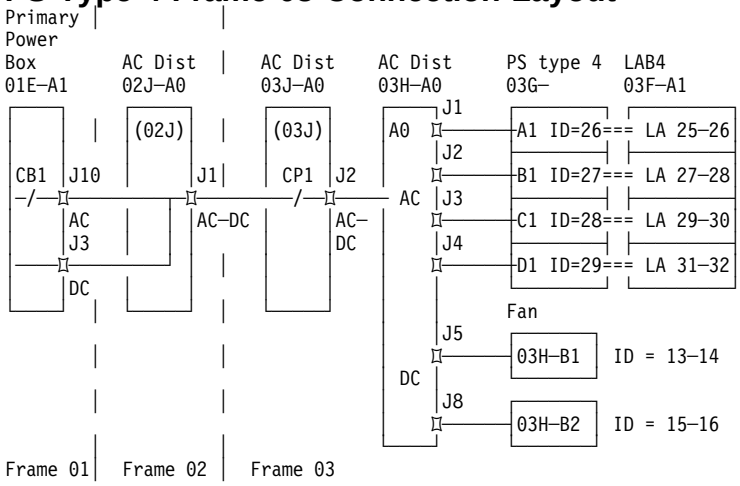
See page YZ511 for details.

PS Type 4 Frame 02 Connection Layout



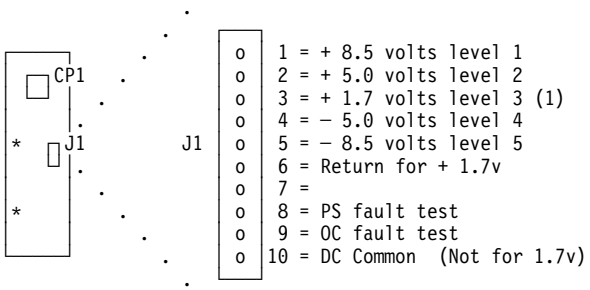
See page YZ512 for details.

PS Type 4 Frame 03 Connection Layout



See page YZ513 for details.

PS Type 4 DC Voltage Test Points



* = Screws, when installed insure a contact inside PS type 4.
(1) = +1.7 volts level 3 is remote–sensed.

See page YZ074 for details.

PS Type 4 DC Voltages and Tolerances

Test points on the power supply are for DC voltage Vmin or Vmax measurement only. Ripple measurement must be made on the board's test point.

Table 10-12. PS Type 4 Voltages and Tolerances

VDC	Level	Vmin on J1	Vmin on Board	Vmax	Ripple	J1 Test' Point[1]
+ 8.50	1	+ 7.90	+ 7.65	+ 9.35	0.15 p-p	1
+ 5.00	2	+ 4.87	+ 4.85	+ 5.25	0.10 p-p	2
+ 1.70	3	+ 1.68	+ 1.67	+ 1.79	0.01 p-p	3
- 5.00	4	- 4.60	- 4.50	- 5.50	0.10 p-p	4
- 8.50	5	- 7.90	- 7.65	- 9.35	0.15 p-p	5

[1] = These values are referenced to test point 10, except 1.7 volts which is referenced to test point 6. See YZ735 and YZ736 for board test points.

Line Adapter Board DC Voltage Test Points

On the following table the TSSB board test points are accessible only when the board is empty. Voltages can be checked on the top of the cards, see “CSP, FESL, and FESH/EAC Card Voltage Test Points” on page 10-24 for details.

For DC common, use pin D08 of the same connector.

LA	PS Type 4 Location	PS Type 4 ID	Board Location	Card Test Point + 8.50[2]	+ 5.00	- 1.70	- 5.00	- 8.50[2]
01-02[1]	01H-A1	08	01G-A1	A2[3] D02	A2[3] D03	A2[3] D04	A2[3] D05	A2[3] D06
03-04	01H-B1	09		A2[3] D09	A2[3] D10	A2[3] D11	A2[3] D12	A2[3] D13
05-06[1]	01H-C1	10		A2[3] B13	A2[3] B12	A2[3] B11	A2[3] B10	A2[3] B09
07-08	01H-D1	11		A2[3] B06	A2[3] B05	A2[3] B04	A2[3] B03	A2[3] B02
09-10	02B-A1	18	02A-A1	A2 D02	A2 D03	A2 D04	A2 D05	A2 D06
11-12	02B-B1	19		A2 D09	A2 D10	A2 D11	A2 D12	A2 D13
13-14	02B-C1	20		A2 B13	A2 B12	A2 B11	A2 B10	A2 B09
15-16	02B-D1	21		A2 B06	A2 B05	A2 B04	A2 B03	A2 B02
17-18	02G-A1	22	02F-A1	A2 D02	A2 D03	A2 D04	A2 D05	A2 D06
19-20	02G-B1	23		A2 D09	A2 D10	A2 D11	A2 D12	A2 D13
21-22	02G-C1	24		A2 B13	A2 B12	A2 B11	A2 B10	A2 B09
23-24	02G-D1	25		A2 B06	A2 B05	A2 B04	A2 B03	A2 B02
25-26	03G-A1	26	03F-A1	A2 D02	A2 D03	A2 D04	A2 D05	A2 D06
27-28	03G-B1	27		A2 D09	A2 D10	A2 D11	A2 D12	A2 D13
29-30	03G-C1	28		A2 B13	A2 B12	A2 B11	A2 B10	A2 B09
31-32	03G-D1	29		A2 B06	A2 B05	A2 B04	A2 B03	A2 B02

[1] LAs 1-2 and 5-6 can be replaced by four TRAs when the TSST board is installed.
Only + 5 volts are used on these LAs.

[2] ± 8.5 volts are used only for HSS adapters.

[3] Connector A2 is for the TSSB board and is replaced by a connector located on the left side of the 01G-A1 board when a TSST board is installed.

Figure 10-2. Line Adapter Board DC Voltage Test Points

For connector and pin locations, see pages YZ335 and YZ336.

CSP, FESL, and FESH/EAC Card Voltage Test Points:

For DC common, use pin Z29 of the FESL or FESH card.

LA	PS Type 4 Location	PS Type 4 ID	Board Location	Card Test Point CSP + 1.70	FESL, FESH, or EAC[2] + 8.50[1]	+ 5.00	- 5.00	- 8.50[1]
01	01H-A1	08	01G-A1	E2 Z33	F2 Z12	F2 Z32	F2 Z33	F2 Z13
02				G2 Z33	H2 Z12	H2 Z32	H2 Z33	H2 Z13
03	01H-B1	09		J2 Z33	K2 Z12	K2 Z32	K2 Z33	K2 Z13
04				L2 Z33	M2 Z12	M2 Z32	M2 Z33	M2 Z13
05	01H-C1	10		N2 Z33	P2 Z12	P2 Z32	P2 Z33	P2 Z13
06				Q2 Z33	R2 Z12	R2 Z32	R2 Z33	R2 Z13
07	01H-D1	11		S2 Z33	T2 Z12	T2 Z32	T2 Z33	T2 Z13
08				U2 Z33	V2 Z12	V2 Z32	V2 Z33	V2 Z13
09	02B-A1	18	02A-A1	E2 Z33	F2 Z12	F2 Z32	F2 Z33	F2 Z13
10				G2 Z33	H2 Z12	H2 Z32	H2 Z33	H2 Z13
11	02B-B1	19		J2 Z33	K2 Z12	K2 Z32	K2 Z33	K2 Z13
12				L2 Z33	M2 Z12	M2 Z32	M2 Z33	M2 Z13
13	02B-C1	20		N2 Z33	P2 Z12	P2 Z32	P2 Z33	P2 Z13
14				Q2 Z33	R2 Z12	R2 Z32	R2 Z33	R2 Z13
15	02B-D1	21		S2 Z33	T2 Z12	T2 Z32	T2 Z33	T2 Z13
16				U2 Z33	V2 Z12	V2 Z32	V2 Z33	V2 Z13
17	02G-A1	22	02F-A1	E2 Z33	F2 Z12	F2 Z32	F2 Z33	F2 Z13
18				G2 Z33	H2 Z12	H2 Z32	H2 Z33	H2 Z13
19	02G-B1	23		J2 Z33	K2 Z12	K2 Z32	K2 Z33	K2 Z13
20				L2 Z33	M2 Z12	M2 Z32	M2 Z33	M2 Z13
21	02G-C1	24		N2 Z33	P2 Z12	P2 Z32	P2 Z33	P2 Z13
22				Q2 Z33	R2 Z12	R2 Z32	R2 Z33	R2 Z13
23	02G-D1	25		S2 Z33	T2 Z12	T2 Z32	T2 Z33	T2 Z13
24				U2 Z33	V2 Z12	V2 Z32	V2 Z33	V2 Z13
25	03G-A1	26	03G-A1	E2 Z33	F2 Z12	F2 Z32	F2 Z33	F2 Z13
26				G2 Z33	H2 Z12	H2 Z32	H2 Z33	H2 Z13
27	03G-B1	27		J2 Z33	K2 Z12	K2 Z32	K2 Z33	K2 Z13
28				L2 Z33	M2 Z12	M2 Z32	M2 Z33	M2 Z13
29	03G-C1	28		N2 Z33	P2 Z12	P2 Z32	P2 Z33	P2 Z13
30				Q2 Z33	R2 Z12	R2 Z32	R2 Z33	R2 Z13
31	03G-D1	11		S2 Z33	T2 Z12	T2 Z32	T2 Z33	T2 Z13
32				U2 Z33	V2 Z12	V2 Z32	V2 Z33	V2 Z13

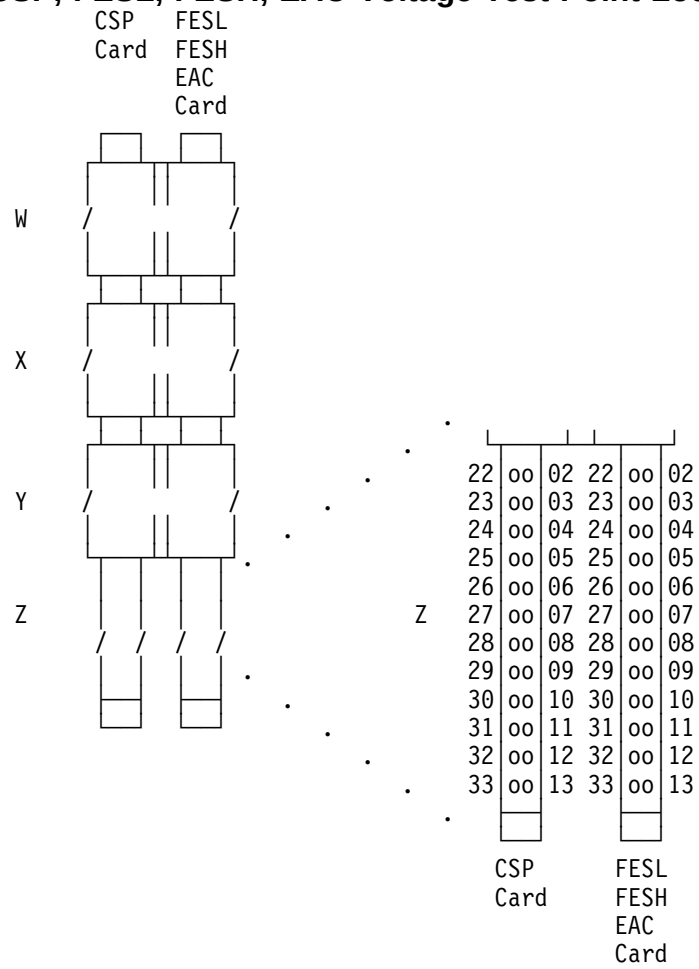
[1] ± 8.50 Volts are used only for HSS adapters.
[2] The EAC uses + 5.00V voltage only.

For pin locations, see "CSP, FESL, FESH, EAC Voltage Test Point Location" on page 10-25.

CSP, FESL, FESH, and EAC Voltages and Tolerances

VDC	Vmin	Vmax
+ 8.50	+ 7.60	+ 9.35
+ 5.00	+ 4.75	+ 5.25
+ 1.70	+ 1.67	+ 1.79
- 5.00	- 4.50	- 5.50
- 8.50	- 7.60	- 9.35

CSP, FESL, FESH, EAC Voltage Test Point Location



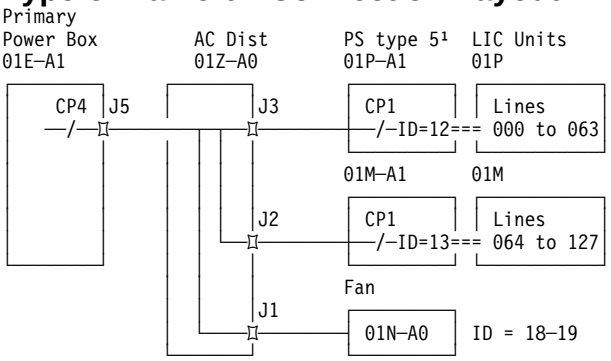
For details, see pages YZ735 and YZ736

Power Supply Type 5 (PS Type 5)

IMPORTANT

Maintenance inside power supply assembly PS type 5 is prohibited.

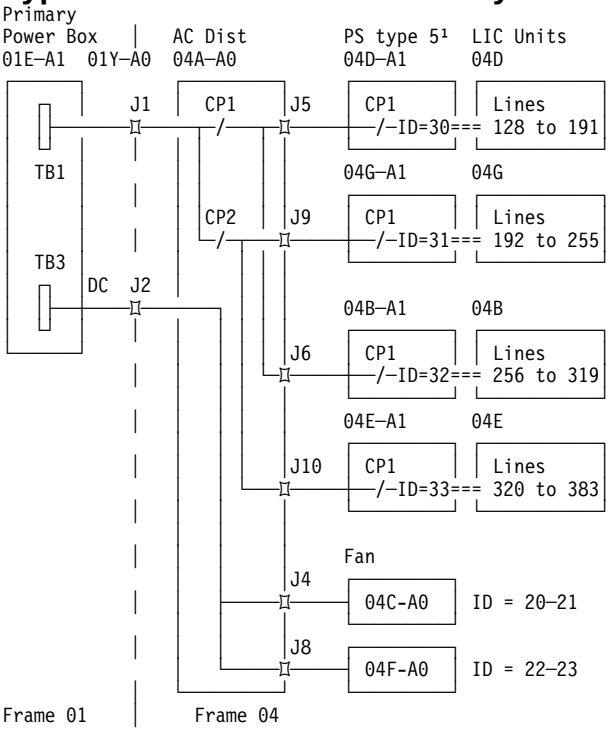
PS Type 5 Frame 01 Connection Layout



1 = When a PS type 5 is powered OFF, the LAs connected to the corresponding lines must be IMLed.

See page YZ551 for details.

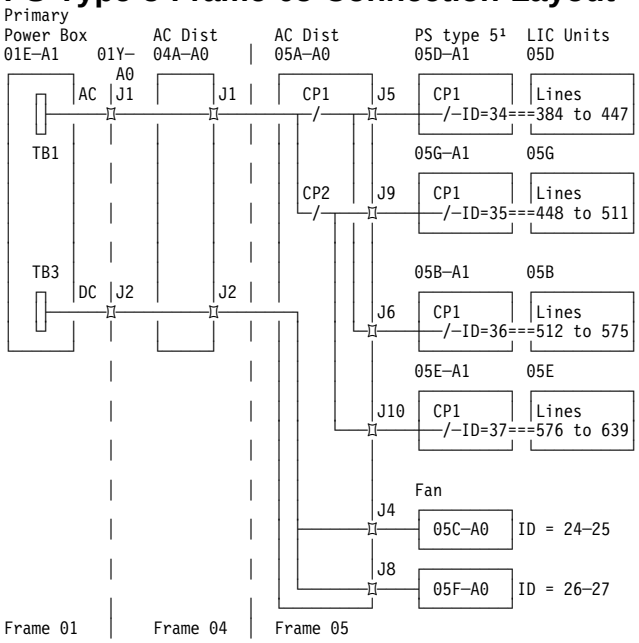
PS Type 5 Frame 04 Connection Layout



1 = When a PS type 5 is powered OFF, the LAs connected to the corresponding lines must be IMLed.

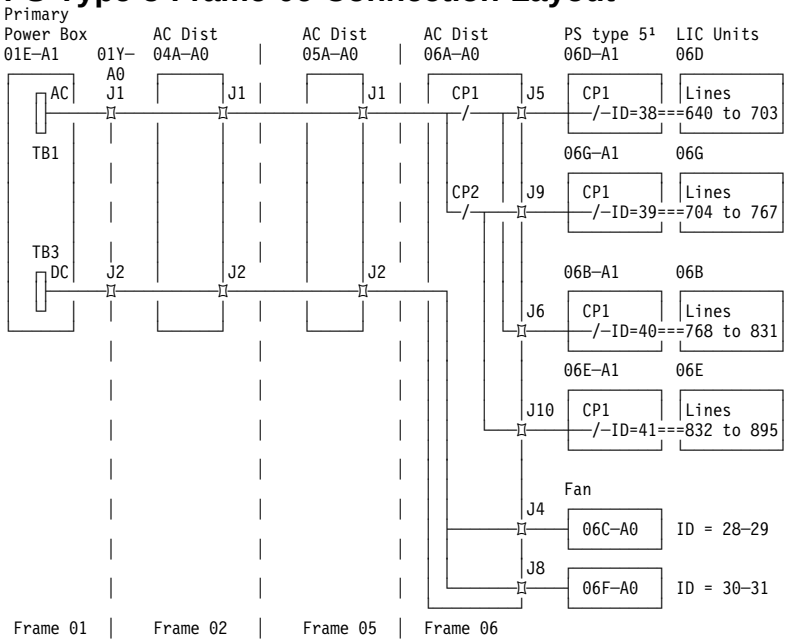
See page YZ554 for details.

PS Type 5 Frame 05 Connection Layout



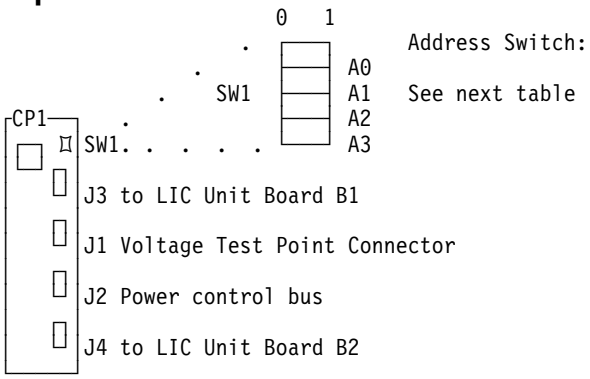
1 = When a PS type 5 is powered OFF, the LAs connected to the corresponding lines must be IMLed.
See page YZ554 for details.

PS Type 5 Frame 06 Connection Layout



1 = When a PS type 5 is powered OFF, the LAs connected to the corresponding lines must be IMLed.
See page YZ554 for details.

PS Type 5 Component Locations



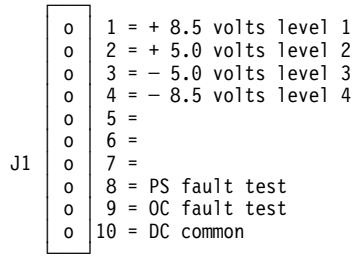
Connectors J2, J3, and J4 see page YZ075 for details.
Connector J1, see **"PS Type 5 DC Voltage Test points"** on page 10-29 for pin assignments.
Switch SW1: Four binary switches used to select the address of the power supply.

SW1 switch position:

Table 10-13. PS Type 5 SW1 Switch Positions

PS Type 5 Location	PS ID	SW1 Switch			
		A3	A2	A1	A0
01P	12	0	0	0	0
01M	13	0	0	1	0
04D	30	0	0	0	0
04G	31	0	0	0	0
04B	32	0	0	0	1
04E	33	0	0	0	1
05D	34	0	0	1	0
05G	35	0	0	1	0
05B	36	0	0	1	1
05E	37	0	0	1	1
06D	38	0	1	0	0
06G	39	0	1	0	0
06B	40	0	1	0	1
06E	41	0	1	0	1

PS Type 5 DC Voltage Test points



PS type 5 DC Voltages and Tolerances

Test points on the power supply are for DC voltage Vmin or Vmax measurement only. Ripple measurement must be made on the board's test point.

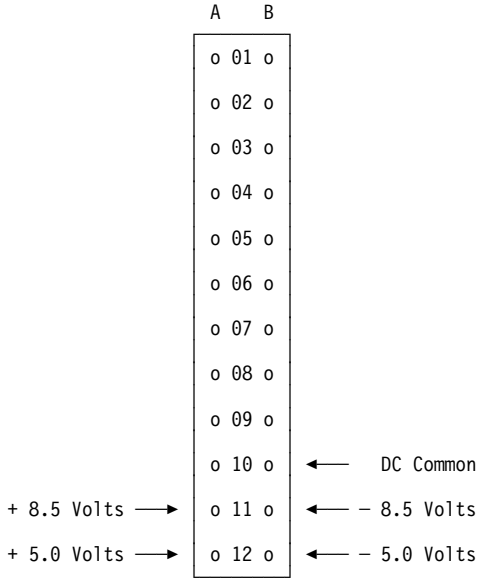
Table 10-14. PS type 5 Voltages and Tolerances

VDC	Level	Vmin on J1	Vmin on Board	Vmax	Ripple	J1 Test Point[1]
+ 8.50	1	+ 7.90	+ 7.65	+ 9.35	0.15 p-p	1
+ 5.00	2	+ 4.85	+ 4.75	+ 5.25	0.10 p-p	2
- 5.00	3	- 4.60	- 4.50	- 5.50	0.10 p-p	3
- 8.50	4	- 7.90	- 7.65	- 9.35	0.15 p-p	4

[1] = These values are referenced to test point 10.

LIC Unit Board DC Voltage Test Points

The DC voltage test points are located on the DMUX card.
For detailed locations, see page YZ738.



Power Supply Type 6 (PS Type 6)

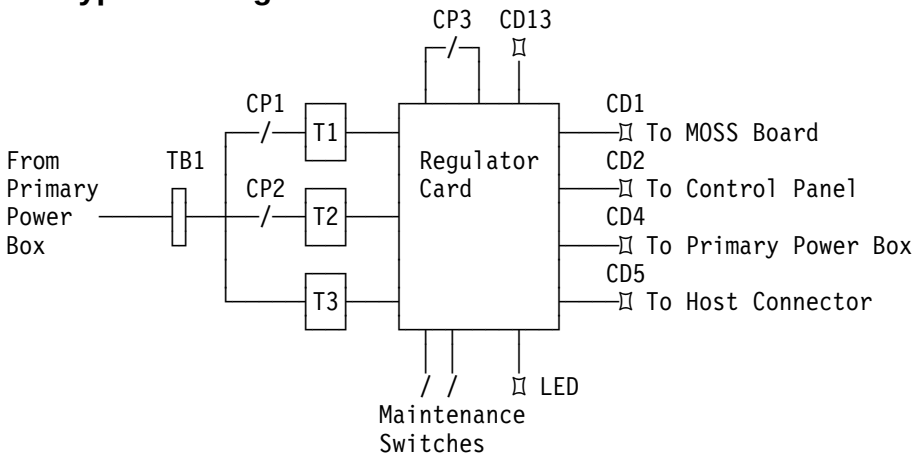
PS type 6 is an FRU. Do not exchange parts inside the PS.

This power supply provides:

- + 24, - 24, + 5, and + 28 DC control voltages.
- 5 VAC for AC line monitoring purposes.
- Main contactor K2 driver.
- 5 and 28 volts disconnection and K2 main contactor holding for concurrent maintenance of the power system control (PAC and PLC cards).
- Interconnection to host EPO box (standard power interface).

PS type 6 is a duplicated power. Voltages A and B are ored and controlled by CP1 for A voltages and CP2 for B voltages.

PS Type 6 Wiring Connection



See page YZ576 for details.

PS Type 6 AC Adjustment

WARNING:

Set the jumpers on TB1 according to the measured input voltage.
See page YZ576 for details.

See page YZ061 for component locations.

PS Type 6 Component Function

- Maintenance switches: Two switches SW1 and SW2 are used for maintenance.

  1. SW1:

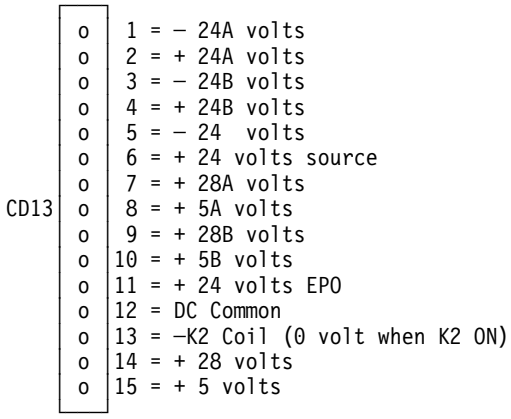
     This switch, when pulled, allows using switch SW2. It is automatically restored to the normal position when closing the internal cover.

2. SW2:

   This switch in T1 position forces the K2 relay ON, and allows replacing the control panel during concurrent maintenance, and replacing the PAC or the PLC card in the MOSS board, by suppressing the +5 and +28 volts. When these voltages are suppressed, all the power controls are disabled.

   This switch in the T2 position forces the K2 relay ON, and allows testing the exchanged FRU (control panel, PAC, or PLC card).

- CP1 and CP2: AC circuit protectors.
- CP3: 24 volts circuit protector.
- LED is ON when K2 is forced ON and the maintenance switch SW1 is in the ON position.
- CD13: DC voltage test points.



A and B are duplicated voltages inside PS type 6. Voltages A and B are ored and give a common voltage.

PS type 6 Voltages and Tolerances

Test points on the power supply are for DC voltage Vmin or Vmax measurement only.

Table 10-15. PS Type 6 Voltages and Tolerances

Volt	Vmin	Vmax	CD13 Test Point[1]
+ 24	+ 20.40	+ 27.70	6/11
- 24	- 20.40	- 27.70	5
+ 5	+ 4.92	+ 5.25	15
+ 28	+ 25.00	+ 31.10	14

[1] These values are referenced to test point 12.

MOSS Board Voltages and Tolerances (PS Type 6)

Ripple measurement must be made at the MOSS board test point.

For connector and pin location see:
"MOSS Board DC/AC Voltage Test Point Locations" on page 10-17.

Table 10-16. MOSS Board Voltages and Tolerances (PS Type 6)

Volt	Vmin	Vmax	Ripple	MOSS Board Test Point[1]
+ 24 EPO MOSS	+ 16.50	+ 27.50	0.5 p-p	01A-W0 B2 A07
- 24	- 16.50	- 27.50	1.0 p-p	01A-W0 B2 B07
+ 5	+ 4.75	+ 5.25	0.1 p-p	01A-W0 B2 B06
+ 28	+ 25.00	+ 31.10	0.5 p-p	01A-W0 B2 B05
5 VAC A	4.30	5.70	NA	01A-W0 B2 B08
5 VAC B	4.30	5.70	NA	01A-W0 B2 B09
5 VAC C	4.30	5.70	NA	01A-W0 B2 B10

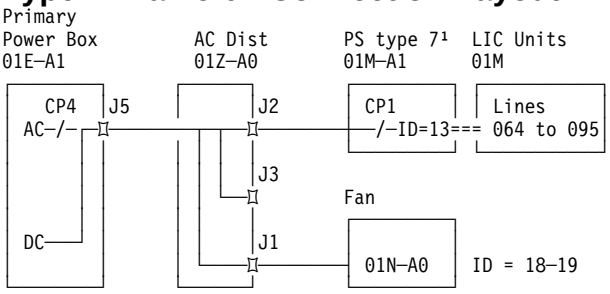
[1] These values are referenced to test point 01A-W0 B2 A06,
except for 5 VAC A = 01A-W0 B2 A08,
5 VAC B = 01A-W0 B2 A09, and
5 VAC C = 01A-W0 B2 A09.

Power Supply Type 7 (PS Type 7)

IMPORTANT

Maintenance inside power supply assembly PS type 7 is prohibited.

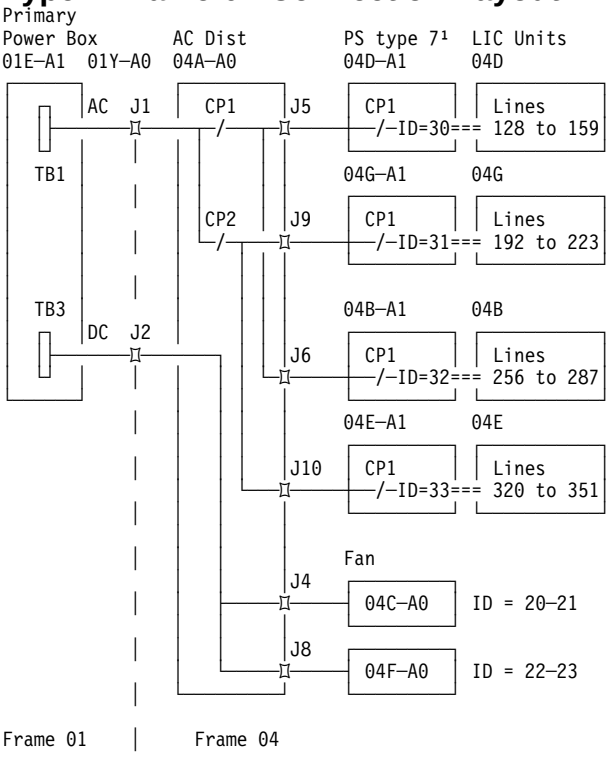
PS Type 7 Frame 01 Connection Layout



1 = When a PS type 7 is powered OFF, the LAs connected to the corresponding lines must be IMLed.

See page YZ551 for details.

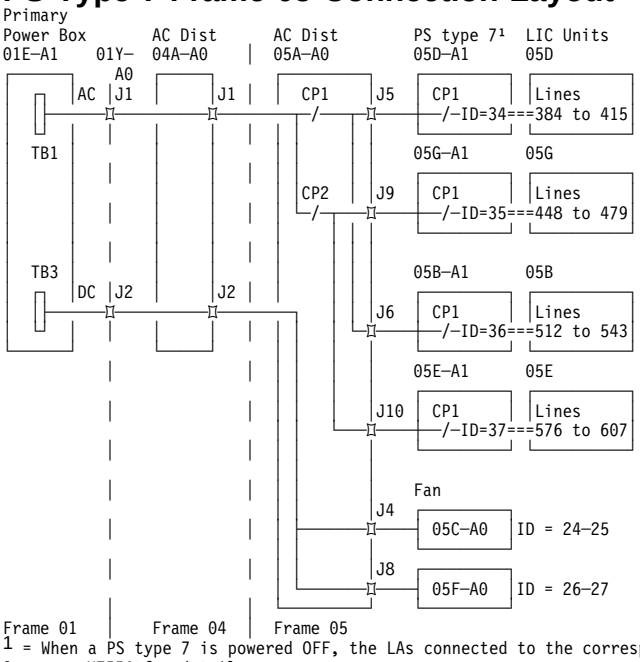
PS Type 7 Frame 04 Connection Layout



1 = When a PS type 7 is powered OFF, the LAs connected to the corresponding lines must be IMLed.

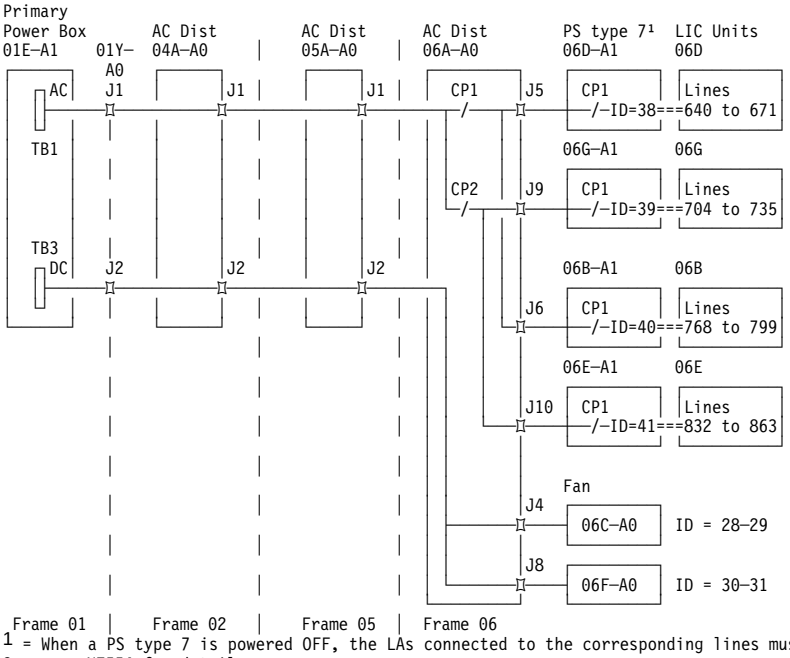
See page YZ554 for details.

PS Type 7 Frame 05 Connection Layout



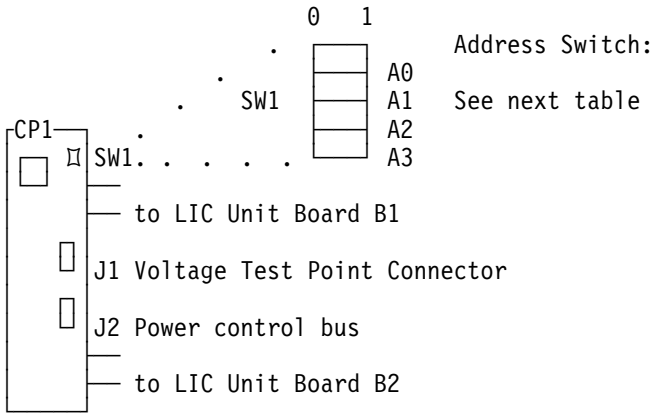
1 = When a PS type 7 is powered OFF, the LAs connected to the corresponding lines must be IMLed.
See page YZ554 for details.

PS Type 7 Frame 06 Connection Layout



1 = When a PS type 7 is powered OFF, the LAs connected to the corresponding lines must be IMLed.
See page YZ554 for details.

PS Type 7 Component Locations



For connection see page YZ077 for details.

Connector J1, see “PS Type 7 DC Voltage Test points” on page 10-36 for pin assignments.

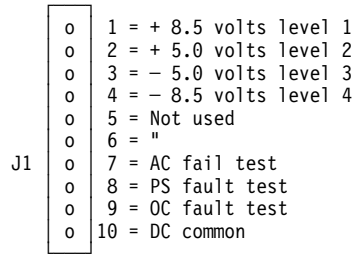
Switch SW1: Four binary switches used to select the address of the power supply.

SW1 switch position:

Table 10-17. PS Type 7 SW1 Switch Positions

PS Type 7 Location	PS ID	SW1 Switch			
		A3	A2	A1	A0
01M	13	0	0	1	1
04D	30	1	0	0	0
04G	31	1	0	0	0
04B	32	1	0	0	1
04E	33	1	0	0	1
05D	34	1	0	1	0
05G	35	1	0	1	0
05B	36	1	0	1	1
05E	37	1	0	1	1
06D	38	1	1	0	0
06G	39	1	1	0	0
06B	40	1	1	0	1
06E	41	1	1	0	1

PS Type 7 DC Voltage Test points



PS type 7 DC Voltages and Tolerances

Test points on the power supply are for DC voltage Vmin or Vmax measurement only. Ripple measurement must be made on the board's test point.

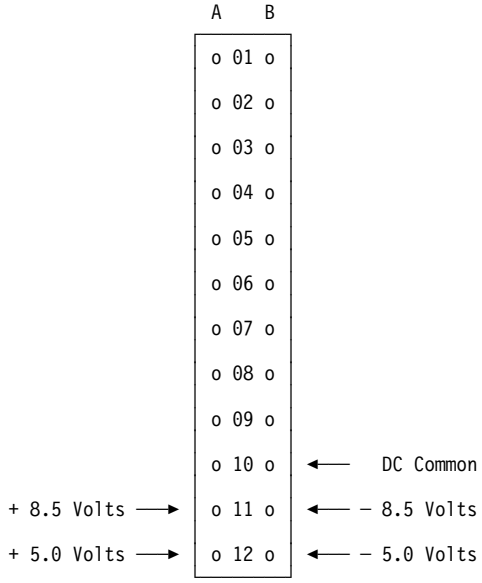
Table 10-18. PS type 7 Voltages and Tolerances

VDC	Level	Vmin on J1	Vmin on Board	Vmax	Ripple	J1 Test Point[1]
+ 8.50	1	+ 8.24	+ 8.07	+ 8.93	0.15 p-p	1
+ 5.00	2	+ 4.85	+ 4.75	+ 5.25	0.10 p-p	2
- 5.00	3	- 4.60	- 4.50	- 5.50	0.10 p-p	3
- 8.50	4	- 8.24	- 8.07	- 8.93	0.15 p-p	4

[1] = These values are referenced to test point 10.

LIC Unit Board DC Voltage Test Points

The DC voltage test points are located on the SMUX card.
For detailed locations, see page YZ739.



Power Supply Type 8 (PS Type 8)

PS type 8 is located inside the primary power box. See pages YZ061 and YZ078 for component location.

PS type 8 supplies:

- DC voltage, 48 volts to the DC fans.
- AC voltage, 200 volts to AC fans (CCU-A and B).

PS Type 8 Voltage Tolerances

Voltage	Vmin	Vmax	Ripple
48V DC	43.5	54	5 V p-p
200V AC	175	225	-

WARNING:

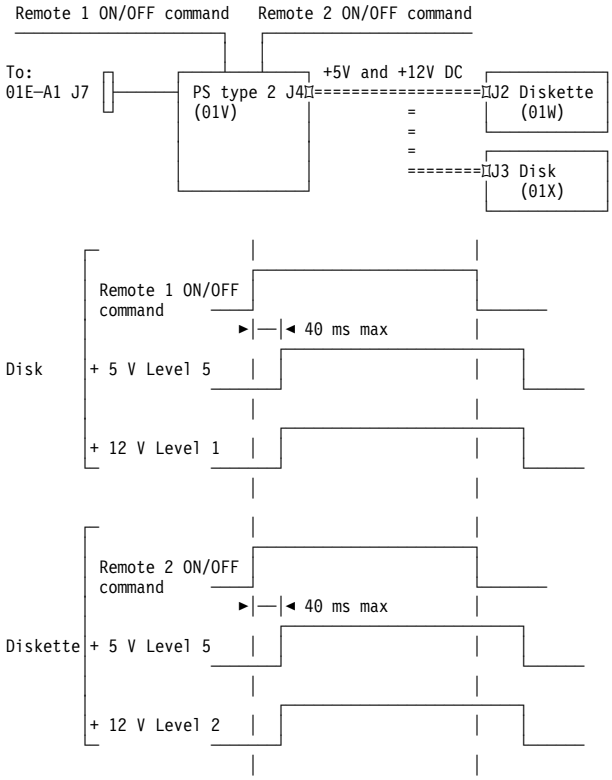
PS type 8 is a ferro-resonant PS.
Set the strap connector on J12 for 200 Volt, or on J13 for 220 Volts, or on J14 for 240 Volts, according to the measured input voltage. See page YZ561 and YZ578 for details.

See page YZ078 for component locations

Disk and Diskette Drive ON/OFF Control

DC voltages + 5 V and + 12 V are supplied by the PS type 2 to the dis (HDD) and diskette (FDD) drives, when the PS type 2 receives a 'Remote 1 On command' or 'Remote 2 ON command' from the MOSS through the PLC card.

If the disk and diskette drives have not been used within 15 minutes, the PS type 2 receives from the MOSS the 'Remote 1 OFF command' and 'Remote 2 OFF command', and DC voltages are no longer applied to the drives.



Disk Voltages and Tolerances (From PS Type 2)

Table 10-19. Disk Voltages and Tolerances (From PS Type 2)

VDC	Level	Vmin	Vmax	Ripple
+ 12.00	1	+ 10.80	+ 13.00	0.12 p-p
+ 12.00	2	+ 11.40	+ 12.60	0.10 p-p
+ 5.00	5	+ 4.75	+ 5.25	0.10 p-p

For DC test points, see pages YZ541 and YZ542.

Power Control Subsystem

Power Control Subsystem Functions

The power control subsystem has in charge the following functions:

- Reporting to the MOSS all faults in any power supply (except PS type 6 and PS type 8). The detection is performed by the power supply itself.

  If the MOSS is inoperative, the fault codes are displayed on the control panel, and up to eight fault codes will be stacked on the power supply. These codes will be sent to the MOSS at the next request.

- Powering the machine ON/OFF either in Local, Host or Network mode.
- Individual ON/OFF powering of each power supply for maintenance purposes (except PS type 6 and PS type 8). This command is issued through the MOSS except for the power ON/OFF dedicated to the power supply powering the MOSS. This last command will be issued through the control panel as the power On/OFF dedicated to that power supply.
- Power ON Reset (POR) function, the Start function (reset of the MOSS only), and the ability to ask any power supply to send a Power ON Reset signal to its dedicated subsystem.

  These three types of reset can be issued through the MOSS. The control panel doesn't have the ability to reset individually (except the MOSS).

- Time function, with the help of an local clock in order to give MOSS the local time and to allow the scheduled power ON function.
- Scheduled Power ON of the whole machine. This function is available only in Network mode.
- Sensing and reporting to the MOSS the status of the air-flow detectors of the machine.
- Communicating from the control panel to the MOSS and from the MOSS to the control panel.
- Main line survey in order to detect AC main failures.
- Automatic Restart function after an AC main failure.
- Diagnosing the power control subsystem and the control panel.
- Monitoring the Remote Power OFF signal coming from the CCUs.
- Monitoring the thermal sensors located in the TCM or the PUC card.

Power Control Data Flow

See Figure 10-3 on page 10-41.

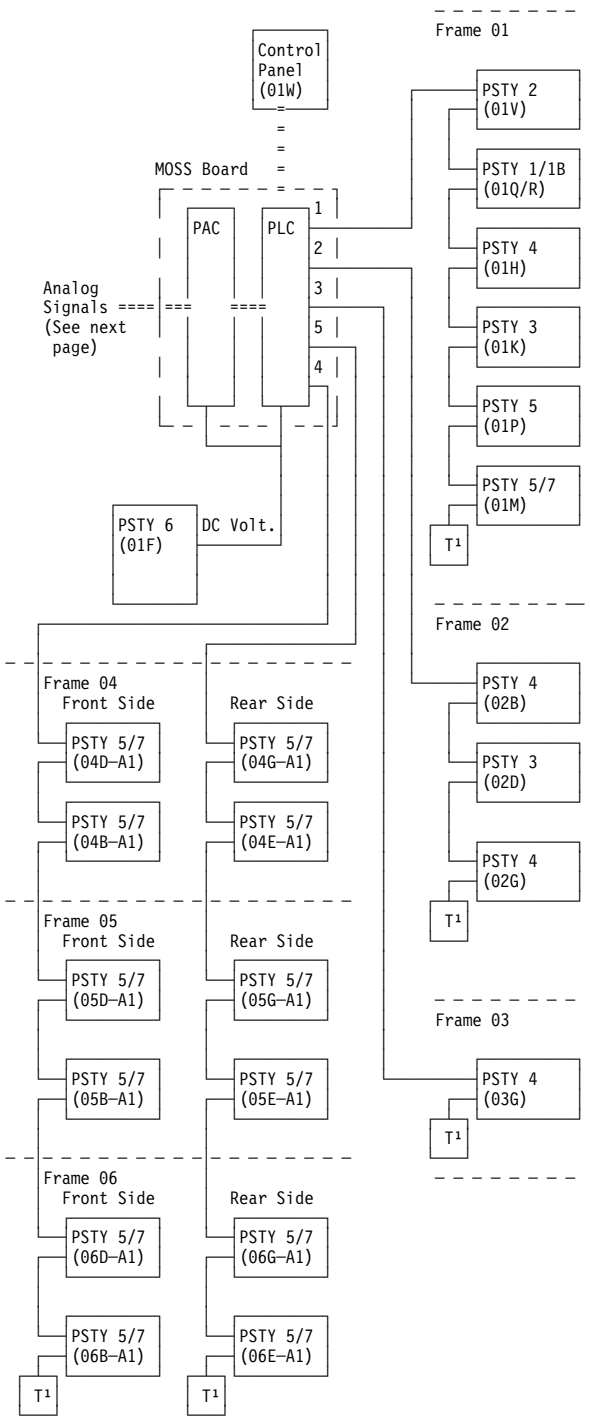
The power control subsystem is made of three parts:

1. The power control cards, which are plugged in the MOSS board:
   - A power logic card (PLC) to manage the whole power control subsystem.
   - A power analog card (PAC) to interface all the analog signals.
     See “Power Control Card Interconnection” on page 10-42 for details.
2. The power supplies.

3. The power control bus (PCB):
   This PCB is used to link the PLC to each power supply.

   Five buses are used:

   - Power bus 1 for base frame 01
   - Power bus 2 for frame 02
   - Power bus 3 for frame 03
   - Power bus 4 for the front side of frames 04, 05, and 06
   - Power bus 5 for the rear side of frames 04, 05, and 06.



1 = T stands for power bus terminator (PTER)

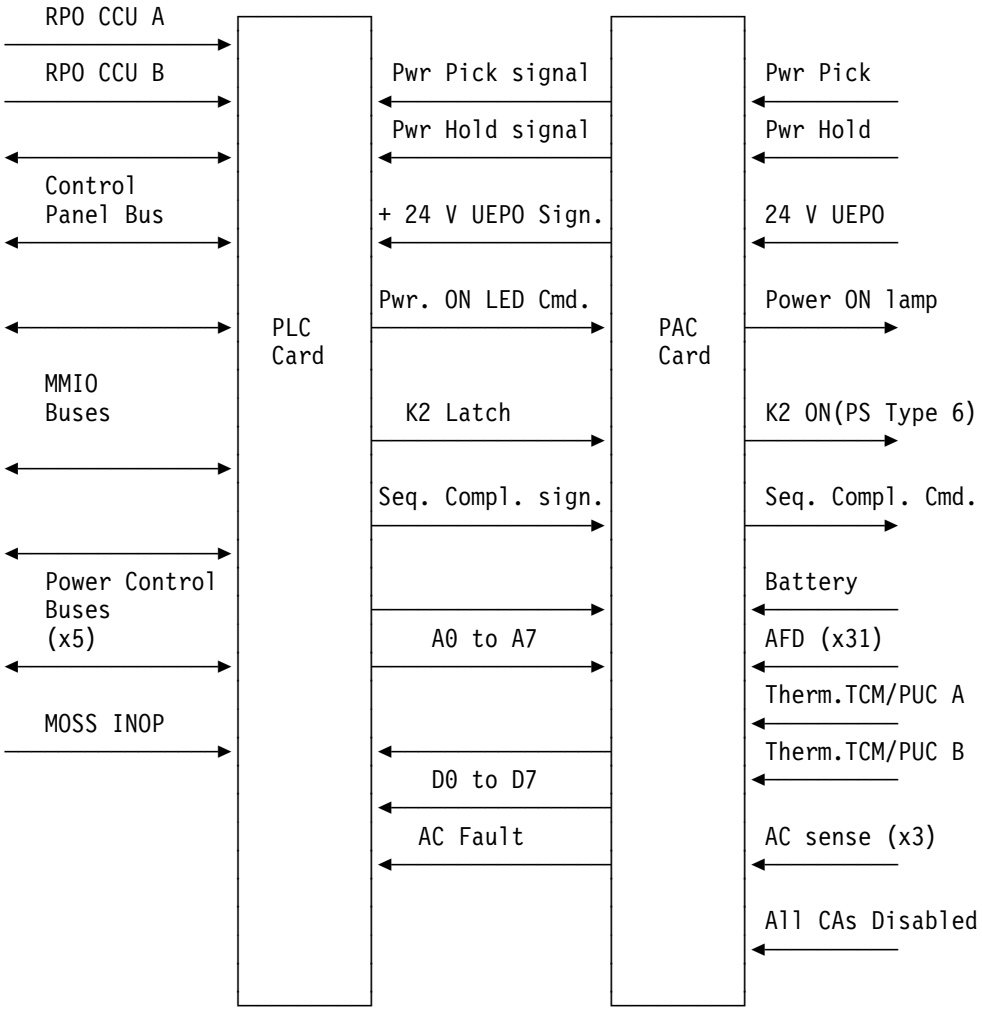
Figure 10-3. Power Control Subsystem Data Flow

Power Control

Power control is made of two cards plugged in the MOSS board:

- The PLC card is dedicated to the interconnection with the MOSS, the control panel and the power supplies.
- The PAC card is dedicated to the following:
  - Power Pick and Hold signals.
  - Sequence Complete signal.
  - AC fault signal.
  - Air flow detector outputs.
  - TCM or PUC temperature monitoring.
  - Relay K2 command.
  - UEPO sense.
  - Battery monitoring.

Power Control Card Interconnection



PLC PAC Interconnection

The PLC card generates the following signals to the PAC card for re-driving:

- Power ON indicator (to drive the indicator of the control panel).
- K2 Latch (to drive the machine's main contactor).
- Sequence Complete signal (to drive the Sequence Complete relay).

The PAC card generates the following signals to the PLC card:

- Power Pick signal (from primary power box).
- Power Hold signal (from primary power box).
- + 24 V UEPO signal (from UEPO Switch).
- AC Fault (generated from the 3 AC senses coming from PS type 6).

The PLC card receives the following signals from the MAC card:

- MOSS Inoperative.
- RPO CCU-A (re-driven from CCU-A).
- RPO CCU-B (re-driven from CCU-B).

The PAC card receives the following signal from the MAC card:

- All CAs disabled.

Power Mode of Operation

Local Mode

In local mode (3 at the power control window) the only way to power ON/OFF the 3745 is to do it manually from the control panel.
In this mode, for safety reasons, the Automatic Restart and the scheduled power ON functions are not available.
In this mode the Power ON Reset of the machine is available from the control panel.

Host Mode

In host mode (1 at the power control window) the only way to power ON/OFF the 3745 is to do it from the locally-attached hosts, via external control cables:
When any of these hosts goes ON, the 3745 powers ON with a power pick command.

When all attached hosts have turned OFF (all power hold dropped) the 3745 turns OFF.

In this mode, the Automatic Restart function is available.

Network Mode

In network mode (2 at the power control window) and only on this mode, the scheduled power ON function is available.
As for all the other communication controllers, in this mode you can power ON the 3745 manually from the control panel, and you can power OFF the 3745 through the NCP (RPO function, also called RMPO for VTAM).
The scheduled power ON function does not disable the manual power On or RPO functions. This means that you always have the ability to power ON the 3745 manually before the scheduled power ON time.

In this mode, the Automatic Restart function is available.
In this mode the Power ON Reset of the machine is available from the control panel.

Switching From One Mode to Another.

- Switching from Host or Network to Local does not impact the machine's Power ON/OFF status.
- Switching from Local to Host:
  If OFF in Local, the machine will be maintained OFF in Host. It will be turned ON later by a power pick pulse from one attached host (if an AC main utility fault occurs, the Automatic Restart function will not apply even if one attached host is ON).

  If ON in Local, the machine will remain ON if at least one attached host is ON. Otherwise, the machine will go OFF.

  An EPO plug Part 8482303 must be installed in position J1 if no host EPO cables are installed. This plug prevents powering OFF the 3745 if the power control is set to position 2 (network mode), when no EPO cables are installed.
- Switching from Local to Network:
  If OFF in Local, the machine will be maintained OFF in Network, waiting for a manual power ON at the control panel or for a scheduled power ON action. If an AC main utility fault occurs after switching from Local to Network, the machine being OFF, the Automatic Restart function will not apply.
  If ON in Local, the machine will be maintained ON in Network.
- Switching from Host to Network:
  The machine power ON/OFF status is not impacted.
- Switching from Network to Host:
  If OFF in Network, the machine will be maintained OFF in Host. It will be turned ON later by a power pick pulse from one attached host (if an AC main utility fault occurs, the Automatic Restart function will not be applied even if one attached Host is ON).
  If ON in Network, the machine will remain ON if at least one attached host is ON. Otherwise, the machine will go OFF.

Power ON/OFF Sequence

Power ON Sequence.

The normal power ON sequence is initiated by:

- Manual power ON at the control panel if the machine is in local or network mode.
- Power pick command (from one attached host) if the machine is in host mode.
- Automatic restart function on an AC main utility failure if the machine was powered ON in host or network mode when the failure occurred.
- Scheduled power ON function if the machine is in Network mode.

Each power supply will receive the power ON command from the PLC.

The first subsystem to be powered ON will be the MOSS, then the CCU(s), the channel adapters, then the scanners and last the LIC units of frame 01. Then frames 02 and 03 are powered ON, and finally frames 04, 05, and 06.

When the power supplies have successfully completed their power ON sequence, the power control resets their power ON reset (POR) signal after a 100 ms delay.

Then the MOSS disk and diskette are powered ON.

The MOSS will process the IML.

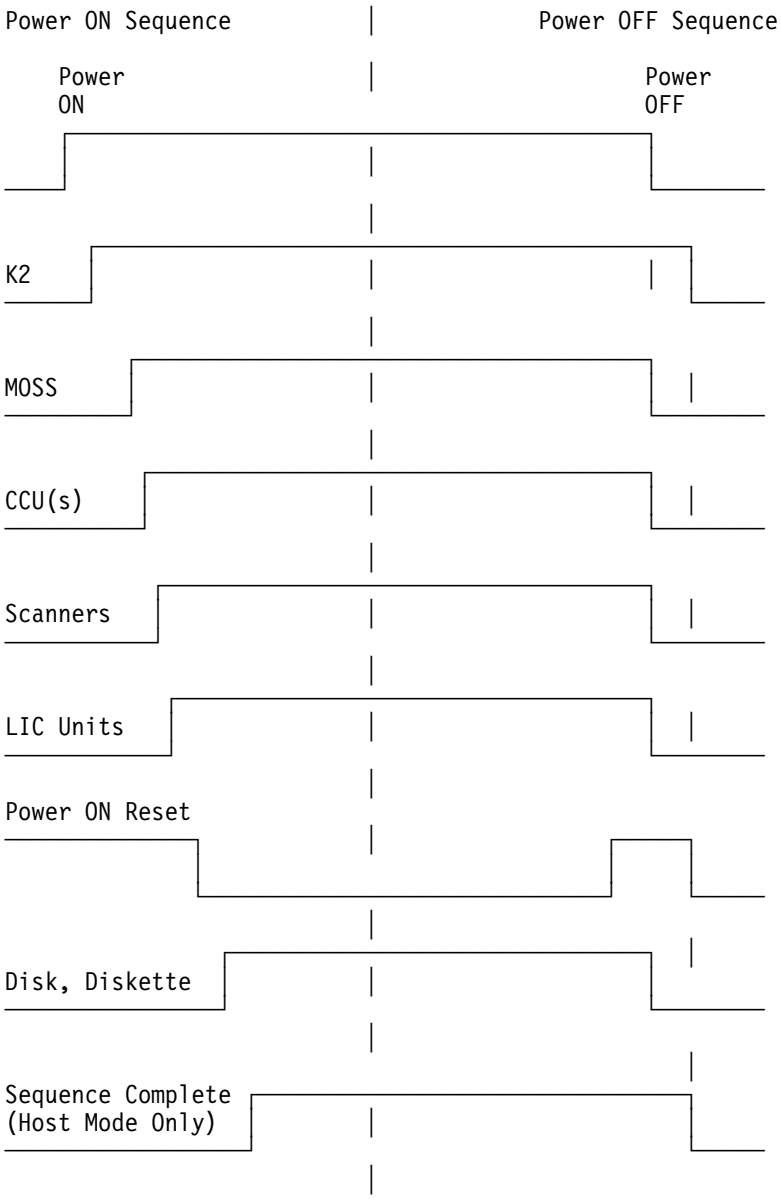
At the end of the Power ON sequence, and if the machine is in host mode, the sequence complete signal is sent to the host. When the machine is in local or network mode, this signal is forced permanently, whether the machine is power ON or OFF.

The power ON lamp on the control panel comes ON as soon as the K2 relay is ON.

Power OFF Sequence.

The normal Power OFF sequence is initiated by :

- Manual power OFF at the control panel if the machine is in local mode.
- The remote power OFF (RPO also called RMPO for VTAM) signal, if the machine is in network mode. A machine with two CCUs will be powered OFF when both RPOs are activated.
- The drop of the last host power hold signal if the machine is in host mode.



POR from Power Control

POR at Power ON

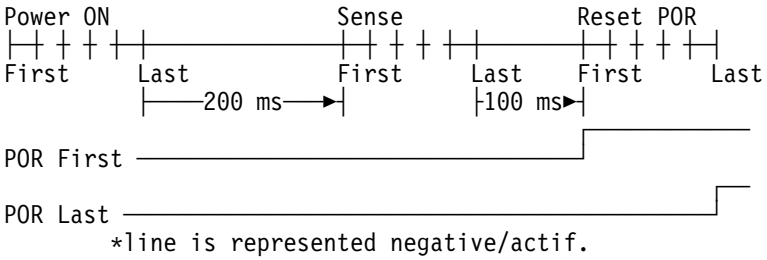
- All the power supplies are started following a sequence defined hereafter (if installed):

  1. MOSS (1)
  2. CCU's (2)
  3. Channels frame 01 (4)
  4. Scanners frame 01 (4)
  5. DMUX/SMUX/LICs frame 01 (2)
  6. Channels frame 02 (4)
  7. Scanners frame 02 (8)
  8. Scanners Frame 03 (4)
  9. DMUX/SMUX/LICs frame 04 (4)
  10. DMUX/SMUX/LICs frame 05 (4)
  11. DMUX/SMUX/LICs frame 06 (4)

  () = Number of power supply

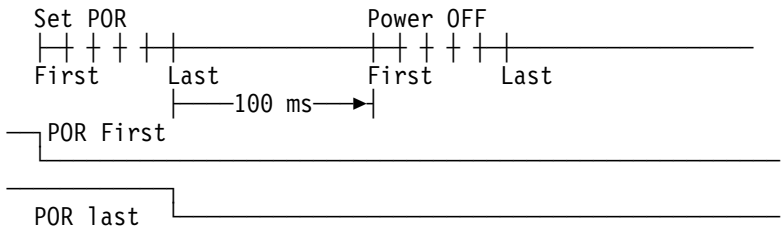
- 200 ms after the request on the last PS the status of the power box is asked in the same sequence.
- 100 ms later, the POR line is deactivated if the box is started, in the same sequence.
- Then the MOSS disk and diskette are powered ON (+5V, +12V). The hard disk needs some 20 s to be ready and the diskette some 2 s.

  The MOSS code will power OFF both of them, if not used during 15 minutes. The motor of the diskette will be turned OFF by the DFA if not used after 8 s.



POR at Power OFF

- All the power supplies are requested to activate the POR line in the defined sequence.
- 100 ms later, all the power supplies are requested to power OFF in the same sequence.



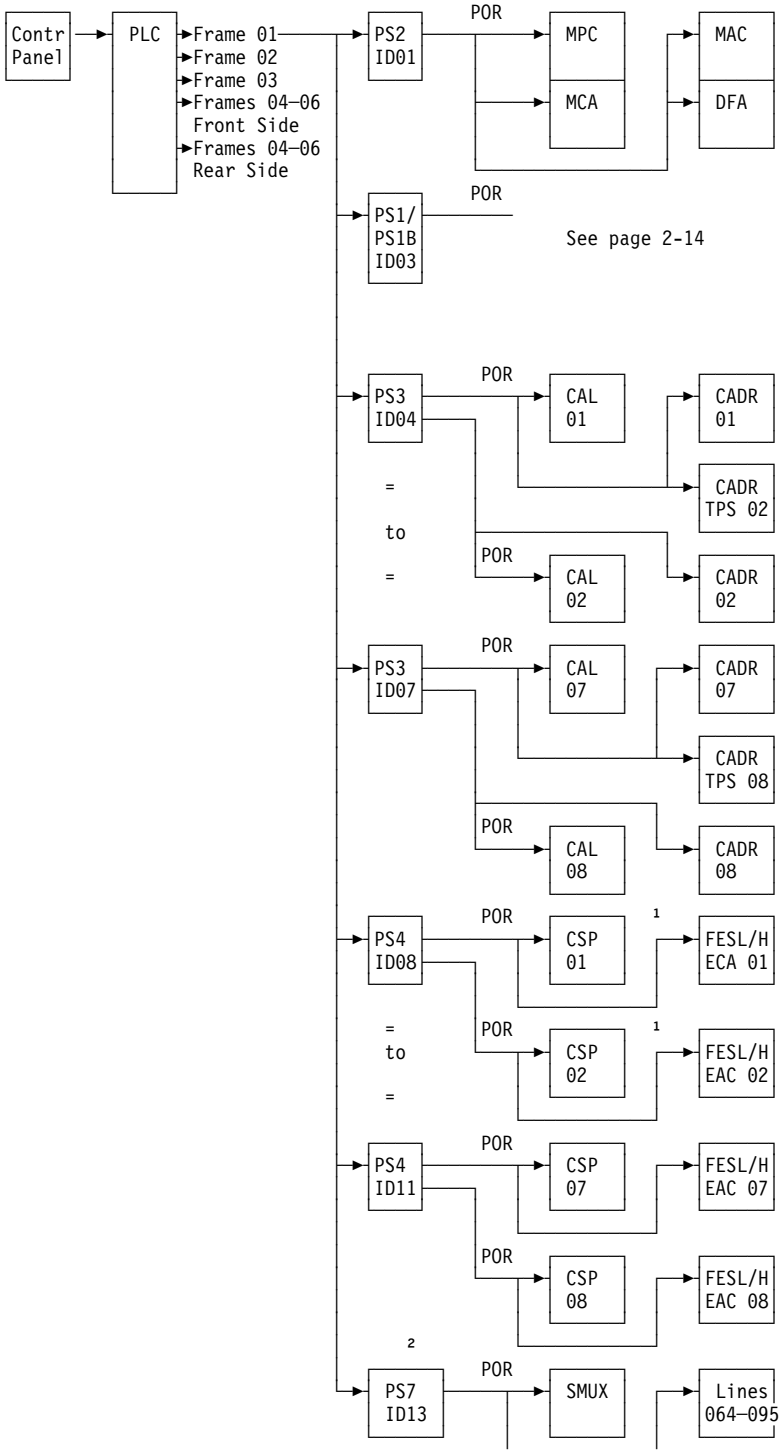
POR Principle

Figure 10-4. POR Principle

POR is always down level when active

Voltage level is provided by the user.

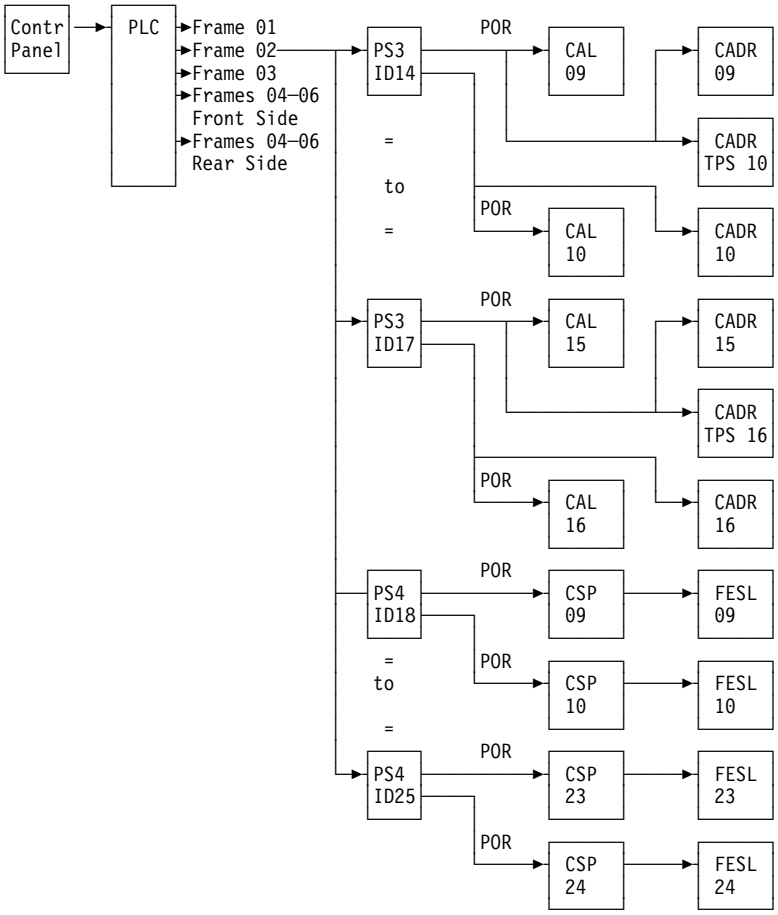
Power ON Reset Frame 01



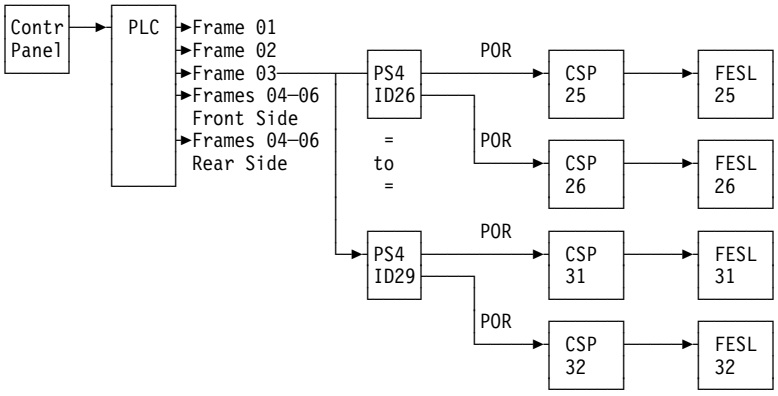
1 = or TRM in 1, 2, 5, 6 positions

2 = When a PS type 7 is powered OFF, the LAs connected to the corresponding SMUX must be IMLed.

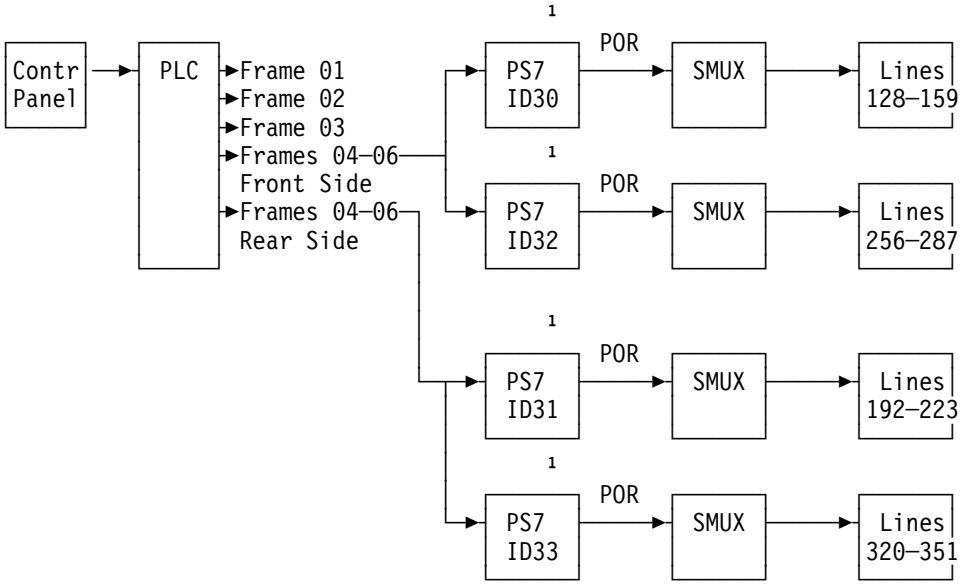
Power ON Reset Frame 02



Power ON Reset Frame 03

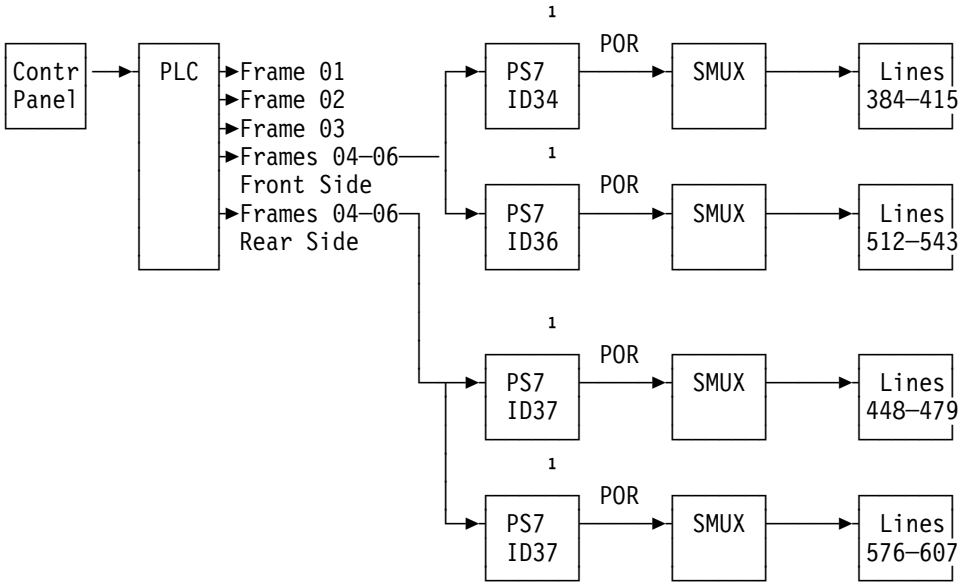


Power ON Reset Frame 04



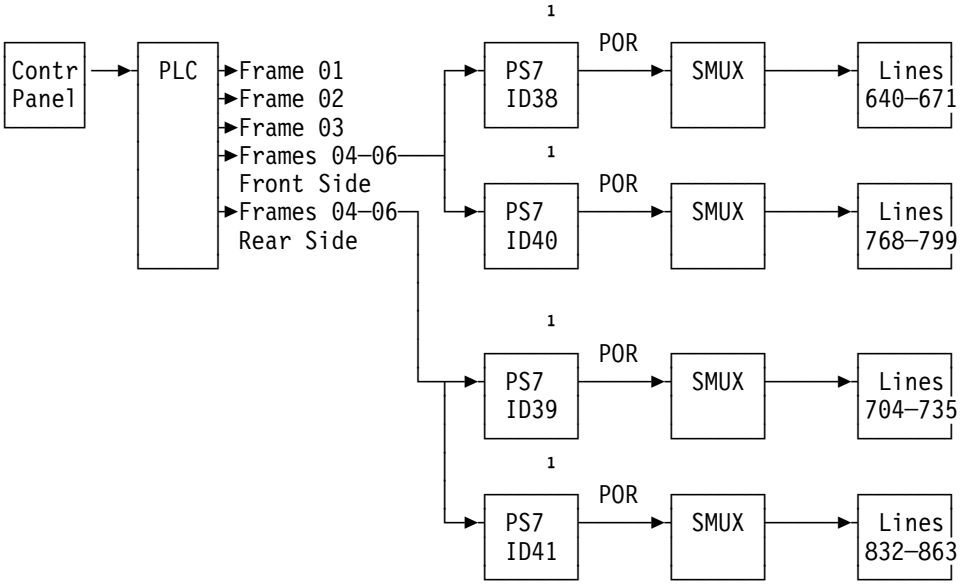
1 = When a PS type 7 is powered OFF, the LAs connected to the corresponding SMUX must be IMLed.

Power ON Reset Frame 05



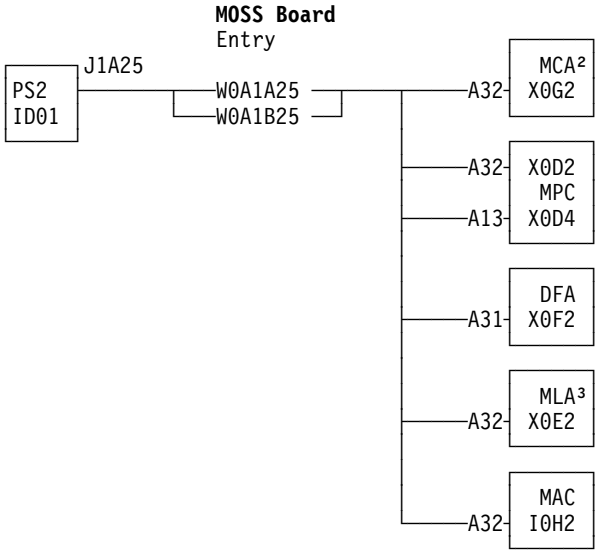
1 = When a PS type 7 is powered OFF, the LAs connected to the corresponding SMUX must be IMLed.

Power ON Reset Frame 06



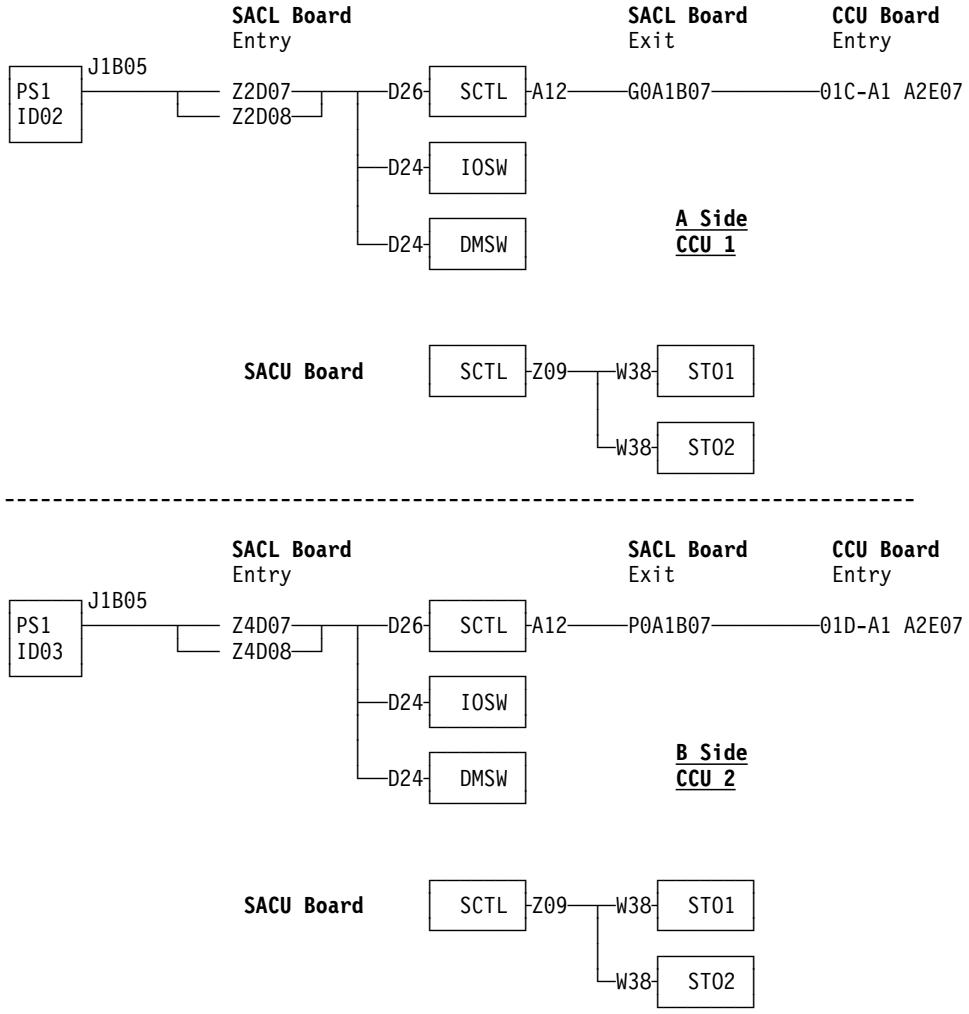
[1] = When a PS type 7 is powered OFF, the LAs connected to the corresponding SMUX must be IMLed.

MOSS Board POR Path

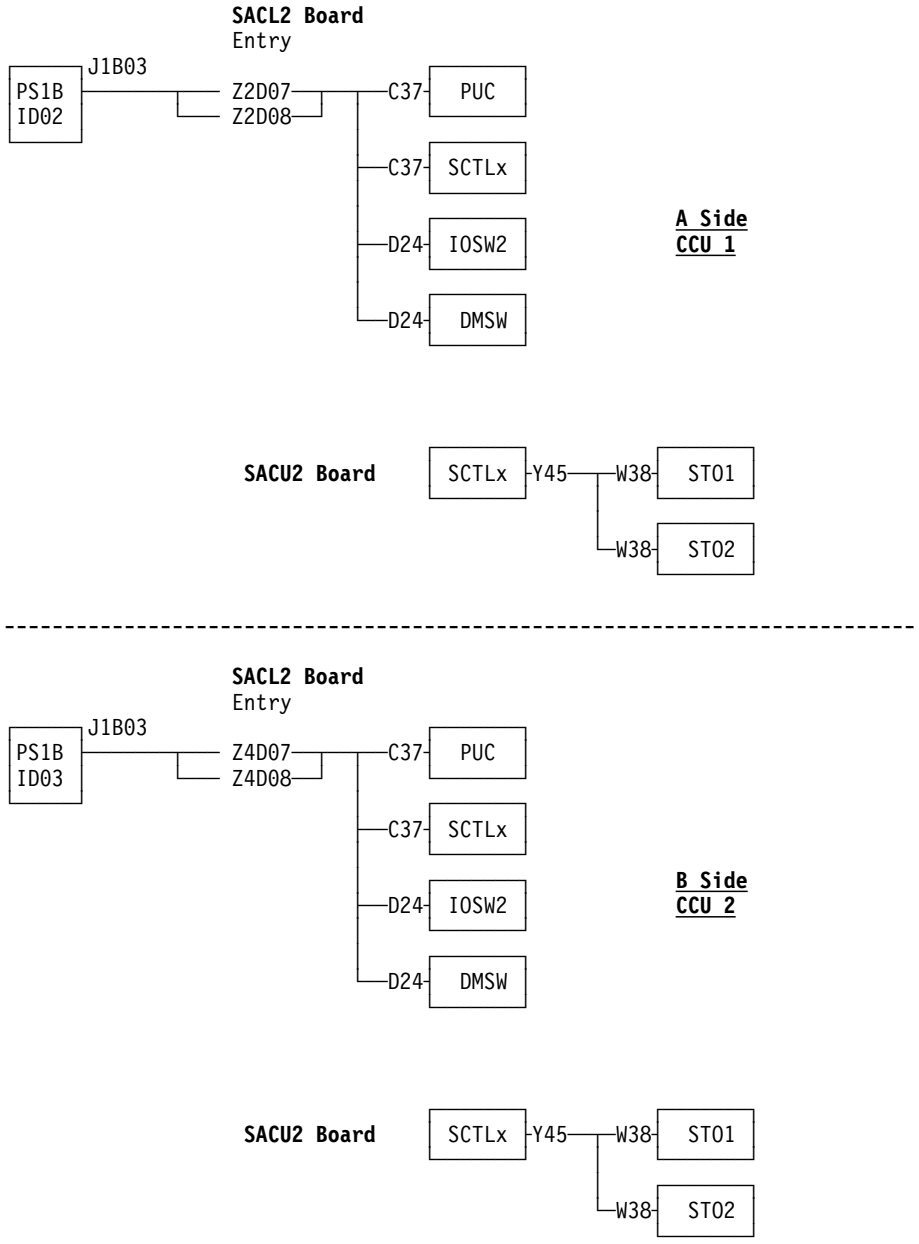


[2] = On 3745 Model 210-610
[3] = On 3745 Model 21A-61A

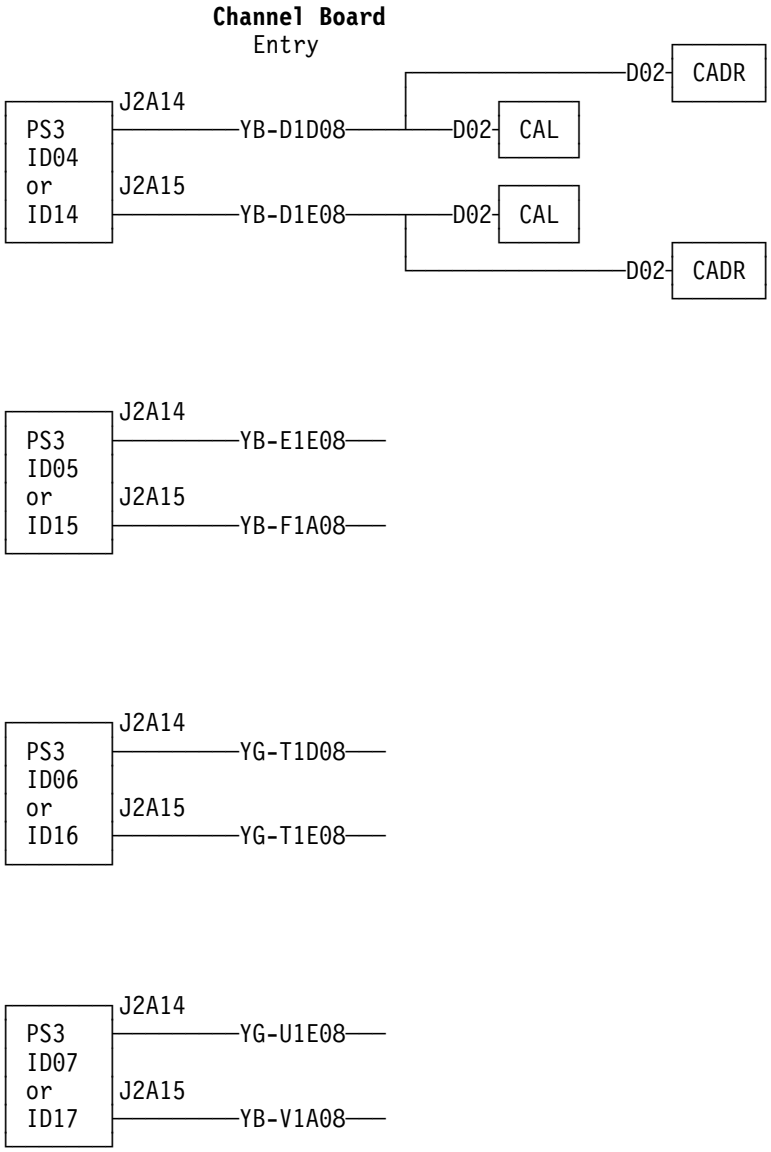
SACU/SACL/CCU Board POR Paths for Models 21x and 41x



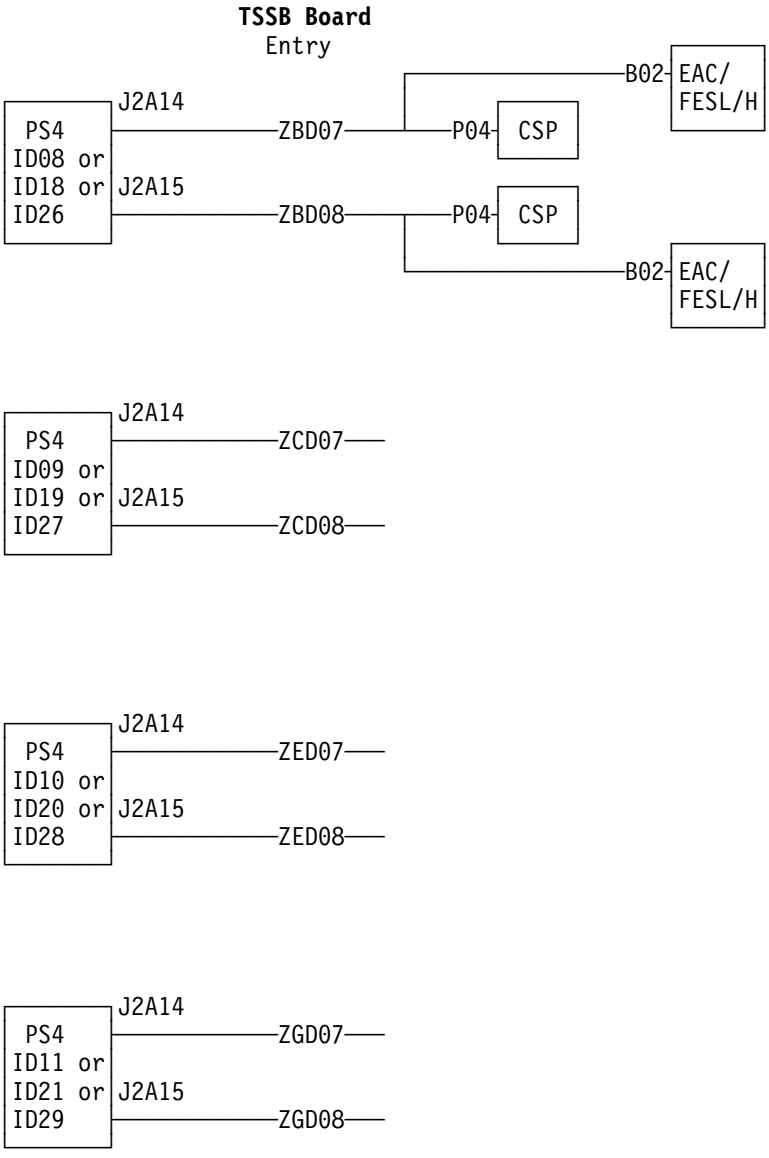
SACU2/SACL2 Board POR Paths for Models 31x and 61x



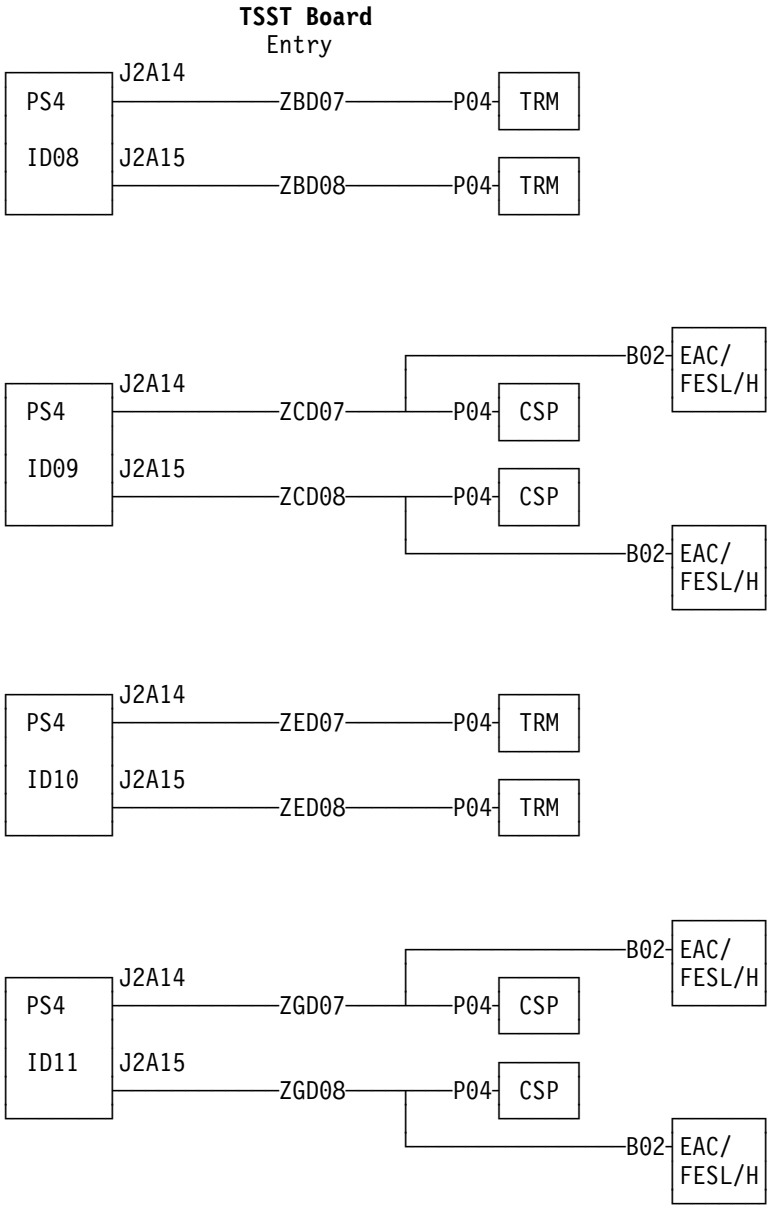
Channel Board POR Path



TSSB Board POR Path



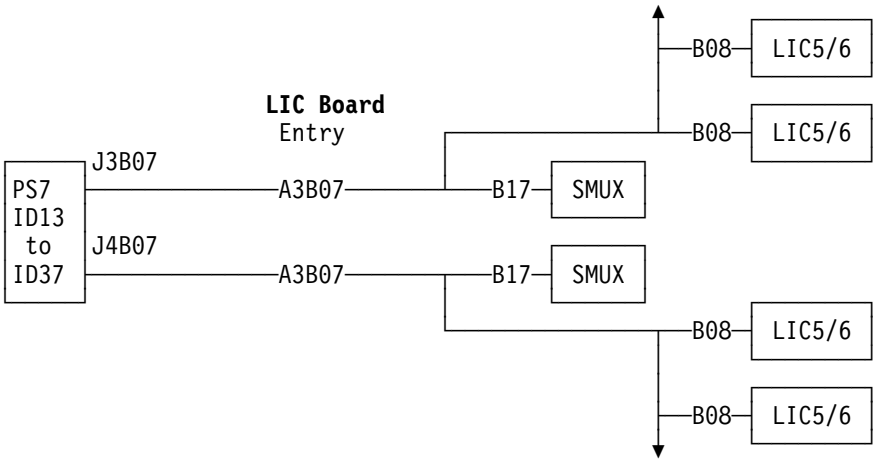
TSST Board POR Path



LIC Board Type 1 POR Pin Location

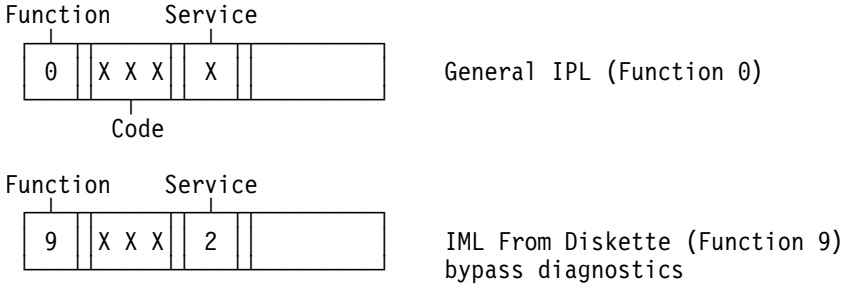
POR unused.

LIC Board Type 2 POR Path

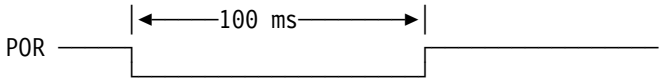


Machine Reset

- The machine being **Power ON** , a general reset is done ONLY with the following function and/or service displayed at the panel.



- Machine reset is started, when pushing 'Power ON/Reset' button, or if selecting the functions above as new function, by the 'validate' key.
- All the power supplies are requested to activate their POR line in the defined sequence.
- 100 ms later, all the power supplies are requested to deactivate the POR line, in the defined sequence.



- The Power ON reset function is also available for the MOSS code.

Scheduled Power ON Function

The purpose of the clock used in the power control subsystem is to keep time and calendar date through extended power OFF periods.
This is to allow scheduled power ON actions to be taken at a predetermined time and day of the week, independently of any intervening AC main power failures. Each day of the week may be associated with a different power ON time.

The logic for the scheduled power ON function is in the PLC card and is powered by a battery during AC main failures.

This function is available in Network mode (2 at power control window) only, and is allowed or inhibited by the customer through the MOSS.

Manual Power ON Versus Scheduled

Manual power ON or power OFF through the NCP has priority over scheduled power ON. If power OFF through NCP completes prior to a scheduled power ON point, then the power control subsystem will turn power ON when the predetermined point is reached.

The scheduled power ON times of the current week will be considered valid for the following weeks if they are not changed.

Automatic Restart Function.

For safety reasons, this function is not available in Local mode.
The automatic restart function intends to assure a re-power ON of the system when the AC main is restored within a certain limit of time after a failure.

If one AC main transient fault is detected, the following message will be sent to the MOSS (if the power supply of the MOSS is still operative):

An AC main power failure occurred at MM/DD/YY HH-MM.

The information will be stocked in the PLC card if the MOSS is inoperative.
When the AC main is restored, a machine auto-restart will take place if the AC main fault has resulted in a machine power OFF.

AC Detection and AC Monitoring

Main Line Survey

Major disturbances are defined as follows:

A 30 % or more dip in the minimum nominal voltage on any one phase while the others are within the specified operating range, with 100 milliseconds minimum duration.

An AC sense line for each phase is sent from PS type 6 (see page YZ576) to the PAC card.

In case of major disturbance, an AC fault is send by the PAC card to the PLC card.

A BER is logged in the MOSS to indicate an AC failure.

Two cases of AC failure may occur:

1. Short AC failure:
   For some short AC failures the machine may not be totally powered OFF (not all power supplies are powered OFF).
   No power ON retry is done on the power supply fault detection, the faults are logged in the PLC card and sent to the MOSS when operative.

   In that case, at the next machine power ON (manual or auto-restart) the faulty power supplies will remain OFF.

2. Long AC failure:
   The machine is completely powered OFF (all power supplies are powered OFF).
   In that case, at the next machine power ON (manual or auto-restart) the power supplies which were ON before the machine power OFF will power ON. The power supplies which were OFF before the machine power OFF will remain OFF.

See “Power Control Card Interconnection” on page 10-42 for details on AC sense connection to the PAC card.

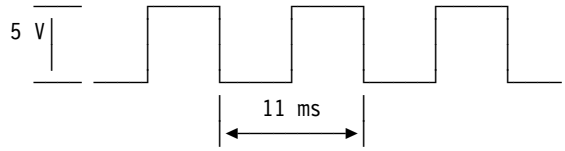
Air Flow Detector

On the 3745 the blowers have a speed detection (hall-effect cell) for the air flow detection.

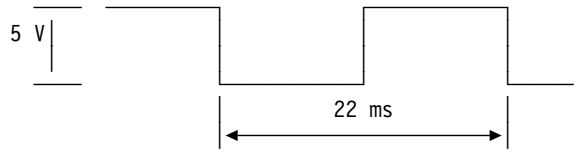
The hall-effect cell sends a signal to the PAC card.
If the PAC senses an air flow detector (AFD) fault, the identification of the faulty blower is sent to the MOSS through the PLC card.

Hall-Effect Cell Output

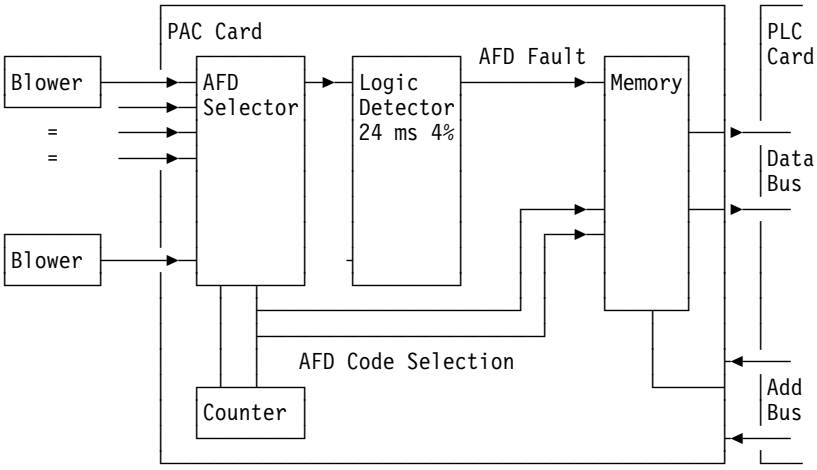
Blower locations: 01J-B1 and B2, 02C-B1 and B2, 02H-B1 and B2, 03H-B1 and B2.



Blower locations: 01A-Z0, 01N-A0, 04C-A0, 04F-A0, 05C-A0, 05F-A0, 06C A0, and 06F A0.



Air Flow Detection Principle



Blower Fault Handling

1. The MOSS is operational

   - LIC blowers, blowers for LUI1 (LIC 1, 3, and 4):
     When one or more blowers are faulty, an alarm is generated and a BER is logged.
   - LIC blowers, blowers for LUI2 (LIC 5 and 6):
     When the first blower of the blower box is faulty, an alarm is generated and a BER is logged.
     When the second blower of the blower box is faulty, an alarm is generated, a BER is logged, and after two minutes the associated power supply (PSTY7) is powered OFF.
   - CA and LA blowers:

     When one blower is faulty, an alarm is generated and a BER is logged.

     When two or more blowers are faulty, an alarm is generated, a BER is logged, and after two minutes, the associated power supplies are powered OFF.
   - MOSS blower:
     The MOSS is powered OFF and code 030 is displayed on the control panel.

     At the next MOSS IML, an alarm is generated and a BER is logged.
   - CCU(s) blower:
     See “TCM Alarm Detection on Models 21x and 41x” on page 10-65 or “PUC Alarm Detection on Models 31x and 61x” on page 10-65 for details.

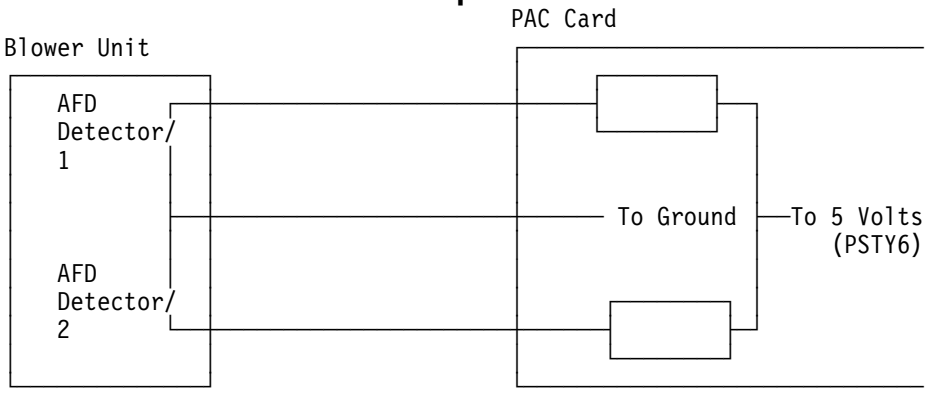
2. The MOSS is not operational

   For the LIC, LA, and CA blowers at the first blower fault:

   - A code is displayed on the control panel. For code meaning see the *MIP* Appendix A: "Control Panel Codes Definition".
   - The associated power supplies are powered OFF.
   - At the next MOSS IML, an alarm is generated and a BER is logged.

Note: After a blower fault, once the power supplies are powered OFF, is it not possible to turn these power supplies ON through the MOSS before the faulty blower is repaired.

AFD Detector Connection Principle



Blower and AFD Identification (ID)

Blower/AFD ID		Blower Location	AFD Connection	
Decimal	Hexadecimal (From BER)		Frame	MOSS
01–02	01–02	01J B1	01J–A0 J6	01A–W0 B3
03–04	03–04	01J B2	01J–A0 J7	01A–W0 B3
05–06	05–06	02H B1	02H–A0 J6	01A–W0 A4
07–08	07–08	02H B2	02H–A0 J7	01A–W0 A4
09–10	09–0A	02C B1	02C–A0 J6	01A–W0 C3
11–12	0B–0C	02C B2	02C–A0 J7	01A–W0 C3
13–14	0D–0E	03H B1	03H–A0 J6	01A–W0 B4
15–16	0F–10	03H B2	03H–A0 J7	01A–W0 B4
17	11	01A Z0	01E–A1 TB3	01A–W0 C4
18–19	12–13	01N A0	01Z–A0 J4	01A–W0 B3
20–21	14–15	04C A0	04A–A0 J7	01A–Y0 A6
22–23	16–17	04F A0	04A–A0 J11	01A–Y0 A6
24–25	18–19	05C A0	05A–A0 J7	01A–Y0 A6
26–27	1A–1B	05F A0	05A–A0 J11	01A–Y0 A6
28–29	1C–1D	06C A0	06A–A0 J7	01A–Y0 A6
30–31	1E–1F	06F A0	06A–A0 J11	01A–Y0 A6

For details on blower and AFD connection, see pages YZ551 to YZ556.

TCM Alarm Detection on Models 21x and 41x

This circuit scans the temperature of the two TCMs, and powers the CCU OFF (CCU A or B) in case of overheating.
This function is performed with the help of a thermal resistor included inside the TCM connected to the PAC card.

This circuit can also warn the PAC card in case the thermal resistor short-circuits or opens.

The thermistor is a resistor whose value grows as the temperature lowers, its reference value is given at 64° Celsius: 100 K Ohms with an accuracy of ± 2%.

Two thresholds are defined:

1. First alert at 70° Celsius.
   - If the TCM temperature goes over this level, the power control requests a BER 04 05 to be logged, with an alert/alarm 95.
   - If the TCM temperature returns under this level, the power control requests a BER 04 06 to be logged, with an alert/alarm 98.
2. Second alert at 75° Celsius.

   If the TCM temperature goes over this level, the PS type 1 corresponding to this TCM is powered OFF, and the power control requests a BER 04 07 to be logged, with an alarm 99.

See “Power Control Card Interconnection” on page 10-42 for details on thermal TCM A/B connection to the PAC card.

PUC Alarm Detection on Models 31x and 61x

This circuit scans the temperature of the two PUC cards, and powers the CCU OFF (CCU A or B) in case of overheating.
This function is performed with the help of two thermal resistors included inside the PUC card connected to the PAC card.

This circuit can also warn the PAC card in case the thermal resistor short-circuits or opens.

The thermistors are resistors whose value grows as the temperature lowers, their reference value is given at 64° Celsius: 100 K Ohm with an accuracy of ± 5%.

Two thresholds are defined:

1. First alert at 70° Celsius.
   - If the PUC temperature goes over this level, the power control requests a BER 04 05 to be logged, with an alert/alarm 95.
   - If the PUC temperature returns under this level, the power control requests a BER 04 06 to be logged, with an alert/alarm 98.
2. Second alert at 75° Celsius.

   If the PUC temperature goes over this level, the PS type 1 corresponding to this PUC is powered OFF, and the power control requests a BER 04 07 to be logged, with an alarm 99.

See “Power Control Card Interconnection” on page 10-42 for details on thermal PUC A/B connection to the PAC card.

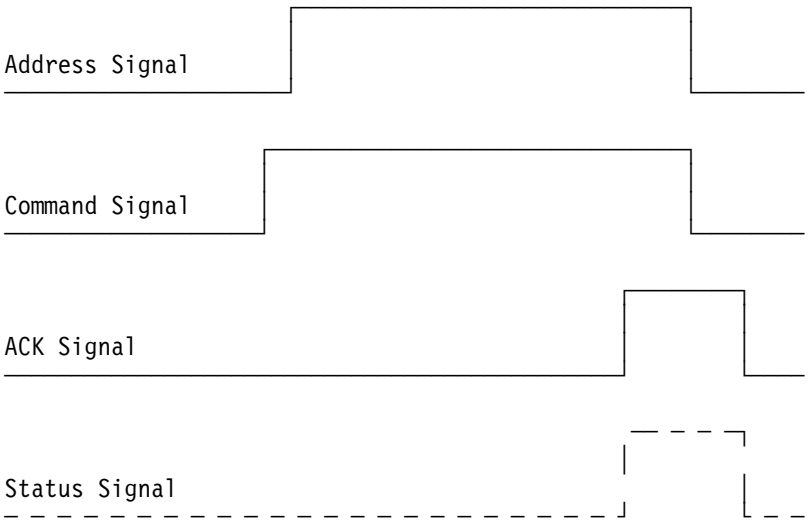
Power Control Bus

Principle

The power control bus links the PLC card to all the PSs.
Commands from the PLC card to any PS, or status from any PS to the PLC are transferred through this power control bus.

Thirteen signal wires are used:

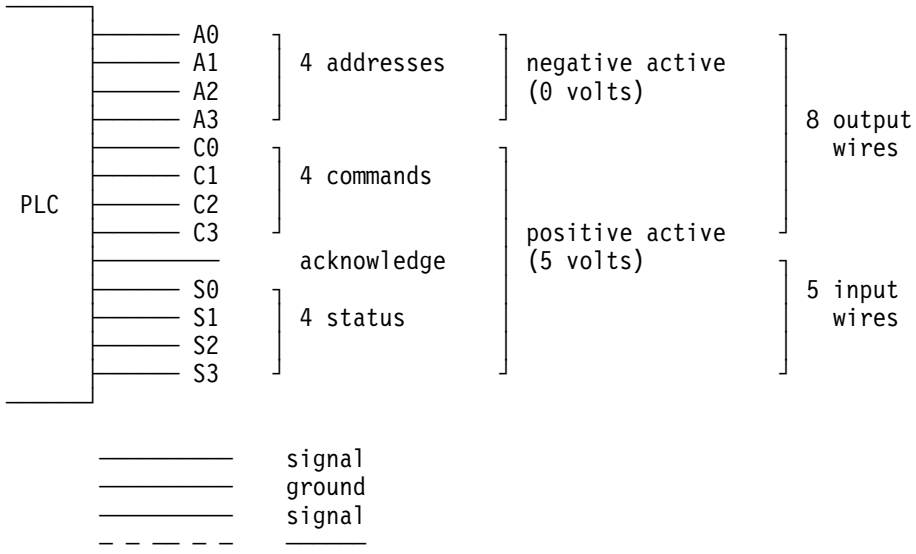
- Four wires for the Address signal (from the PLC card to a PS).
- Four wires for the Command signal (from the PLC card to a PS).
- One wire for the ACK signal (from the PS to the PLC card).
- Four wires for the Status signal (from the PS to the PLC card).



Power Control Bus Test

The power bus is made of 13 signal wires, each one shielded to ground.

All output wires from PLC card are connected to ground through 82-Ohm terminator resistors.



Type of failure detected :

- Short circuit on a signal wire
- Open circuit on a signal wire
- Driver or receiver forcing a low or high level

The test sends alternating patterns on the bus and verifies if the received patterns alternate.

Bus levels are NPL levels (0/5 volts).

Power Supply Polling

In order to obtain the status of the power supplies, the PAC will poll the power supplies continuously, via the power control bus.

The sequence will be:

1. Send the "Check" command to the power supply.
2. Receive the returned code from the power supply.
3. If the PAC does not receive the power supply acknowledge signal, the status of the corresponding power supply becomes "No Reply".
   If the PAC does not receive the Address code as answer, the status of the corresponding power supply becomes "Interconnection KO".
   If the PAC receives the Address code as an answer, it asks the power supply to send the power supply status.
4. If the returned code is "Power ON", exit.
   If the returned code is a "Power Fault", send the corresponding BER to the MOSS and exit.

if the returned code is other than "Power ON", the power supply will be considered failing and the corresponding BER will be sent to the MOSS.
For corresponding codes, see Chapter 12, “Error Logging” on page 12-1.

The errors that can be detected on each power supply are:

- Over-current on one secondary output (one code per power supply).
- Over-voltage/Under-voltage on one secondary output (one code per power supply).

Fault Detection

When a power supply is found faulty during the polling operation, if this power supply was previously ON in the PLC tables:

1. The PLC tables are updated.
2. The information is sent to the MOSS when operative.
3. Power ON retry is not done.
4. At the next machine power ON (manual or auto-restart) the power supplies which were OFF before the machine power OFF will remain OFF.

The Address Signal

An address is used to select one power supply among those connected to the bus.

The Address signal uses 4 wires.
The four bits used for the Address signal are called A0, A1, A2 and A3.

As it is possible to have the same type of power supply used several times on the same bus, each power supply must have a way to know its own address from the external world, this address is called Address Init.

Each power supply connected to the same bus, must have an Address Init unique and different from the Address Init of any other power supply connected to the same bus. One bus is limited to fourteen power supplies.

For PS type 1 or 1B, a switch SW1 is set to 0 or A if the PS is for CCU-A, and to 1 or B if the PS is for CCU-B. See “PS Type 1 Component Locations” on page 10-10 for PS type 1 details, or “PS Type 1B Component Locations” on page 10-13 for PS type 1B details.

For PS type 3, the PS address is given by the printed wires on the power board.

For PS type 4, a jumper may be installed on the left side of the power receptacle board. See page YZ035 for details.

For PS type 5, a switch (SW1) is used to set the address. See “PS Type 5 Component Locations” on page 10-28 for details.

Table 10-20 (Page 1 of 2). Power Supply Addressing

Frame	PS Type	Location	Address Init				PS ID
			A3	A2	A1	A0	
Frame 01	2	01V	1	1	1	0	01
	1/1B	01Q	1	1	0	0	02
	1/1B	01R	1	1	0	1	03
	3	01K A1	1	0	0	0	04
	3	01K B1	1	0	0	1	05
	3	01K C1	1	0	1	0	06
	3	01K D1	1	0	1	1	07
	4	01H A1	0	1	0	0	08
	4	01H B1	0	1	0	1	09
	4	01H C1	0	1	1	0	10
	4	01H D1	0	1	1	1	11
	5	01P A1	0	0	0	0	12
	5	01M A1	0	0	1	0	13
	7	01M A1	0	0	1	1	13
Frame 02	3	02D A1	1	0	0	0	14
	3	02D B1	1	0	0	1	15
	3	02D C1	1	0	1	0	16
	3	02D D1	1	0	1	1	17
	4	02B A1	0	1	0	0	18
	4	02B B1	0	1	0	1	19
	4	02B C1	0	1	1	0	20
	4	02D D1	0	1	1	1	21
	4	02G A1	0	0	0	0	22
	4	02G B1	0	0	0	1	23
	4	02G C1	0	0	1	0	24
	4	02G D1	0	0	1	1	25
Frame 03	4	03G A1	0	1	0	0	26
	4	03G B1	0	1	0	1	27
	4	03G C1	0	1	1	0	28
	4	03G D1	0	1	1	1	29

Table 10-20 (Page 2 of 2). Power Supply Addressing

Frame	PS Type	Location	Address Init				PS ID
			A3	A2	A1	A0	
Frame 04	5	04D A1	0	0	0	0	30
	5	04G A1	0	0	0	0	31
	5	04B A1	0	0	0	1	32
	5	04E A1	0	0	0	1	33
	7	04D A1	1	0	0	0	30
	7	04G A1	1	0	0	0	31
	7	04B A1	1	0	0	1	32
	7	04E A1	1	0	0	1	33
Frame 05	5	05D A1	0	0	1	0	34
	5	05G A1	0	0	1	0	35
	5	05B A1	0	0	1	1	36
	5	05E A1	0	0	1	1	37
	7	05D A1	1	0	1	0	34
	7	05G A1	1	0	1	0	35
	7	05B A1	1	0	1	1	36
	7	05E A1	1	0	1	1	37
Frame 06	5	06D A1	0	1	0	0	38
	5	06G A1	0	1	0	0	39
	5	06B A1	0	1	0	1	40
	5	06E A1	0	1	0	1	41
	7	06D A1	1	1	0	0	38
	7	06G A1	1	1	0	0	39
	7	06B A1	1	1	0	1	40
	7	06E A1	1	1	0	1	41

The Command Signal

To send a command to a power supply selected by the Address signal, the Command signal is used.

The Command signal uses 4 wires. The four bits used for the Command signal are called C0, C1, C2 and C3.

See Table 10-21 on page 10-71 for details.

The Address and the Command signals are sent at the same time to the power supplies connected to the bus. Each power supply decodes the Address signal and only the power supply that has the Address INIT equal to the Address signal will decode the Command signal and process the requested action.

Table 10-21. Command Signal	
C3 C2 C1 C0	**Command Signal Name**
0 0 0 1	Check
0 0 1 0	Remote 2 ON
0 0 1 1	Remote 2 OFF
0 1 0 0	Power ON
0 1 0 1	Power OFF
0 1 1 0	POR 2 Set
0 1 1 1	POR 2 Reset
1 0 0 0	Remote 1 ON
1 0 0 1	Remote 1 OFF
1 0 1 0	POR 1 Set
1 0 1 1	POR 1 Reset
1 1 0 0	Status Request

Power ON Command:
The Power ON command initiates a power ON sequence of the PS if it was previously deactivated. If the PS is active, this command does not impact the status of the PS.

A power ON sequence for a PS consists in raising the secondary outputs till they reach their operating limits. The POR outputs of the PS stay at their active level (low level).

A PS is considered active as long as its secondary outputs are in their operating limits.

A PS is considered deactivated when its secondary outputs are at the zero volt level due to a normal power OFF sequence or a fault detection.
When the PS is deactivated, the POR outputs must be at their active level (low level) and the secondary outputs dedicated to Remote 1 or 2 commands must be at the zero volt level.

Power OFF Command:
The Power OFF command initiates a power OFF sequence of the PS if it was previously ON.

If the PS is OFF the Power OFF command does not impact the Status of the PS.

A power OFF sequence for a PS consists in dropping the secondary outputs till they reach the zero volt level (including the secondary outputs dedicated to Remote commands 1 and 2).

Remote 1 ON Command: (See [1])
The Remote 1 ON command raises the secondary outputs dedicated to the Remote 1 command until they reach their operating limits.

This command is operative only if the PS is ON.

Remote 1 OFF Command: (See [1])
The Remote 1 OFF command shuts the secondary outputs dedicated to the Remote 1 command down, until they reach the zero volt level.

This command is operative only if the PS is ON with the secondary outputs dedicated to the Remote 1 command in their operative limits. In any other case, this command does not impact the status of the PS.

Remote 2 ON Command: (See [2])
The Remote 2 ON command raises the secondary outputs dedicated to the Remote 2 command until they reach their operating limits.

This command is operative only if the PS is ON. In any other case, this command does not impact the status of the PS.

Remote 2 OFF Command: (See [2])
The Remote 2 OFF command shuts the secondary outputs dedicated to the Remote 2 command down, until they reach the zero volt level.

This command is operative only if the PS is ON with the secondary outputs dedicated to the Remote 2 command in their operating limits. In any other case, this command does not impact the status of the PS.

Status Request Command:
The Status Request command will result in sending on the bus the Status signal corresponding to the status of the PS.

This Status Request command is valid at any time when the PS is connected to the AC input.

POR 1 Set Command:
The POR 1 Set command sets the POR 1 output of the PS at its active level (low level).

This command is valid only if the PS is ON with its POR 1 output signal at the inactive level (high level). In any other case, this command does not impact the status of the PS.

POR 1 Reset Command:
The POR 1 Reset command set the POR 1 output of the PS to its inactive level (high level).

This command is valid only if the PS is ON with its POR 1 output signal at the active level (low level). In any other case, this command does not impact the status of the PS.

---

1 Applies only to PS type 2 (MOSS for disk/diskette power ON/OFF control).

2 Only applies to PS type 2 (MOSS for disk/diskette power ON/OFF control).

POR 2 Set Command:
The POR 2 Set command set the POR 2 output of the PS to its active level (low level).

This command is valid only if the PS is ON with its POR 2 output signal at the inactive level (high level). In any other case, this command does not impact the status of the PS.

POR 2 Reset Command:
The POR 2 Reset command set the POR 2 output of the PS to its inactive level (high level).

This command is valid only if the PS is ON with its POR 2 output signal at the active level (low level). In any other case, this command does not impact the status of the PS.

Check Command:
The Check command will result in sending on the bus the Status signal corresponding to the Address INIT of the PS.

This Check command is valid at any time when the PS is connected to the AC input.

The ACK Signal:
The ACK signal is generated by the PS having its Address INIT equal to the Address signal of the bus, after the decoding of the Command signal, if this command is valid.

This ACK signal informs the PLC card that the Command signal has been preceded by the PS. It is also used as a Data Valid signal for the Status signal if the Command sent initiates an answer from the PS.

Status Signal

Some commands received by the PS (Status Request, Check) will result in sending from the PS a status signal to the PLC CARD as an answer.

The status signal uses 4 wires. The four bits used for the status signal are called S0, S1, S2 and S3.

See Table 10-22 for details.

Table 10-22. Status Signal

S3 S2 S1 S0	Status Signal Name
0 1 1 0	Power Supply Fault
0 1 1 1	Overcurrent Fault
1 1 0 0	Power Down
1 1 0 1	Power Up
Address Init	Check OK

Power Up Status:
The Power Up status of the PS indicates that the secondary outputs of the PS (except those dedicated to the Remote 1 and 2 commands), are above the under-

voltage detection limits and under the over-voltage detection limits whatever the levels of the POR outputs (active or inactive level).

Power Down Status:
The Power Down status of the PS indicates that the secondary outputs of the PS (including those dedicated to the Remote 1 and 2 commands) are at the zero volt level, due to a Power OFF Sequence of the PS as response to a Power OFF command previously received.

Overcurrent Fault Status:
The Overcurrent Fault Status of the PS indicates that one of the secondary outputs of the PS (including those dedicated to the Remote 1 and 2 commands) has reached its over-current limit.

Power Supply Fault Status:
The Power Supply Fault Status of the PS indicates that one of the secondary outputs of the PS (including those dedicated to the Remote 1 and 2 commands) has reached its over-voltage or under-voltage limit.

Check OK Status:
The Check OK status is the requested answer of the PS receiving the Check Command.

Power Configuration Table

Using the *Service Functions,* the "Power Services (POS)" function can be selected from the console.

This function allows to:

- Display the power supply information:
  - PS identification
  - Corresponding PS status
  - Corresponding subsystem attached
- Power ON or OFF a power supply.
- Recreate the power configuration table.
- Acknowledge a change in the air filters or battery.

3746 Model 900 Power Connection and Control

For details on 3745/3746-900 power connection, power control to the 3746-900, and information on the 3746-900 power, refer to the *3746 Model 900 Hardware Maintenance Reference*, online documentation.

Maintenance

The machine being OFF, the PLC and PAC cards can be changed after setting the main CB1 OFF.

The machine being ON, the PLC and PAC cards can be changed with the help of the Maintenance Switches (SW1 and SW2), located in the primary power box.
See page YZ076 for location.

See *MIP* Chapter 5 for how to use these switches for PLC and PAC card exchange procedures.

Maintenance inside all power supplies is prohibited.

Power Control Bus Test

The power control bus test function is provided to check the integrity of the interface between the PLC card and the power supplies.

This function is dedicated to CE use only.

When the power control subsystem loses the control of a power supply due to interconnection problems, a BER is logged by the MOSS.
Based on this information, the CE might have to check the power control bus.

This test is available, the machine being power ON or OFF, and will not impact the power supply status. It doesn't stop the cooling and temperature monitoring.

The patterns, depending on the CE's choice made at the control panel, will be sent on the bus till the next action on the control panel (this allows scoping on the wrap-block tool). During the test, the PLC stops looking after the PS.

The result of the test, Test OK (004), or not OK (005), is displayed on the control panel by means of a code.

Using a "step by step" methodology, the CE will be able to isolate the faulty FRU (PLC card, power supply, power control bus or board).

The test sends patterns over some wires of the bus. These patterns are returned over other wires of the same bus to be checked.

See *MIP, Chapter 4* for details on test procedures.

Chapter 11. IML and IPL

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IPL Initialization

Power-On-reset

- Normal IPL (selected function: 0 or 9 in service mode 0).

  The IPL is performed according to the configuration and mode:

  – Single:
  IPL is performed on the CCU.

  – Twin in standby mode:
  IPL is performed on the default CCU:

    - when IPL is successful, the state of the default CCU is 'run', IPL is started on the standby CCU. If there is no active load module, IPL is stopped after phase 1 (test complete). Otherwise, IPL is continued through phase 4 and the active load module is pre-loaded.
    - when IPL is not successful, an automatic fallback is performed.

  – Twin in dual mode:
  IPL is performed on both CCUs at the same time. When IPL is not successful no fallback is performed.

  – Twin in backup mode:
  IPL will be performed on both CCUs at the same time. When IPL fails on a CCU, an automatic fallback is performed at the successful completion of IPL on the other CCU.

  When a CCU has been powered Off, an automatic fallback is performed at the successful completion of IPL on the relevant CCU.

3745 Console

1. General IPL.

   The configuration and modes are considered:

   - Single:
   The CCU is IPLed.

   - Twin in standby mode:
   IPL is performed on the CCU that already supports the configuration, if any. When no CCU supports the whole configuration, IPL is performed on the default CCU.

     When the IPL of the active CCU is complete, IPL is started on the standby CCU. If there is no active load module, IPL is stopped after phase 1 (test complete). Otherwise, IPL is continued through phase 4 and the active load module is pre-loaded.

   - Twin in dual mode:
   All the CCUs are re-IPLed.

   - Twin in backup mode:
   Both CCUs are IPLed. When an IPL is not successful an automatic fallback is performed at IPL completion.

     Note: When a CCU has been powered Off, an automatic fallback is performed at the successful completion of IPL on the relevant CCU.

2. CCU-A IPL (two CCUs are installed).

- When the 3745 is configured in twin in standby mode, and currently switched to CCU-B, IPL is started on the standby CCU. If there is no active load module, IPL is stopped after phase 1 (test complete). Otherwise, IPL is continued through phase 4 and the active load module is pre-loaded into the standby CCU.
- When the 3745 is configured in twin backup mode , and the whole configuration is switched to CCU-B, CCU-A IPL is rejected (switchback has to be performed).
- Otherwise, IPL is performed on CCU-A.

3. CCU-B IPL (same as CCU-A IPL).
4. Manual fallback facility (direction of fallback will be requested).
   - The 3745 configuration is single: Fallback request is refused
   - The 3745 is in twin in standby mode:
     – when the direction of fallback specifies a CCU which is the standby and the configuration is currently switched to the other CCU, perform fallback.
     – otherwise, the fallback request is rejected.
   - The 3745 is configured in twin in dual mode: The fallback request is refused.
   - The 3745 is configured in twin in backup mode: All adapters must not be already switched on one CCU, and the receiving CCU (CCU TO) must be running.
5. Switchback facility.
   - The 3745 configuration is single: The switchback request is refused.
   - The 3745 is in twin in standby mode: Switchback is refused.
   - The 3745 is in twin in dual mode: Switchback is refused.
   - The 3745 is in twin backup mode: The state of the CCU to which the buses will be switched must be 'reset/ready' and the state of the CCU from which buses are going to be switched must be 'run'.

See pages 3-6 to 3-9 for related information about IPL modes and bus switching.

Automatic

May be caused by a CCU hardcheck, control program abend, or host IPL request.

Considering the configuration and mode:

- Single:
  Perform IPL again.

- Twin in standby mode:
  There are two cases:
  1. The standby CCU is not pre-loaded:
     - Perform IPL again.
     - If this fails on a CCU hardcheck and the other CCU's state is 'reset/ready', IPL the standby CCU with all the configuration attached to it. The state of the faulty CCU becomes 'down'.
     - If IPL fails on a CCU hardcheck and the other CCU's state is not 'reset/ready', abort. The state of the faulty CCU becomes 'down'.
  2. The standby CCU is pre-loaded:
     - If host IPL request, perform IPL.
     - If hardcheck, abend or CCU-power down, perform fallback to the standby CCU.
     - Re-IPL failing CCU, taking dump to disk (phase 1B).
- Twin in dual mode:
  Perform IPL again.
- Twin in backup mode:
  Perform IPL again.

  When this fails on a CCU hardcheck, consider the other CCU:

  When its state is running: perform fallback.

  Otherwise, abort.

  The state of the faulty CCU becomes 'down'.

Notes:

1. In case of CCU power drop:
   When configured in standby mode, IPL is performed on the backup CCU.
   When configured in backup mode, an automatic fallback is performed.
2. MOSS automatic re-IML

   The configuration, mode, CCU default, and CCU state information are preserved from a MOSS automatic re-IML.

   A manual IPL is not restarted after a MOSS automatic re-IML. An automatic re-IPL is automatically restarted after a MOSS re-IML.
3. Fallback for CAs

   Only CAs which were operational just before the fallback are considered. They are reset, initialized, and chained as described for phase 1-A.

   CAs which were not found operational are reset and will be passed as inoperative to the control program.

Controller Initialization

The initialization of 3745:

1. Tests the MOSS IML circuits using microcode from MOSS ROS, and the TSS IML circuits using microcode from the TSS ROS.
2. Loads and initializes the MOSS microcode in MOSS storage (MOSS IML).
3. Initializes the hardware in the CCU.
4. Loads and initializes the 3745 load/dump program (CLDP) in CCU storage, along with the IPL port(s) defined for this 3745 (channel and link).
5. Loads and initializes the microcode in the scanner(s) (scanner IML).
6.
    a. Loads and initializes the control program in CCU storage (CCU IPL). This program is received either from the host through a channel-attached, link-attached IPL port, or from the MOSS disk.
    b. Dumps the contents of CCU storage either to the host through a channel, or link IPL port.

The initialization step in progress (IML, then IPL) is displayed on the hex display of the control panel, and IPL on line 4 for CCU-A or line 7 for CCU-B of the machine status area (MSA) of the operator console.

When the initialization is complete, the message 'IPL COMPLETE' is displayed on the operator console, and message 000 stays on the hex display.

When initialization fails, an error code is displayed on the hex display and could be displayed on the machine status area (MSA) when available.

The loading of the control program (from a host, over a link, or from the disk) is under control of the controller load/dump program (CLDP).

IPL Structural Description

Power-On-Reset, 3745 IPL

The Power-On-reset signal resets the MOSS, and the whole IPL process is involved (path phase 1A is used). Figure 11-1 gives the dynamic flow of the IPL process on Power-On-Reset. POR may be requested from the control panel, from the host, or may be scheduled.

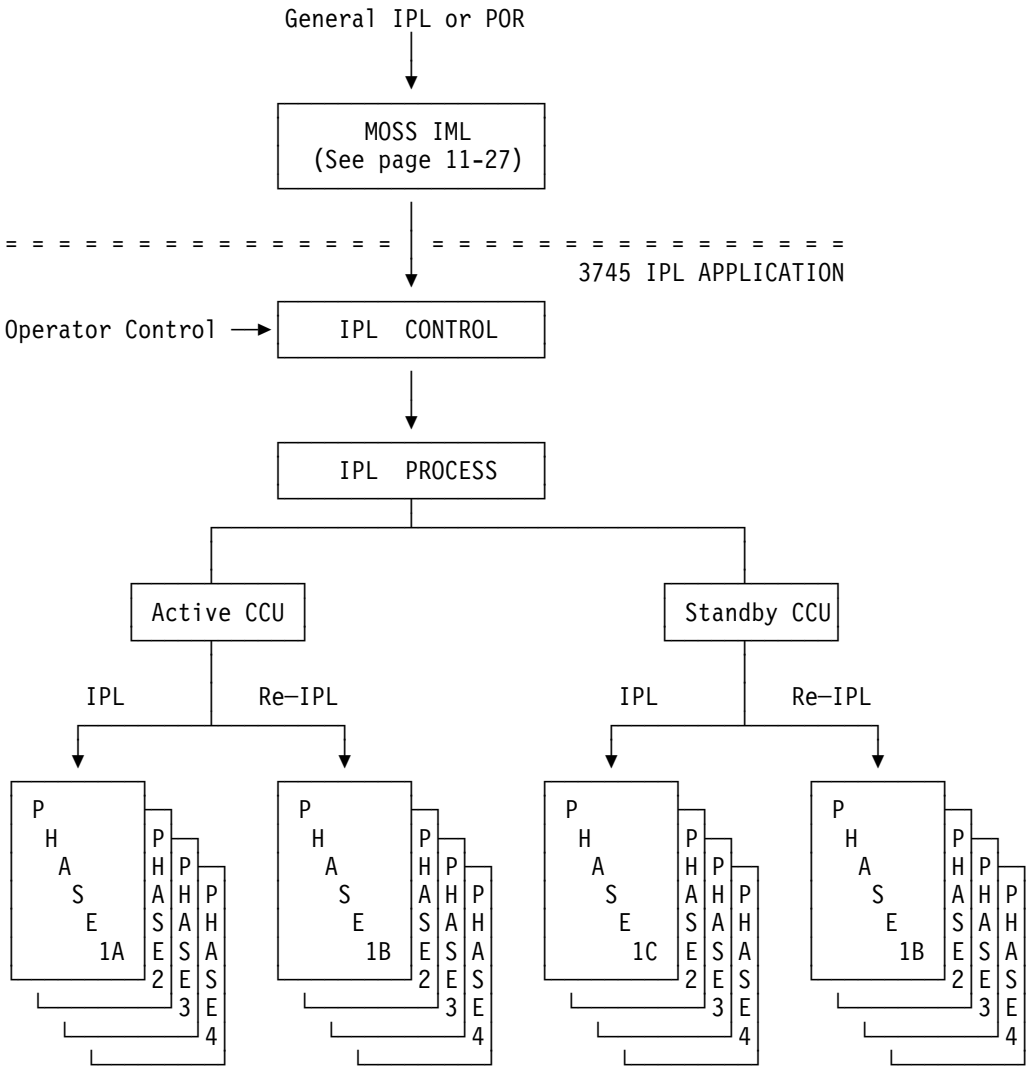


Figure 11-1. IPL Structural Description

When the IPL request is not due to a POR, it is detected by the MOSS microcode which initiates a 3745 re-IPL (path phase 1B is used).

IPL Step-by-Step Sequence

When a step-by-step IPL is performed, a message IPL PHASE x STOP is displayed before the execution of the indicated phase.

IPL

IPL may be initiated by several items:

- A general IPL (function 0 or function 9, service mode 0) from the control panel on POR.
- IPL requested from the console when the CCU is not yet initialized.
- IPL after fallback.
  The fallback may either be requested by the MOSS operator from the console, or automatically performed (3745 twin in standby mode).
- IPL after switchback.
  The switchback is requested from the console, (3745 twin in backup mode).
- A scheduled POR.
- If IPL is requested from a 3746-900 adapter, the MOSS-E CTT must be correctly set (refer to "Configuration ESCON Processor" in MOSS-E).

Figure 11-2 shows the dynamic flow of the IPL.

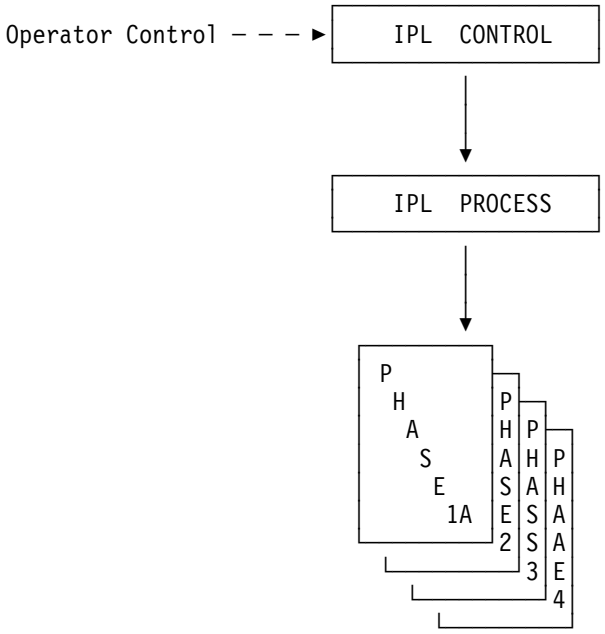


Figure 11-2. IPL Dynamic View

Re-IPL

Re-IPL may be initiated by several items:

- IPL requested from the console
- Control program abend
- CCU hardware check
- Host IPL request, direct from 3745 adapter on 3745 Model 210-610 and via MOSS-MOSS-E when re-IPL over ESCA
- Timed IPL.

The following is a description of what is done in automatic cases:

1. When the CCU IPL request is not from a CCU hardcheck, IPL phase 1B is performed on the same CCU.
2. When the CCU IPL request is from a CCU hardcheck:
   a. The previous IPL was NOT triggered by a CCU hardcheck, IPL phase 1B is performed on the same CCU.
   b. The previous IPL was triggered by a CCU hardcheck with IPL phase 1B, IPL phase 1A is performed on same CCU.
   c. The previous IPL was triggered by a CCU hardcheck with IPL phase 1A, considering the configuration and mode.
      - Single:
        CCU IPL is stopped.
      - Twin in standby mode:
        IPL the other CCU with the whole configuration; otherwise CCU IPL is stopped. The faulty CCU state becomes 'down'.
      - Twin in dual mode:
        CCU IPL is stopped and the faulty CCU state becomes 'down'.
      - Twin in backup mode:
        Perform automatic fallback; otherwise CCU IPL is stopped. The faulty CCU state becomes 'down'.

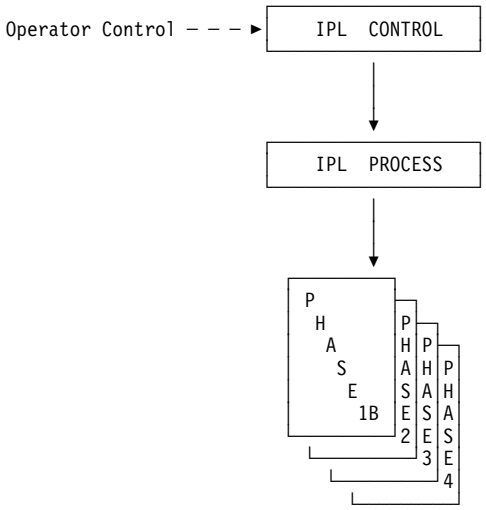


Figure 11-3. Re-IPL: Dynamic View

Backup Resources Test

When the 3745 is configured as twin in standby mode, the standby CCU is s automatically tested once the IPL of the operative CCU is completed.

The test called 'Phase 1C' is started after every IPL or re-IPL completion of the operative CCU.
Before starting the test, the message 'TEST IN PROGRESS' is displayed on the IPL line of the MSA.
Once the test is terminated, one of the following messages is displayed on the IPL line of the MSA:

- TEST COMPLETED
- TEST CHECK Fxx
  xx = 01 = Error
  xx = 02 = Hardcheck
- TEST CANCELLED

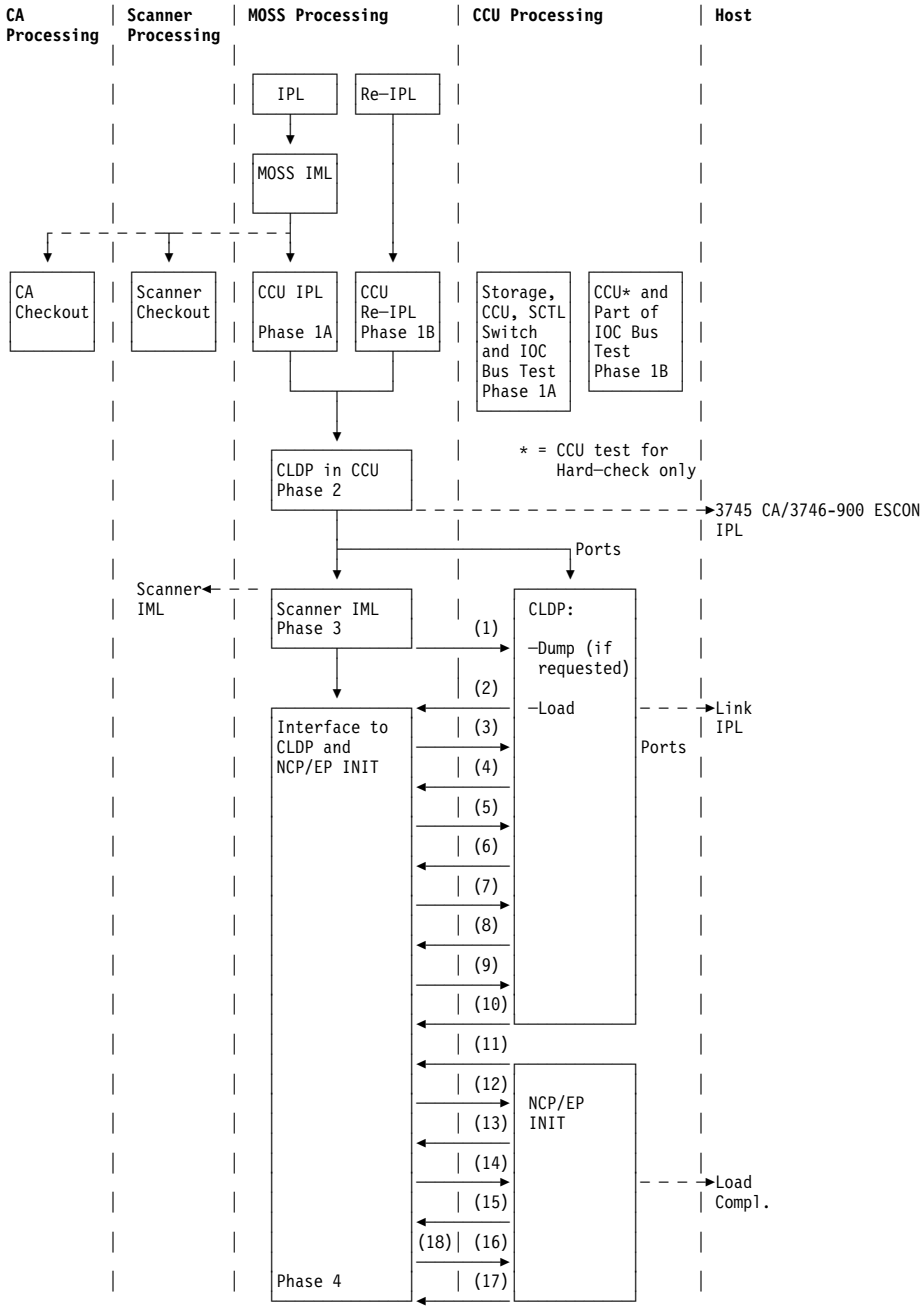
When the test is successfully completed or ended with a check, a BER is generated.

IPL of the Standby CCU

When there is an active load module on the disk, the backup resources test is extented to a complete IPL of the standby CCU. The standby CCU is loaded with the active load module to be prepared for a fallback from the active CCU.

The standby CCU is IPLed with no adapters and no port swaps. The CDS and port swaps are passed to the standby CCU's NCP at fallback time.

Controller Initialization Flow



Legend:

(1) Scanner IML complete
(2) First dump record built
(3) First dump record complete
(4) Roll in 256KB
(5) Roll in complete
(6) IPL from disk
(7) IPL from disk complete
(8) CP information
(9) CP information response
(10) Control program loaded
(11) Control program parameters
(12) Control program parameters saved
(13) CDS information requested
(14) CDS information available
(15) Request re-issue port swaps
(16) Re-issue port swaps
(17) Control program initialized
(18) Re-issue MB port swaps 3746-900

Note: The 3746-900 IML is done asynchronously and could be completed at any time during 3745 IPL.

Controller Initialization Sequence

IPL Phase	Hex Step	MOSS/CCU Action	Scanner Action	CA Action
1A	FF0 FF1	Controller Initialization Controller IPL LSSD mechanism checking CCU LSRs initialization SWAD initialization CCU and high-speed buffer checkout (See Note 1) SCTL checkout (See Note 1) Storage protect initialization CCU storage test Switch checkout and initialization (See Notes 1 and 2) CA initialization Full instruction test (FIT) IOC bus test	The reset sent to IOC adapters starts the scanner test from CSP ROS: Start Initialization Instruction test Local storage test Interrupt mechanism test Control store test Address compare mechanism test IOC bus interface test (XR00, XR01, XR02, ping, pong) L1 interrupt to CCU Autoselect L2 interrupt to CCU Priority and channel Request test IOC-bus test phase 1 IOC-bus test phase 2 (ROS) IOC-bus test phase 2 (Storage) Timer (100 ms) Interrupt to MOSS test (TSS only) Hard stop test	Reset CAs connected to CCU(s) under IPL. Initialize those which have been successfully reset. Chain the CAs which have been successfully initialized. • Chaining is performed per IOC bus. • Chaining is not possible if more than one gap exists in the sequence of installed CAs. A gap is: – a power supply down, – a CA in error (for example, not initialized), – two CAs in error sharing the same power supply count for one gap. • When chaining is not possible on an IOC bus, all CAs of this bus are reset and will be passed as INOPERATIVE to the control program. Errors that have been encountered are recorded in BER 01-06 (IPL complete with errors).

See Notes on the next page.

Notes:

1. When two CCUs are under IPL, the checkout will be sequentially executed on each CCU (except the checkout loading from the MOSS disk).
2. **Trigger Item Switch Initialization.**

   At POR, IPL from the Console:

   - Single: All the buses (IOC and adapter buses) are to be attached to the single CCU. When attaching a bus fails, the IPL is aborted and an IPL check BER is logged.
   - Twin in standby mode: All the buses (IOC and adapter buses) are to be attached to the CCU under IPL (CCU under IPL is unique). When attaching a bus fails, the IPL is aborted and an IPL check BER is logged.
   - Twin in backup mode or twin in dual mode: The main and primary buses are attached to the CCU(s) under IPL (CCU-A to adapter buses 1 and 2, CCU-B to adapter buses 3 and 4). When attaching a bus fails, the IPL is aborted and an IPL check BER is logged.

   Fallback: All the buses (IOC and adapter buses) are attached to the CCU under IPL. When attaching a bus fails, the IPL is aborted and an IPL check BER is logged.

   Switchback: The IOC and adapter buses are attached to the CCU under IPL. When attaching a bus fails, the IPL is aborted and an IPL check BER is logged.

   Automatic: The switch configuration is unchanged.
3. If the MOSS is powered Off:
   - After an 'IPL Complete', the connection MOSS to control program is not broken. At MOSS power On, the MOSS will be automatically connected to the control program.
   - During phase 1 of the IPL, the CCU status may be wrong at power On. For example, IPL-REQ, RESET, or POWER DOWN status may be replaced by the READY status.

Controller Initialization Sequence (Continued)

IPL Phase	Hex Step	MOSS/CCU Action	Scanner Action	CA Action
1B	FF1	CONTROLLER RE-IPL LSSD saving CCU LSRs saving CCU dump on disk (See note 1) LSSD mechanism checking CCU LSRs re-initialization Scanner dump Roll out processing (See note 2) Retrieving BERs from CRP (See note 3) Saving bottom of CCU storage (See note 4) Full instruction test (FIT) IOC bus test Restoring CCU storage bottom	Program reset Run scanner checkout	• Chain the CAs which were operational just before the re-IPL takes place (the chaining rules described for phase 1-A apply for phase 1-B). • The CAs which were not found operational (that is, which were initially inoperative, which have become down or which were in concurrent maintenance) are reset and will be passed as INOPERATIVE to the control program.

Notes:

1. When the CCU dump option has been previously set (IPL requested from host), and the dump data space is free on disk for that CCU, the CCU is dumped to the MOSS disk.

   On control program abend and CCU hardcheck: when the automatic disk dump parameter is set ON and when the dump data space is free for that CCU, the MOSS dumps the whole CCU automatically and saves the dump on the MOSS disk.

2. The last 256KB of CCU storage are rolled out for eventual dump purposes: during IPL phase 4, CLDP may ask MOSS to restore the last 256KB of CCU storage, to dump the CCU to the host. In the CCU, these 256KB are altered with information loaded from MOSS (saved LSSD, saved LSR, IPL port table, CLDP) during phase 2.
3. When the CRP is found empty and the IPL request comes from a control program abend (other than CLDP), a BER is logged as ALARM support with the control program abend code previously saved by the MOSS.
4. After diagnostics completion, the 256KB moved have to be restored at the bottom of CCU storage.

Backup Resources Test

IPL Phase	Hex Step	MOSS/CCU Action	Scanner Action	CA Action
1C	FF0	Backup resources test LSSD mechanism checking CCU LSRs initialization CCU and high-speed buffer checkout SCTL checkout Storage protect initialization CCU storage test Switch internal checkout Full instruction test (FIT)	No action	No action

Controller Initialization Sequence (Continued)

IPL Phase	Hex Step	MOSS/CCU Action	Scanner Action
2	FF2	LOAD AND START CLDP (See Note) • Load CLDP and IPL port definition in Rollout Area (256KB) • 3746-900 knowledge is done via IPL port table information. It is set by the MOSS, based on CDF information. • Previously saved LSSD and LSR contents sent to CLDP (re-IPL only) • Give control to CLDP to monitor IPL ports and may signal to the hosts that control program loading is started on a channel IPL port.	No action
3	FF3	SCANNER IML Three types: TSS, HPTSS, and ESS (Selective scanner IML is a MOSS function and is not part of the controller initialization.) • The list of scanners that have completed IML is sent to CLDP. • CLDP starts monitoring the defined link's IPL ports for an IPL Initialization. • The 3746-900 resources are received via RST exchange.	• CSP storage set to zero • Microcode on disk/diskette broadcast to scanners by MOSS. The scanner code is sent on a block basis using the CCU/scanner buffer. MOSS transmits blocks to the CCU buffer and each scanner gets each block through cycle steal. After a time out, MOSS gets the completion block from each working scanner and resumes storage loading with the next block.

Note: A single CLDP exist on the MOSS disk for all kind of CCUs. The CLDP is loaded in the CCUs specified in the ccu-under-ipl variable defined in the resident IPL Control Block. That is, depending on ccu-under-ipl content, the IPL phase 2 will load CLDP into CCU-A or CCU-B or into both CCUs.

Controller Initialization Sequence (Continued)

IPL Phase	Hex Step	MOSS/CCU Action	Scanner Action
4	FF4 FF5 or FF6 or FD6 FF7 000	CCU LOADING, DUMPING, AND INIT (See following notes) • The control program can start from the host if loading on link-IPL port • Write IPL command detected (from host) • Loading on channel IPL port • Loading on link IPL port • Loading from the disk • CCU control program loaded • CCU initialization with CDF parameters • MOSS initialization with control program information table (CPIT) CONTROLLER INITIALIZATION COMPLETED WITHOUT ERROR	The scanner handles the traffic load.

Notes:

1. The MOSS microcode provides support to the new IPL/dump procedures. The following support is provided to the operator:

   a. The ability to control the saving of a control program load module, at IPL time, from CCU storage to the MOSS disk.
   b. The ability to optionally load a control program load module from the disk into CCU storage.
   c. The ability to load one of the 3745 CCUs from the MOSS disk while loading the second CCU from a host.
   d. The ability to optionally save a dump from CCU storage to the MOSS disk as a normal part of the IPL process.
   e. The ability to dump the CCU storage to the host, while performing IPL on a CCU.
   f. The ability to load both CCUs from disk.

   The purpose of the 3745 IPL phase 4 is to communicate with the CLDP and with the control program to answer their commands or to give them complementary information.

2. The MOSS/CLDP communication is divided in three steps:

   a. Step 1: Dump.

      - The dump is requested by the network operator: the CLDP performs the CCU dump to the host, and as soon as enough space is freed in the CCU, the CLDP requests MOSS to roll back into the CCU that part of CCU storage saved on MOSS during IPL phase 1B. The storage dump is not available on remote load activation through non SNA lines.
      - The dump is not requested by the network operator: Should the dump report parameter be set to dump saved to disk in the IPL port table, the CLDP would build the dump header and send it to the MOSS.

   b. Step 2: IPL.

      - If the IPL is requested by the network operator, as soon as the CLDP has loaded the control program, it sends to MOSS the control information indicating whether the control program is to be saved on the MOSS disk or not, the control program entry point, its size, and the new setting of the automatic disk IPL/disk dump options. These automatic options have to be considered on the next automatic CCU IPL request.

- If the IPL is not requested by the network operator, the CLDP would ask MOSS to perform IPL of the control program from the MOSS disk by sending the IPL from disk request. If a load module exists on disk and its status is active. Otherwise the control program would be loaded from the host.

c. Step 3: End of Synchronization with the CLDP.

Stand-Alone IPL/DUMP (from/to Disk)

The stand-alone IPL/DUMP (unattended operations) contains the following functions:

- Load the control program from the disk.
- Dump the control program on the disk.
- Retrieving a dump from the disk.

Two load modules per CCU and one dump are available per CCU.

- A control program (CP) load module is saved on the disk under control of the access method. In addition, the access method indicates through an IPL request, what the functions to perform are when the next automatic IPL takes place (automatic IPL from disk and/or automatic dump to disk). These two options are always set/reset at the same time.

  The CP load module on disk is used for an automatic IPL either under explicit request of the access method, or if the automatic IPL option has been set.

  The following IPL requests can lead to an IPL from disk:

  1. 'IPL from disk' host request.
     A CP load module must exist on disk. The load module status becomes active after the IPL.
  2. Power On.
     A CP load module must exist on disk, its status must be active and the automatic IPL from disk option must be ON.
  3. CCU hardcheck.
     A CP load module must exist on disk, its status must be active, and the automatic IPL from disk option must be ON. In addition, dump location on disk must be available for that CCU except in case of remote load activation (non SNA lines).
  4. Control program abend.
     Same as for CCU hardcheck.
  5. IPL request from the MOSS console.
     A load module must exist on disk, its status must be active, and the automatic IPL from disk option must be ON.

- Only one dump can be kept on the disk per CCU. As long as this dump is present, no other dump is possible for this CCU.

  A dump on disk is performed if the automatic dump option has been set during a previous host IPL request, or via new DII option for remote load activation initialization.

Notes:

1. A load module on the MOSS disk is set active:
   - Either after an IPL from disk host request has been serviced.
   - Or when a load has been done from the host, followed by a save request, or via new DII option for remote load activation initialization.
2. The active flag is reset in case of a reload from the host without a save request.
3. All the load module attributes (load module name, entry point, length, active, automatic IPL, automatic dump) are saved on disk.
4. There is one Online updating capability of the automatic IPL and automatic dump options from MOSS.

   They can be updated through a new IPL from the host.
5. Upon request from the host operator, the dump is transferred from the MOSS disk to the host through the dump transfer function.
   The disk is purged on request from the host operator.
6. In case of multiple load modules the attributes can be set or reset on the active load module.

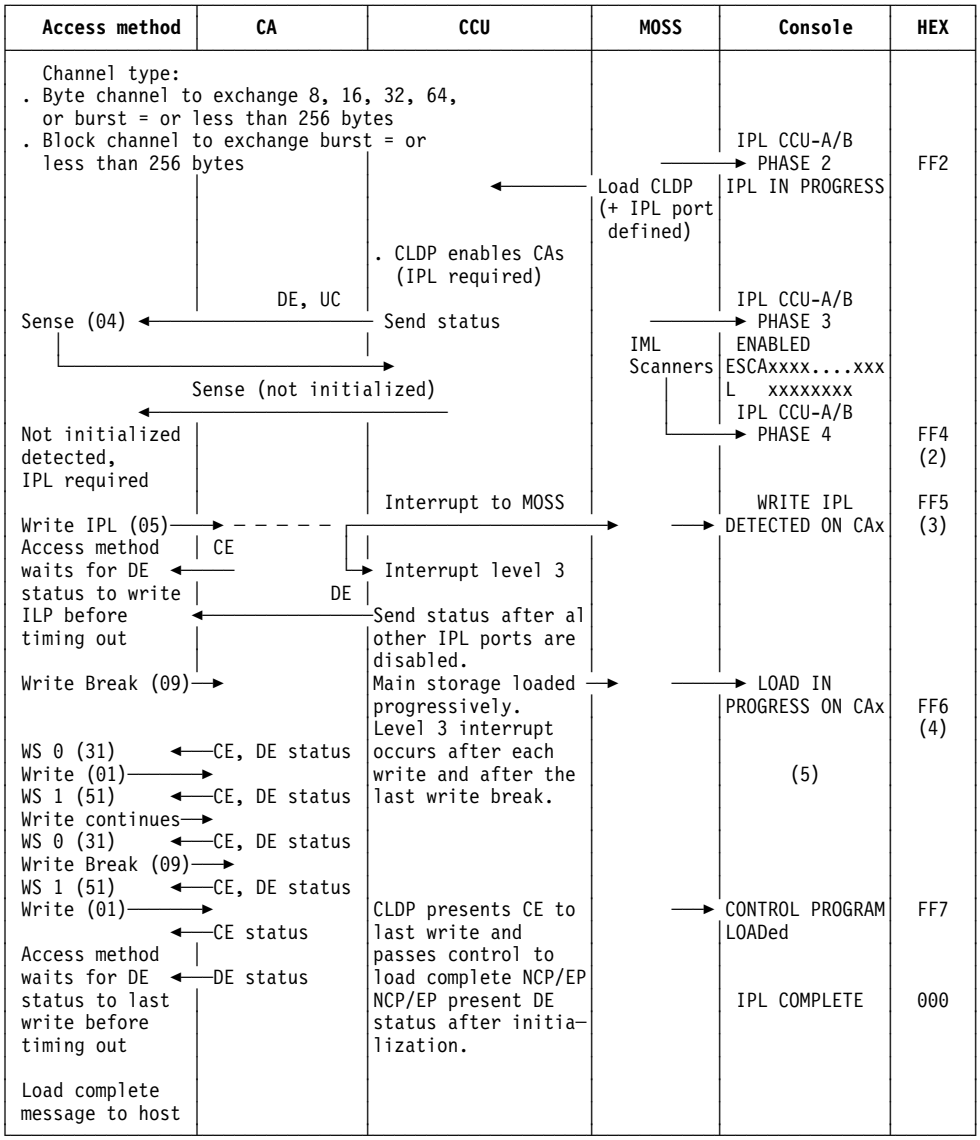
IPL Exchanges Over a CA or ESCA IPL Port

The figures on the next pages on the next panels indicate the sequences in loading a control program into the 3745 over a CA or ESCA IPL port, when an IPL has been started, except when the IPL is initiated from the host.

When the IPL is initiated from the host, the DE, UC, and sense are not sent by the 3745, but the remaining sequences are the same.

During an IPL, the responder is the CLDP in the 3745. The host system can start sending the control program to the 3745 as soon as the CLDP has been loaded (end of IPL phase 2). The host continues sending the remainder of the control program to the 3745 through IPL phase 4.

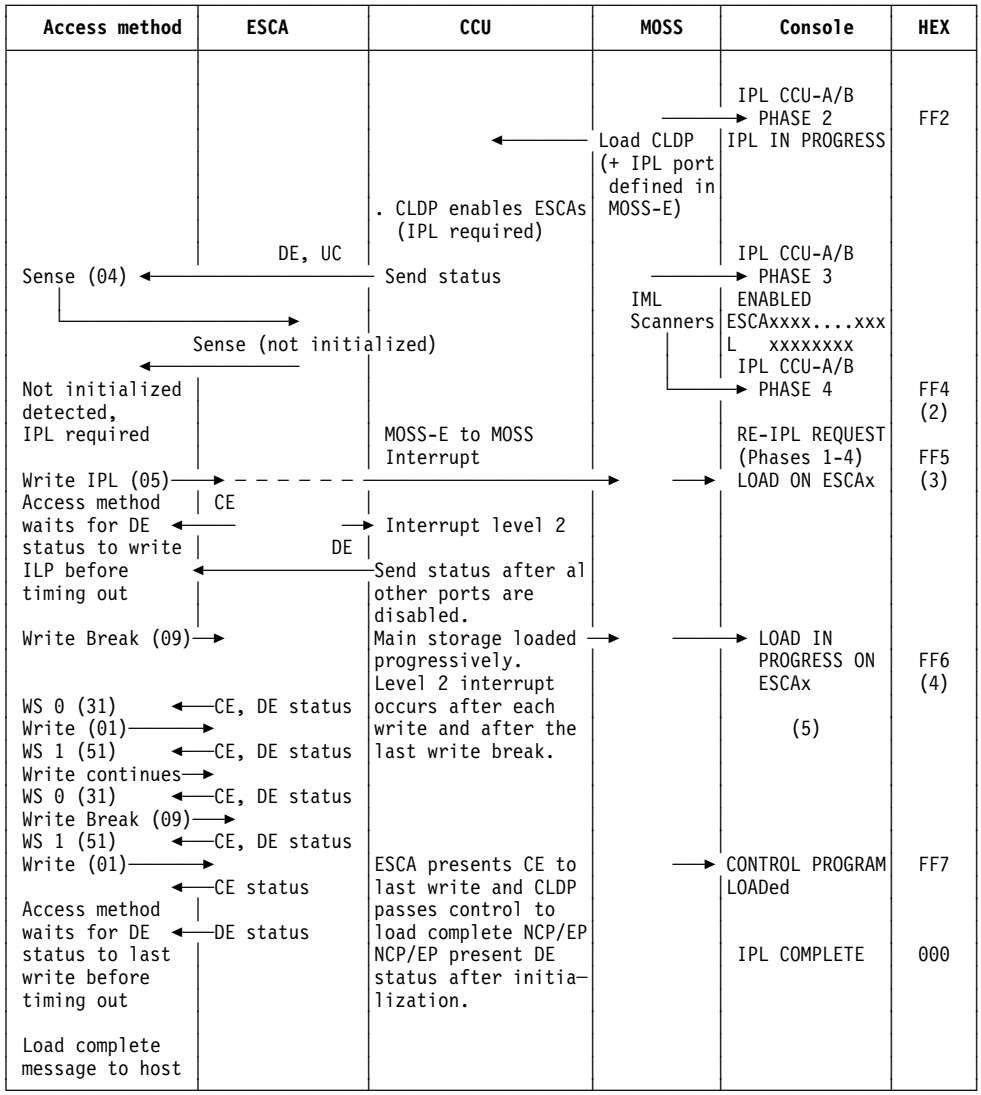
IPL Exchange Mechanism (3745 CA IPL Port)



Notes:

1. Refer to *Service Functions* for a description of the IPL messages that appear in the machine status area.
2. FF4 is displayed until a write IPL command is received from the host.
3. FF5 is displayed only during an channel IPL.
4. FF6 is displayed only during an link IPL.
5. On line 2 of the machine status area, X72: XXXXXX indicates the progression of the IPL by displaying the CCU storage addresses. The X'72' contents increment until the IPL is complete.

IPL Exchange Mechanism (3746-900 ESCA IPL Port)



Notes:

1. Refer to *Service Functions* for a description of the IPL messages that appear in the machine status area.
2. FF4 is displayed until a write IPL command is received from the host.
3. FF5 is displayed only during a channel IPL.
4. FF6 is displayed only during an link IPL.
5. On line 2 of the machine status area, X72: XXXXXX indicates the progression of the IPL by displaying the CCU storage addresses. The X'72' contents increment until the IPL is complete.

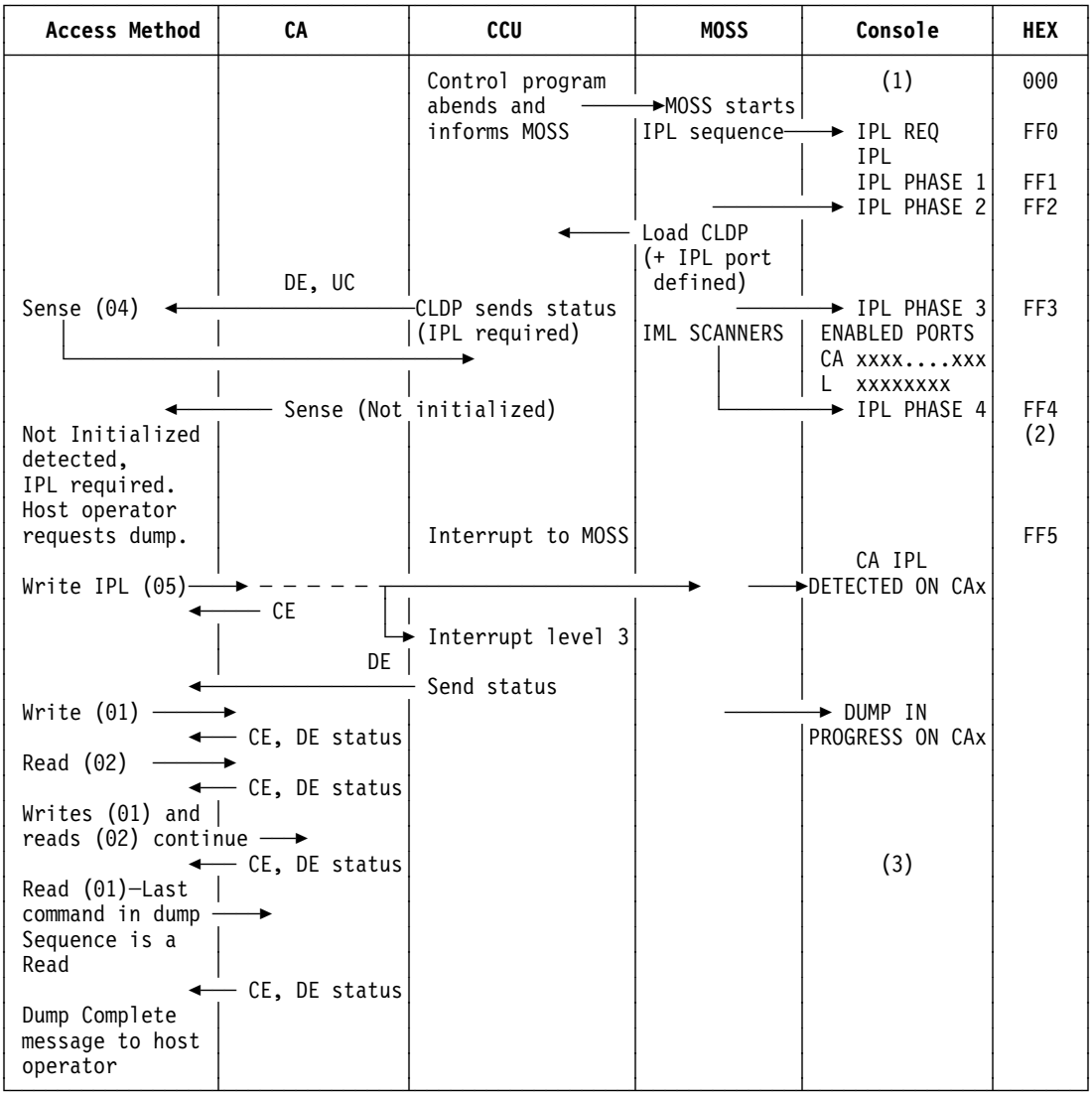
Dump Exchanges Over a CA or ESCA IPL Port

The following figures indicate the sequences in dumping the storage contents of a 3745 after a control program abend via a 3745 CA or a 3746-900 ESCA.

After the abend, MOSS loads the CLDP and the CLDP is the responder during the dump sequence. If a dump is initiated from the host with a control program still active (no abend), the DE, UC, and sense are not sent by the 3745, but the remaining sequences are the same.

The dump can proceed as soon as the CLDP has been loaded (end of IPL phase). The dump continues until the last read command is received by the CLDP. The CLDP is then ready to receive another dump or program load sequence. The hex display remains FF5 after the dump is completed.

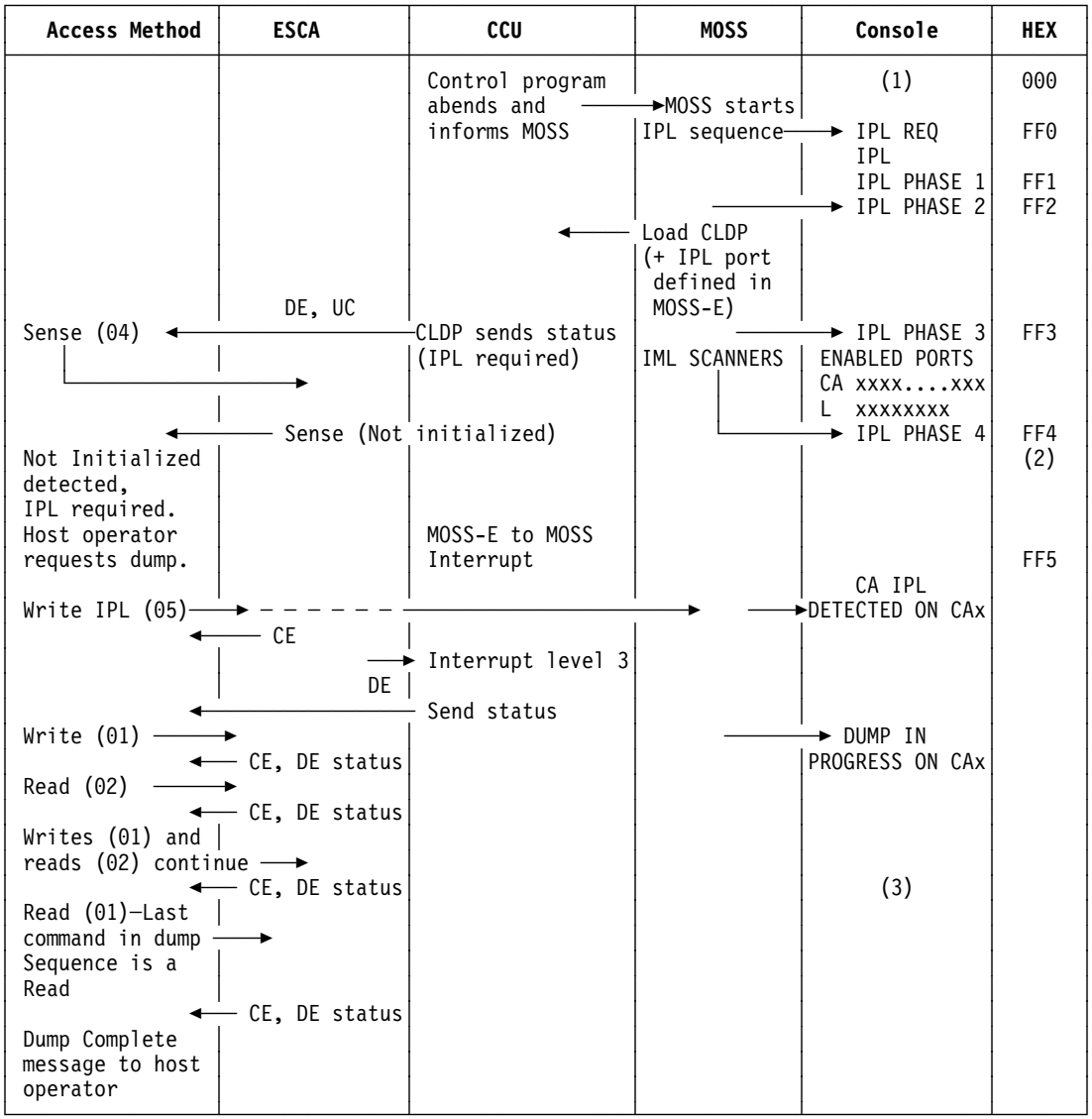
Dump Exchange Mechanism (3745 CA IPL Port):



Notes:

1. Refer to *Service Functions* for a description of the dump messages that appear in the machine status area.
2. FF4 is displayed until a wWrite IPL command is received from the host.
3. On line 2 of the machine status area, X72: XXXXXX indicates the progression of the dump by displaying the CCU storage addresses. The X'72' contents increment until the dump is complete, that is, the dump complete message appears on the host console.

Dump Exchange Mechanism (3746-900 ESCA IPL Port):



Notes:

1. Refer to *Service Functions* for a description of the dump messages that appear in the machine status area.
2. FF4 is displayed until a wWrite IPL command is received from the host.
3. On line 2 of the machine status area, X72: XXXXXX indicates the progression of the dump by displaying the CCU storage addresses. The X'72' contents increment until the dump is complete, that is, the dump complete message appears on the host console.

IPL Exchanges Over a Link IPL Port (SNA Lines Only)

The control program sending the IPL PIUs to the link-attached 3745 must be loaded and active. The CLDP processes the IPL PIUs in the 3745 that is being IPLed.

IPL phase 4 has to be entered before an IPL can take place over a link (IML must have been performed on the scanners).

IPL over a remote link is possible with TSS and HPTSS. It is not supported for TRSS or ESS.

Refer to "Chapter 1, MSA Fields Definition (IPL Information)" of the *Service Functions* for a description of the IPL progress messages that appear in the machine status area.

FF5 is displayed only during IPL or over a channel adapter IPL port.

On line 2 of the machine status area, X '72': XXXXXX indicates the progression of the IPL by displaying the CCU storage addresses. The X'72' contents increment until the IPL is complete.

When X'72' is equal to 00XXXX, XXXX is an abend code. Refer to page “CLDP Abend Codes” on page 11-25 for details.

For more information, refer to *AOG, LKP Function*.

Dump Exchanges Over a Link IPL Port (SNA Lines Only)

FF5 is displayed only during IPL over a channel adapter.

FF6 is displayed during the dump and dump completion. The CLDP is then ready to receive another dump or load sequence.

Refer to "Chapter 1, MSA Fields Definition (IPL Information)" of the *Service Functions* for a description of the machine status area.

On the 3745 console, X'72' indicates the progression of the dump by displaying addresses that increment until the dump is complete.

For more information, refer to *VTAM Documentation* and *Remote Loading/Activation Guide, SA33-0161*.

Abnormal Conditions During Controller Initialization

1. Any IPL request made during the processing of a previous IPL request is detected and serviced immediately, unless an IPL of the other CCU is in progress.
2. If a CLDP abend occurs (output X'70'), the MOSS stops the IPL application. A manual intervention is required to restart the initialization, which resumes from phase 1B.
3. If an NCP/EP initialization abend occurs (output X'79' + X'70'), the MOSS automatically resumes the initialization from phase 1B until the threshold is reached.
4. Any hardware check causes an IPL abend. See “Control Program Load/Dump Abend Codes” on page 11-24 for the list of abends.

5. A BER is logged if an IPL abend occurs, or when initialization is complete with non-blocking errors (for example, a scanner on which IML cannot be performed), or when IPL is successfully completed.

Using CCU Functions During Initialization

You may use the CCU functions (for example, display, alter) as soon as the CCU initialization is complete (phase 1A or 1B). Using the CCU function key (F2), you may switch from the initialization process to the CCU services, and conversely.

During step-by-step IPL, the CCU FNCTN must be used only when the IPL stop message, indicating a step end, is displayed on the console.

Control Program Load/Dump Abend Codes

Abend codes are in the form: CNNN, where:

- C = Component of the CLDP that failed
- NNN = Unique number to indicate where the failure occurred.

CLDP Abend Codes

IPL State Abend Code Wait	
0001	No potential IPL ports available (neither CA, nor LA, nor automatic disk re—IPL)
0002	MOSS TIMEREG = 0 (timer set when a mailbox is sent to MOSS and reset when the acknowledgement is received)
0003	IPL port found, but not a CA, not a LA, and not MOSS disk.

Level 1 Abend Codes	
1002	Level 1 error, Hardstop (indicates it is neither a CA Level 1, nor a LA Level 1, nor an IOC error, nor a Level 1 error while in Level 1)
1003	Exit routine did not receive ACK from MOSS
1004	Level 1 error raised by a CA
1005	Level 1 error raised by a LA
1006	Level 1 IOC error
1007	Level 1 error while in Level 1
1010	Time out on IPL from disk response from Level 1.
1012	Time out on dump to disk response from Level 1.
1066	Level 1 from coupler when load/dump is in progress

Level 2 Abend Codes	
2004	Re—IPL : SIM received
2005	DISC received
2006	Early SNRM (before IPL or dump final)
2007	Early XID (before IPL or dump final)
2008	Supervisory frame is not RR, RNR, REJ
200A	Link activity timer (60s) has elapsed (ie no line activity) during a link IPL.
200B	SDLC frame not a supervisory one, and command not supported by CLDP.
200C	Level 2 spurious interrupt in not wait for IPL state.
200D	Level 2 unresolved interrupt neither IOC 1, neither IOC 2.
200E	Level 2 unresolved interrupt neither PC1 L2, neither from a LA.
202A	Permanent link error on ESCON.
202B	Permanent station error on ESC0N.
202C	RDI/RDU completed.
202D	Error with disk when ESCON request.

CLDP Abend Codes (Continued)

Level 3 Abend Codes	
3001	Host IPL request while dumping
3002	Initial selection interrupt and no bits set in CA register 0
3003	Invalid CCW: – Read type not a Sense (04), not a Sense ID (E4), not a Read (02). – CCW to be NOOP'ed not a Write IPL (05), and not a NOOP (03).
3004	No valid CCW: – Write type not a Write (01), and not a Write Break (09).
3005	Not equal to 0, 128, 256, 384 (inbound remaining xfer length).
3006	CA hung (for example: after a PGM reset cannot be disabled, or is always in 'CHANNEL MONITOR' mode).
300A	CA backup timer elapsed because no channel activity for 60 seconds. See Note.
300D	CA Level 3 unresolved interrupt neither I/S, nor D/S
300E	Level 3 unresolved interrupt neither timer, nor PCI, nor panel, nor CA.
3010	Time out on IPL from disk response from level 3.
3011	Time out on control info response from level 3.
301A	ESCON backup timer elapsed.

Level 4 Abend Codes	
4001	NAK from MOSS

Note: One of the causes for abend code 300A is a CA defined with the data streaming option and connected to a host which does not support data streaming.

MOSS IML Description

Introduction

MOSS IML is done in steps starting from the MOSS physical reset, then testing the MOSS components, and ending with the initialization of the MOSS microcode.

The IML microcode used is stored:

- On the MOSS ROS
- On the disk or diskette

MOSS IML stops when a severe error is encountered. An error code is displayed on the hex display of the control panel.
See *MIP* Appendix A, for control panel code definition.

MOSS Diagnostics

Moss diagnostics run before the MOSS IML and may be activated by:

- The machine Power On
- The machine reset
- MOSS Power On
- MOSS IML
- MOSS automatic re-IML

IML Codes

Hex	MOSS Diagnostics When Power ON or Reset, with OPTION:		
	No Bypass Diagnostics	**Bypass Diagnostics**	**When Automatic Re—IML**
	Reset IML	Reset IML	Reset IML
170			Alert PLC card that Re—IML starts
002	Internal init MMIO test MPC test	Internal init	
0A0	Storage test (non destructive if dump) Init ROS mainline controller		Storage test Init ROS mainline controller
0D0	DFA test (full test, smaller if dump)		DFA test
17B		Storage init	
17F	Return control to ROS IML processor	Return control to ROS IML processor	Return control to ROS IML processor

IML Codes (Continued)

Hex	MOSS Diagnostics When Power ON or Reset, with OPTION:		
	No Bypass Diagnostics	**Bypass Diagnostics**	**When Automatic Re—IML**
F02	IML Initialization	IML Initialization	IML Initialization
F03	Open Adapters	Open Adapters	Open Adapters
F04	Open Disk/Diskette	Open Disk/Diskette	Open Disk/Diskette
F05	Check Disk/Diskette Id	Check Disk/Diskette Id	Check Disk/Diskette Id
F08	Directory Entry Load MOSS Operational Code	Directory Entry Load MOSS Operational Code	Directory Entry Load MOSS Operational Code
F09	Go to MOSS Loader	Go to MOSS Loader	Go to MOSS Loader
F0A	Call for diagnostics Reset all adapters See Note	Reset all adapters See Note	Call for diagnostics Reset all adapters See Note
190	MCA test (3745-x10)		MCA test
1D0	MAC test		MAC test
1FF	Return control to storage IML processor MLA diag (3745-x1A)		Return control to storage IML processor
F0B	Control is given to the level supervisor of the operational code which in turn dispatches the operator control task. The console initialization is done if power On.		
F0C	Start of the logical initialization: Timer initialization of the MAC Dispatch MSA task, loop detection task, BER task Disk and diskette initialization Power initialization CDF loading and initialization of dynamic table Channel information table loading Purge scanner operation active from a previous IML Reset MOSS inoperative MCCU—A and MCCU—B Enable HLIR and LLIR interrupts Reconnection to the control program On 3745 21A-61A: load code on 2MB and dispatch LAN control task		
F0E	End of IML The MOSS is alone	End of IML The MOSS is alone	End of IML The MOSS is alone
F0F	End of IML The MOSS is offline	End of IML The MOSS is offline	End of IML The MOSS is offline

Note: Before being operational, the MOSS microcode is initialized. Control is given to this code on Level 6. PSVs from 1 to 5 are initialized. BER stacked pointers are initialized if POR. (The operator control task is prepared to take control.)

Scanner IML Step Description

Introduction

Loading the microcode into the scanners is either a general function common to all scanners, or a selective function related to one scanner only.

From a scanner point of view, general or selective IML functions are supported by the same scanner ROS code.

From a MOSS point of view, the general IML of the scanners is a phase of the controller initialization, whereas the selective IML of a scanner is a TSS function.

IML requests are presented to the MOSS, which controls the scanner IML.

IML Principle

An IML responder is located in the scanner ROS (CSP card).

The IML is done on a block transfer basis, between the MOSS disk or diskette and the CSP storage, via the MOSS storage and the CCU main storage scanner communication area.

This block transfer is completely transparent to the control program running in the CCU.

Blocks of code along with control information transit through the MOSS/scanner dedicated area, which is the last 32KB of the CCU storage (plus the area for the scanner mailboxes).

CCU commands are simulated via the MIOC interface.

IML Steps

The IML of a scanner takes four steps.

Step 1: Scanner Reset/IML (IPL with Phase 1A)

1. A general 'reset' signal is sent to every scanner (general IML) by the MOSS microcode during phase 1 of the controller initialization.
2. On the scanner side, checkout starts when the 'reset' signal is received.

   At this time, the scanner ROS is ready to handle the scanner IML commands.

Step 2: Get CSP Checkout Result (IPL with Phase 1B)

After a time out, the MOSS fetches and tests the checkout result of any scanner. It uses IOH instructions sent to each scanner and specifying a 'read checkout status' command.

The MOSS flags the scanner as 'no IML performed' if the checkout result is bad, or if the scanner does not answer the IOH. The error is logged, and the IML sequence goes on if at least one scanner is working.

Step 3: Transfer Block of Code

1. The MOSS sends the first IML commands with two MIOHs indicating the address of the communication area in CCU storage. Each scanner can then determine its address in the mailbox and the address of the buffer part of the communication area.
2. The MOSS starts transferring the microcode in block format. The block length is 1792 bytes (max).
3. The MOSS loads each block from the disk or the diskette in the 'buffer part' of the MOSS/scanner dedicated area in the CCU.
4. The MOSS sends an MIOH instruction to each scanner, specifying:

   a. Scanner address.

   b. IML command.
5. The MOSS initiates a time out counter and waits for the end of transfer for the current block.
6. On the other side, receiving the MIOH command causes the scanner to cycle steal both the control information and the current block, and to store it in its storage.

A transfer completion code is sent back to the dedicated area. If an error occurs, the scanner sends back an error status to the dedicated area.

Step 4: Get Block Transfer Completion

1. When the transfer of blocks of code is finished (MOSS time out), the MOSS reads the transfer completion code returned by each scanner in its dedicated area.
2. If the command failed, the scanner is flagged as 'no IML performed' in the scanner configuration block residing in the MOSS storage, and the error is logged.
3. The MOSS then loops, transferring the remaining blocks to the working scanners.
4. When scanner loading is complete, MOSS sends the 'init' signal to leave the scanners in the initialized state.

   Once the code has been loaded, the scanner init parameters are loaded in the 'buffer part' of the MOSS/scanner dedicated area in the CCU.
   In addition the MOSS loads the control part of each scanner within the dedicated area.
5. Once the scanner has been 'Initialized', it returns a status to the MOSS indicating success or failure of the IML. In addition, the scanner returns the MUX number and the extend bit presence.

   The MUX number and the extend bit presence are compared with the CDF. In case of bad compare, the scanner is considered as not being IMLed.

Timed IPL

Timed IPL Description

The timed IPL feature allows to reload all the controllers in a network at a scheduled time.

This network initialization consist of:

1. From VTAM, commands are sent to all the 3745 controllers in the network, to:
   - Set a scheduled IPL for a specified load module.
   - Perform a multiple load module (MLM) add command integrating a scheduled IPL.
   - Perform a MLM replace command integrating a scheduled IPL.
2. When the MOSS receives such a command, it checks if it is feasible. If yes, the will keeps this time for the load module and at the prescribed time, it will trigger automatically an IPL which will load the load module in the CCU.

   When a 3746-900 is attached to a 3745 21A-61A, a coupler reset will be sent if the 3745 configuration is as follows:
   - Single CCU or
   - Twin CCU in mode:
     – Standby or
     – Dual/backup and Timed IPL must be triggered for both CCU at the same time.

To control the network, the timed IPL allows:

1. To cancel a scheduled IPL.
2. To send an alert to NetView at a prescribed time, warning the operator that a scheduled IPL is set and that the IPL will occur soon.
3. To display on the VTAM console, the disk IPL information related to scheduled IPLs.
4. To display on the MOSS console, the disk IPL information related to scheduled IPLs.

IPL Triggering Conditions

Automatic IPL is performed when the MOSS state = ONLINE. This is the operational state.

The automatic IPL will not be started if:

1. The battery is down.
2. The scheduled IPL date and time is passed.
3. At the time of the scheduled IPL, the MOSS status does not allow an automatic IPL.

Chapter 12. Error Logging

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Introduction

Hexadecimal Codes

During 3745 initialization, the hardware is checked before loading the NCP or PEP. While the different tests are running, they may encounter an error or an unusual event. The logging routines are in charge of indicating the anomaly, analyzing it and displaying a hexadecimal code on the operator's panel. The MIP gives an exhaustive list of all the errors and progression codes.

If a 3745 control panel error occurs, or if a MOSS IML threshold is reached, the control panel displays hexadecimal codes indicating the cause of the error. In parallel with the display of the hexadecimal code, a Box Event Record (BER) may be built if the state of the machine's hardware permits it.

Thus very often there is a connection between a hexadecimal code and a BER. (See page 12-33).

Box Event Records (BERs)

The Event Logging Procedure of the MOSS reports each error caused by either an intermittent failure or a 3745 down (controller re-IPL).

Any such event in a 3745 subsystem is reported first to the NCP/PEP, and then to the MOSS for logging. In this case, a BER is built in a place called check record pool (CRP), where MOSS has access to it. In some cases, a BER is built directly by the MOSS itself. In any case, the BER is stored in a buffer in the MOSS RAM. The BER built by the MOSS is called composite MOSS BER, and may contain several BERs (usually three). The MOSS also generates the power BERs and the diagnostic BERs. For the generation, the formatting, and the storage of the BERs, see page 12-6.

Note: Some BERs, generated during IML may have a date/time stamp of '00/00 00:00', because the MOSS has not yet fetched the date and time. These BER will appear in the correct sequence in the BER log and should be considered in problem determination.

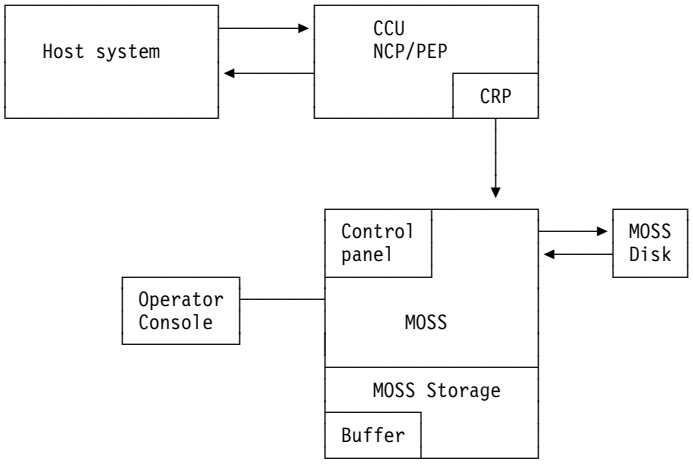


Figure 12-1. Box Event Records Handling

Thresholds

Errors are normally retried by the Control Program or Microcode, in order to achieve fault tolerance and eliminate abends or loss of resources on intermittent failures.

When the count is maintained by the Control Program, the threshold values are found in the CDS at initialization (each NCP IPL).

For the whole machine, exhausting a threshold does not change the BER.

Table 12-1. Threshold Table

Function or Adapter	Threshold
PIO-CA	8
PIO-LA	8
AIO-1 or 2	2
ADP-CA	2
ADP-LA	2
Unresolved Level 1	2
Unresolved Level 2	2
Unresolved Level 3	2
Unresolved Level 4	2
PCI-2	2

BER Generalities

BER Generation

The MOSS creates the BERs from information supplied either by the NCP/PEP or by the MOSS itself.

If the MOSS is offline or not operational, the NCP/PEP stores the event or error information in the check record pool (CRP) located in main storage. When the CRP is full, each attempt to store more information increments a count in the CRP, but the information itself is lost. This count is entered into the last BER of the CRP (field LOST in NCP/PEP BERs). When the MOSS comes back online, the contents of the CRP are transferred to the MOSS. The Figure 12-1 on page 12-4 describes how the information is handled (see also "BER Recovery Procedures" on page 12-27).

In case of MOSS I/O errors the error information supplied by the MOSS itself is stored in a composite BER with ID 85 (see page 12-34).

Automaint builds a reference code for each BER (see page 12-19).

BER Formatting

The MOSS identifies the BER with a number and formats the information together with date, time, flag and other control bytes in the MOSS storage buffer as follows:

Table 12-2. Format of a BER

Byte Number	Contents
1-2	Total BER length in bytes
3-4	BER number (identification)
5-12	Reference code
13-18	Reserved
19	Flag
20	CCU
21-24	Time of day (binary value in seconds)
25	Month (in packed decimal)
26	Day (in packed decimal)
27	Year (in packed decimal)
28	BER Type
29	BER ID
30-nnn	Error information (hexadecimal) (nnn is the total BER length)

Notes:

1. The MOSS formats the labels for BER display, and supplies both date and time given via time services.
2. The NCP date and time of the BERs may differ from that of the MOSS. The date and time is built by the MOSS when the BER is logged on the disk, and does not necessarily match the moment this event is acknowledged by the NCP.
3. The exact layout depends on the BER type and BER ID (see the BER formats description at the end of each BER type xx section).

Byte	21	22	23	24	25	26	27
Contents	00	00	F5	8F	12	21	87
Meaning	One bit = 1 sec 62 863 sec = 17h 27m 43s				Dec	21st	87

Figure 12-2. Example of Date and Time

NCP/PEP BER Formats Versus MOSS BER Formats: The following chart explains why the BER formats and contents of NCP/PEP-generated records are different from the MOSS-generated records.

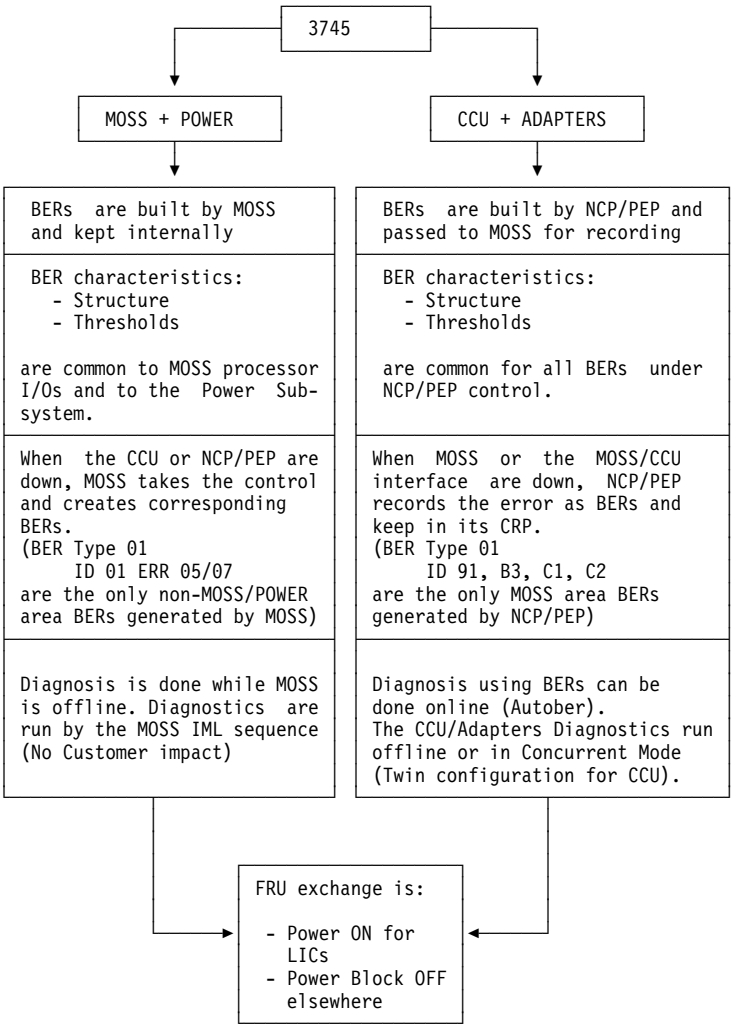


Figure 12-3. BER Formatting by MOSS and NCP/PEP

BER Storage on Disk

The MOSS stores the BERs, prepared in the MOSS RAM, on the **wraparound** BER file on disk in the order of their arrival.

When the BER file is full, the next BER to arrive overwrites the oldest BER (or BERs) in the BER file. No count is kept of such overwrites. The BER file may store several hundred BERs.

BER Storage when the Disk is not Operational: When the disk is not operational, the MOSS keeps the BERs in a buffer in the MOSS RAM. This buffer is preserved during MOSS IML (see Chapter 7). When the buffer is full, new BERs are lost, but a count of lost BERs is kept in a byte of the buffer. This is called the lost record count.

When the disk becomes operational again, MOSS stores the buffer in the BER file on disk, together with a BER giving the number of lost BERs in the event/error description line.

BER File Erasure: The entire BER file can be erased by using the DUMP/DPLY/DEL utility program. **The BER file should NOT be erased, except in exceptional cases**, since:

- It is not possible to erase individual BERs in the file, but only the entire BER file.
- The service personnel may need old BERs for history purposes.
- The BER file, when full, writes the most recent BERs on the disk space used by the 'oldest' BERs (wraparound file). When the BER file is erased, a BER is logged to that effect in the file. For more details, see *Service Functions, SY33-2055*.

BER Display

Normally, you may access the BER file on the MOSS disk using the 'ELD Function' from the console. For more details on 'How to', see *Service Functions, SY33-2055*.

The BER Detail Display Screen gives you the main information (also called 'fields') on the event represented by the BER.

Some of the fields may not appear on the BER detail display, but they are part of the BER and they are listed as they appear in the BER file. See the section 'BER Formats on Disk' page 12-128. For more details, refer to *Service Functions* manual.

BER Type and Identification

BER TYPE

The first byte of information concerning the event, points to the general area of BER occurrence:

BER Type	Description
01	MOSS-related events or errors (plus events or errors recorded by MOSS when MOSS takes control of the box, or operations such as CCU hardcheck, scanner errors).
03	Diagnostic error detection (CE option)
04	Power subsystem errors, and events reported to MOSS by the power control
08	Events/errors related to ESS operations
09	Events/errors related to 3746-900 operations
10	Events/errors related to channel adapter operations
11	Events/errors related to TSS and HPTSS operations
12	Control program exceptions (software errors detected by the hardware)
13	CCU-related events/errors when NCP/PEP has control (excluding CCU hardcheck)
14	IOC bus-related errors, when not possible to attribute them to a specific adapter
15	TRSS events/errors related to Token-Ring subsystem operations

Figure 12-4. BER Types Description

BER ID

The second byte identifies the category of error or event:

BER Created by the NCP/PEP

- bit 0 Probable cause of the error.
  - OFF: the most probable cause is the control program
  - ON : the most probable cause is the hardware or the microcode
- bits 1 to 3 Program level that recorded the error/event.
  - 001: Control program level 1
  - 010: " " " 2
  - 011: " " " 3
  - 100: " " " 4

BER Created by the MOSS: When a BER is created by the MOSS, a byte identifies the origin of the error or event.

The complete list of MOSS BER IDs is given in “MOSS BER Type 01 - Summary” on page 12-37.
Here the ID does not refer to event/error categories as in the NCP/PEP. For MOSS BERs, the event/error categories are found in another byte, called 'MOSS-CHECK'.

BER Structure

The BERs have a hierarchical structure, which allow you to go from the general problem area to the specific failing element.

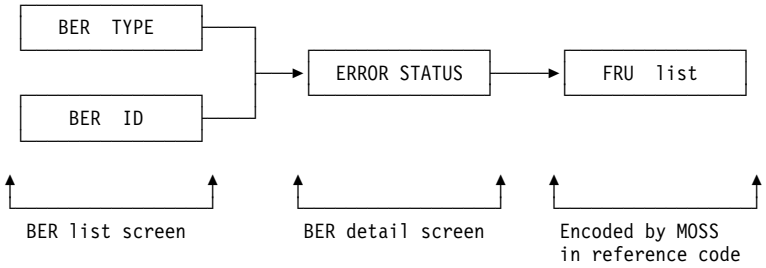


Figure 12-5. Hierarchical Structure of a BER

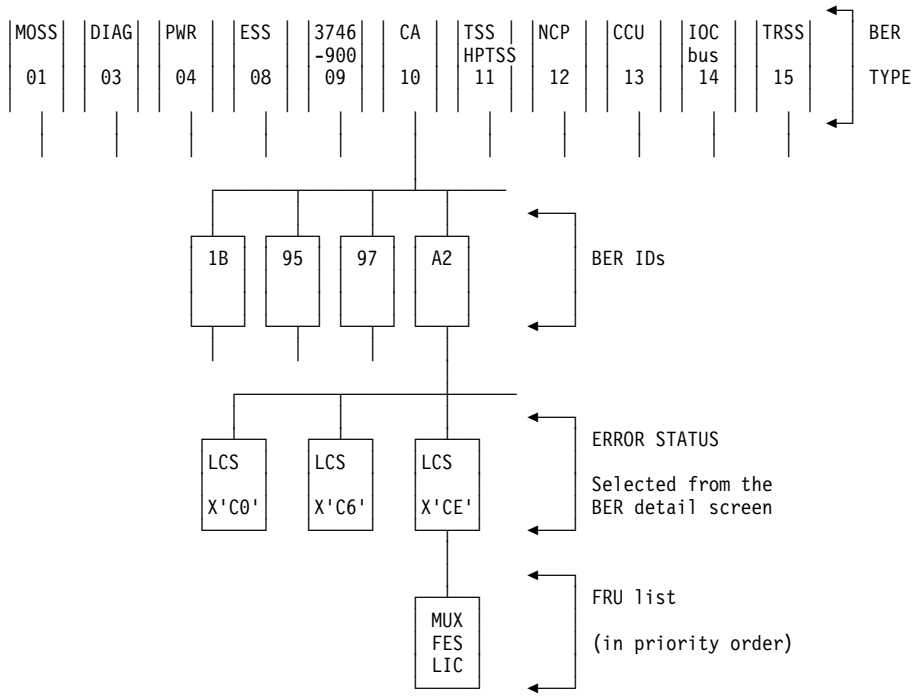


Figure 12-6. Example of a BER Tree Structure

Note: The **ERROR STATUS** is a predetermined field, characteristic of the error. BERs have a different **ERROR STATUS**, according to their TYPE and ID.

BER Handling Tools

Table 12-3. References for BER Handling

Function	Reference
Hexadecimal display at console	3745 MIP
Hexadecimal display versus MOSS BERs	MIR page 12-33
Host print request for BERs (MOSS ID 00 only)	For software information on BERs originated by NCP/PEP, refer to the associated product documentation.
BER formats	MIR, end of every 'BER Type xx' section.
BER save, purge, display	3745 Service Functions, SY33-2055.
CE BER updating	MIR, page 12-22.
CE manual analysis	MIR, page 12-22.
Auto BER analysis	MIR, page 12-21.

Examples of BER Generation

DMA TSS/HPTSS BERs (Type 11)

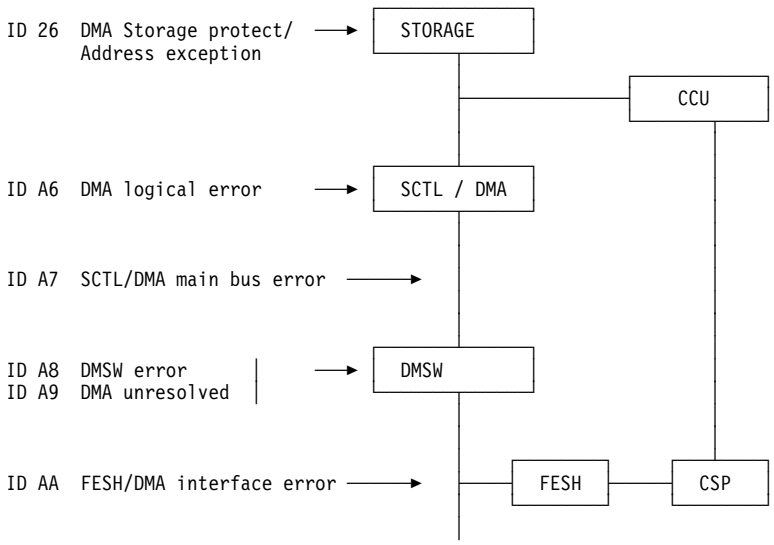


Figure 12-7. DMA TSS/HPTSS BERs

BER 08 Type 1C and BER 11 Type 1C Mechanism

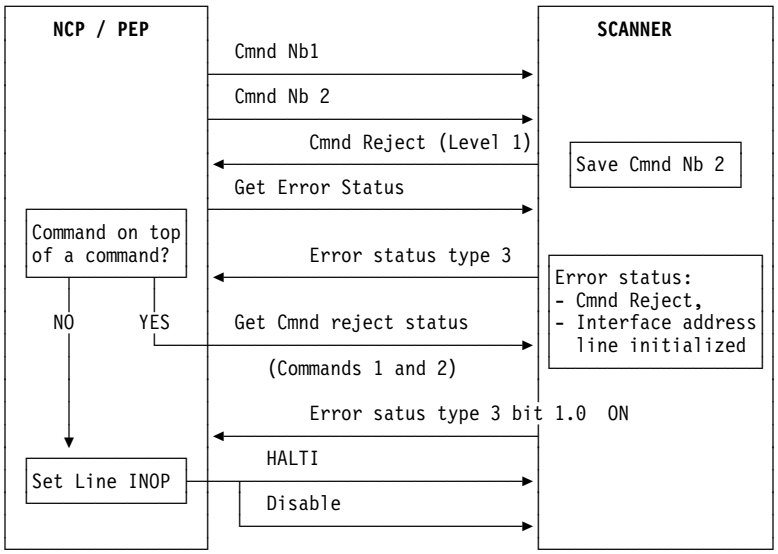


Figure 12-8. BER 08 Type 1C and BER 11 Type 1C Mechanism

NCP/PEP

- Builds BER 08 1C/11 1C, and puts it in the CRP for the MOSS
- Sets next T1C time out exit level 1. Timer will end this command with 'E4' status.

MOSS sends alert/alarm A15.

BER 08 Type B1/A4 and BER 11 Type B1/A4 Mechanism

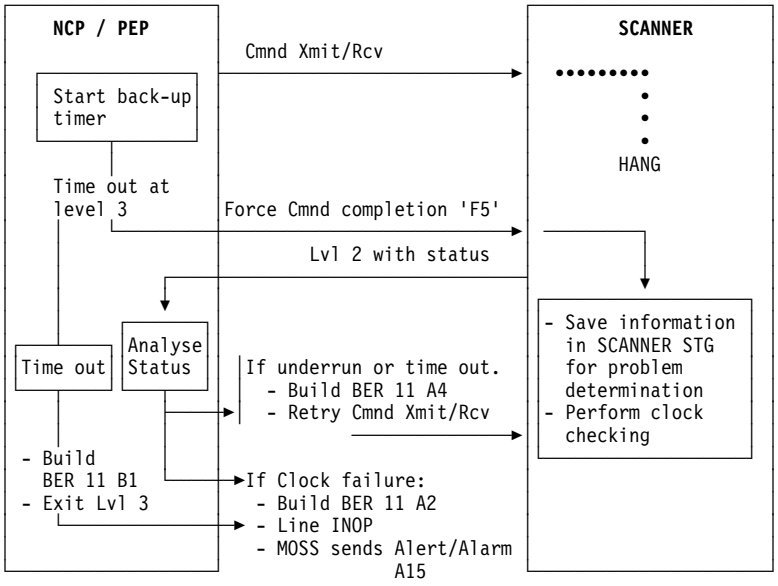


Figure 12-9. BER 08 Type B1/A4 and BER 11 Types B1/A4 Mechanism

BERs Which Are Not Machine Errors

Type	ID	EXT	Description
01	06	01	BER file deleted
		02	BER stack overflow
		07	MOSS Off line request by the operator
		12	Request to operator for fallback or switchback
	19		MOSS IML successful
	20	01	IPL complete without error
		02	IPL complete without error after fallback
		03	IPL complete without error after switchback
		04	Fallback complete without error
		05	Switchback complete without error
		06	IPL complete on standby
	21	01	IPL started
		02	IPL complete without error after fallback
		03	IPL complete without error after switchback
		04	Fallback started
		05	Switchback started
		06	IPL started on standby
	24		Concurrent maintenance started
	25		Concurrent maintenance ended
	26		Concurrent maintenance cancelled
	27		Concurrent maintenance rejected due to traffic
	28		Concurrent maintenance CA installed
	29		Concurrent maintenance CA deleted
	37		Concurrent maintenance CA changed
	38		Concurrent maintenance NCP request to cancel
	40		Fallback back-up requested
03	01		Diagnostic started
	02		Diagnostic completed succesfully
04	09		Power up of a power block
	0A		Power Control Mode change
	0B		Power ON a specific power block
	0C		Power OFF a specific power block
	0D		Set time of day
	14		Air flow detected is OK
	15		General power OFF (remote, network)
	29		End of IML data due to an event
	31		Set time of day
	34		Air filters changed
	35		Battery changed
08 11	96		Scanner disconnect state: The scanner has been disconnected by a request from the MOSS operator, and is reporting this to the Control Program.
15	96		TRM disconnect state: The TRM has been disconnected by a request from the MOSS operator, and is reporting this to the Control Program.

Figure 12-10. BERs Which Are Not Machine Errors

Specific Mechanisms

BER/Alarm/Alert Mechanism on a 3745 Major Error (3745 Down)

Whenever a 3745 down condition is detected, there is a BER/alert/alarm generation mechanism started during the 3745 re-IPL initiated by the MOSS (see table here-after). The possible causes of a 3745 down condition are:

- CCU hardcheck
- Hardware error
- Software error, hardware-detected
- Software error, software-detected.

The next table is a summary. For more details, refer to Table 12-7 on page 12-37, and to the description of the corresponding BERs.

Description	BER ID-Check-Ext field	Alert (m)	Alert (a)	Alarm (m)	Alarm (a)
IPL started	21-01	-	-	-	-
IPL completed W/O error	20-01	D0	-	D0	-
Re-IPL due to hardw. check, completed with error and dump on active CCU	06-05-05	-	27	-	27
Re-IPL due to hardw. check, completed with error and dump on standby CCU	06-05-05	-	28	-	28
Re-IPL due to hardw. check, completed with error, no dump	06-05-05	-	20	-	20
Re-IPL due to softw. error, completed W/O error, with dump (depends on abend code) on active CCU	06-05-07	-	41 42 47	-	41 42 47
Re-IPL due to softw. error, completed W/O error, with dump (depends on abend code) on standby CCU	06-05-07	-	29	-	29
Re-IPL due to softw. error, completed OK, no dump	06-05-07	-	46		46
Re-IPL due to force dump from VTAM	06-05-07	-	48		48
Re-IPL for CP abend	06-08-07	-	40		40
IPL/re-IPL completed with errors	06-03-01	D1	D1	D1	D1
IPL/re-IPL completed with error and dump	06-06-01	-	-	44	44
IPL/re-IPL completed with error, no dump	06-06-01	-	-	49	49

Figure 12-11 (Part 1 of 2). Alarm and Alerts Generated by IPL, Fallback and Switchback BERs

Description	BER ID-Check-Ext field	Alert (m)	Alert (a)	Alarm (m)	Alarm (a)
Fallback back-up started	21-04	-	-	-	-
Fallback back-up OK	20-04	B1	23	B1	23
Fallback back-up with error	22	BB	26/4B	BB	26/4B
Fallback back-up check	06-10	B3	22	B3	22
Fallback standby started	21-04	-	-	-	-
Fallback standby OK	20-04	B1	23/4A	B1	23/4A
Fallback standby with error	06-03-02	BB	26	BB	26
Fallback standby check	06-10, or 06-06-02	B3	22	B3	22
Switchback started	21-05	-	-	-	-
Switchback OK	20-03	B5	-	B5	-
Switchback with error	06-03-03	BC	-	BC	-
Switchback check	06-06-03 06-11	BD	-	BD	-
Request to network operator for fallback	06-12	B0	-	B0	-
Request to network operator for switchback	06-12	B4	-	B4	-

Figure 12-11 (Part 2 of 2). Alarm and Alerts Generated by IPL, Fallback and Switchback BERs

Notes:

In the header of the above table:

- (m) means Manual
- (a) means Automatic

Analysis of a BER/Alarm/Alert Sequence

Any error detected by the MOSS during the re-IPL checkout tests, and during the re-IPL process is also logged between the BERs signalling the start and the end of re-IPL.

Also, any pending BER found by the MOSS in the CRP, is fetched and logged during re-IPL phase 1B.

Therefore, a typical sequence would appear like this, as seen on the BER file retrieval screen, option ALL:

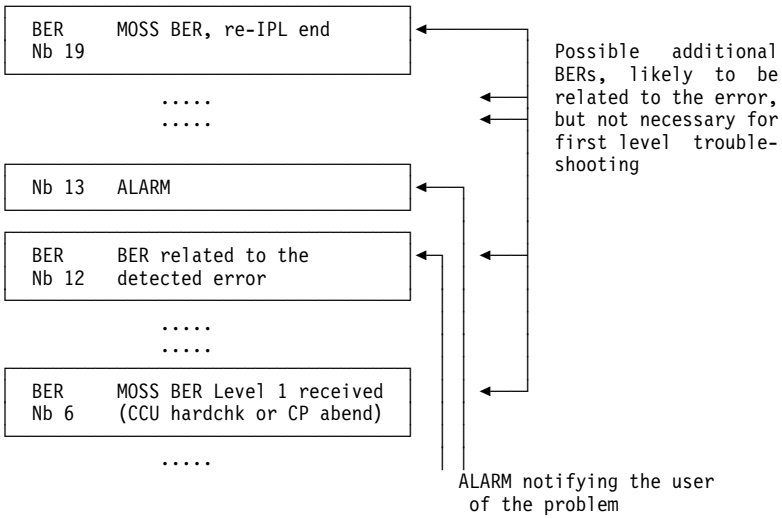


Figure 12-12. Example of a BER/Alarm/Alert Sequence

Note that BERs are displayed in inverted chronological sequence (most recent first).

BER Display

There are three kinds of BER display screens:

- BER summary
- BER list
- BER detail.

When troubleshooting, you should normally display the BER summary, then the BER list, and last the BER detail(s) pertaining to the fault. The BER display procedures and details are given in the *Service Function Manual, SY33-2055*.

Finding the Appropriate BER Detail Screen

Use the following table to find the page for BER DETAIL screen explanations for a given BER type and BER ID. This table also shows whether the C.P or the MOSS created the BER.

For software information on BERs originated by the NCP/PEP, refer to the associated product publications.

In the ELD detail screens of this chapter, 'hh..' represents an hexadecimal value, 'bbb..' a binary value.

Table 12-4. References for BER Detail Screen			
Type	**Meaning**	**Created by**	**Page Number**
01	MOSS-related BERs	MOSS	12-43 to 12-116
	All IDs except: ID 91, B3, C1, C2	NCP/PEP	12-118
03	Diagnostic	MOSS	12-140
04	Power control	MOSS	12-144
08	ESS-related BER	NCP/PEP	12-154
09	3746-900 related BER	NCP/PEP	12-162
10	CA-related BER	NCP/PEP	12-186
11	TSS/HPTSS-related BER	NCP/PEP	12-201
12	NCP/PEP related BER	NCP/PEP	12-209
13	CCU-related BER	NCP/PEP	12-212
14	IOC-related BER	NCP/PEP	12-216
15	TRSS-related BER	NCP	12-220
02	A BER type 02 may appear on the BER list file. It is the type for the alarms logged on the disk. This BER type must be ignored.		

Field Common to Many BER Detail Screens: X'76' and X'76'U: The control program stores the error information in the IOC bus error register in X'76', in order to place its contents in the BER fields. If another IOC bus error occurs while filling in the BER fields, the contents of the IOC bus error register for the second error are placed in the X'76'U field of the IOC BER.

MOSS BER IDs List

Table 12-5. List of BERs Built by the MOSS

Description	BER Type	BER ID	Refer to page
Level 0 error handler	01	00	12-43
Level 1 error handler	01	01	12-58
MAC error handler	01	02	12-60
DFA error handler	01	03	12-63
CCA error handler	01	04	12-67
MOSS/scanner	01	05	12-70 and 12-72
Events when no IPL	01	06	12-74
IPL Tasks	01	06	12-75
MOSS/TRSS	01	07	12-90
CA dump function	01	08	12-93
Disk function	01	10 11 12	12-94 and 12-94
Keyboard function	01	13	12-94
MIOC function	01	14	12-94
Mailbox interface function	01	15	12-96
MOSS-CP Interface	01	16	12-96
RSF function	01	17	12-97
IML complete with error	01	19	12-98
MOSS-CP Interface	01	1A to 1D	12-96
IPL complete with error	01	20	12-99
Fallback/Switchback	01	21	12-103
Fallback function	01	22	12-105
Concurrent maintenance	01	24 to 29	12-112
Adapter error on diags	01	30	12-112
Switch error handler	01	31	12-113
MCAD error	01	32	12-113
Backup resources test during IPL	01	33	12-115
Cyclic hour notification	01	36	12-116
Concurrent maintenance	01	37 and 38	12-112 and 12-116
MMIO interface error	01	39	12-116
Switchback twin backup	01	40	12-105
MOSS Composite BER	01	85	12-34 and 12-133
MOSS CP interface	01	91 B3 C1 C2	12-118

Note: The composite BER is displayed only in the BER list. When you choose the SEL of BER ID 85 you will see displayed the BER detail screen of the last BER built by the MOSS.

Scrolling over the composite BER detail, and using key F8 (F8: NEXT), you get only the last part of the composite BER whose description appears in the BER list. The other parts of the BER can be displayed using key F7 (F7: PREVIOUS) see page 12-34.

AutoMaint

AutoMaint Strategy

The automatic BER analysis (AutoBER) provides a **reference code** (see: “Reference Code Structure” on page 12-24). It identifies, either the faulty FRU(s), the software/microcode errors, or other error causes (for example, CP sysgen).

This reference code is sent both to the network console through alert and to the MOSS console through alarm. When the host operator receives it within the alert, the NetView panels or the *Problem Determination Guide (PDG)* for alarm, may ask him to contact the HCS/HSC, and to give them the reference code.

If NetView is not available, once the alert is received on VTAM it is logged on the LOGREC disk. In this case, the customer must consult the alarm displayed at the MOSS console.

The reference code is put in the header of the analyzed BER on disk, and:

- If an alarm must be generated, the reference code is appended to:
  - The alarm on disk, and
  - The alarm on the console.
- If an alert must be generated, the reference code is provided as one of the variable data.

Note: If alarms can always be generated when applicable, alerts need to have a CP loaded and operational to be transmitted from MOSS to NetView through NCP and VTAM. Then, it is not unusual to have some alarms with no alert.

In addition, for some specific cases, only a panel hexadecimal error code is available. Customers have to use the PDG, service personnel will refer to the MIP.

Using the ELD function, CEs and customers can have access to the complete list of alarms, BERs, reference code in the BER file itself, through the MOSS console.

In case of alarm, the CE can log specific information, which will be kept by the system (alarm).

This type of information can be useful to keep a history file of CE interventions.

The different alarms are identified through a two-digit hexadecimal value called the alarm number. When existing, related alert always carries this number through a field called Product Alert Reference Code, not to be confused with the Automain Reference Code which appears in alert through a field called IBM 3745 Reference Code.

Alerts on NetView screens are generally self explanatory. Code points transmitted in Generic Alerts are translated by NetView into understandable text, except product variable data which is displayed as specified in alert. Then if the PDG gives the list of alerts with their contents, it is only for information to customers so

that they can prepare Clists for automated operations (for example, automatic resource reactivation after a successful error recovery).

Some BERs and related alarms/alerts have no reference code, as they are only reporting major events to the external world (no case of error, for example, CCU (re-)IPL complete, or scanner (re-)IML complete).

When applicable, a valid or meaningful reference code must be retrieved from previous BER(s) and related alarm(s). In the PDG and according to the alarm number, possible causes and recommended actions are given (as for alerts).

- The customer can fix the problem by himself (for example, CP sysgen error, modem power OFF...) or,
- The customer calls the IBM hardware central service (HCS) and gives the reference code and the alarm number.

Automatic BER Analysis

The analysis automatically starts when a BER occurs:

- It is called by the BER-logging task and processes the current BER just after it has been moved from the MOSS buffer into the sector image of the disk.
- It returns control to the logging task upon completion.
- Its purpose is to:
  - Build a reference code, according to the current BER contents and/or the contents of the BER file as output of an automatic correlation process.
  - Send this reference code to the MOSS console, within the ALARM.
  - Send this reference code to the host console, within the ALERT.
  - Write the reference code(s) within the BER and the alarm on the disk

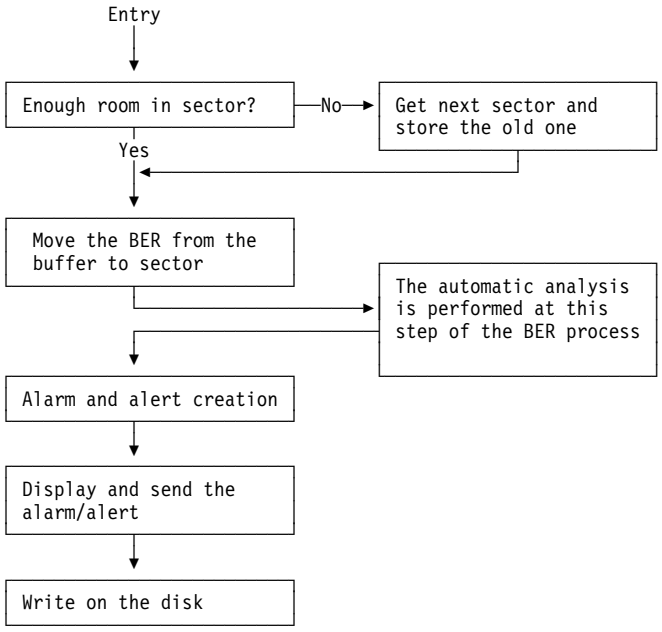


Figure 12-13. Automatic BER Analysis Process Flow

Note: Some BERs will never have an alarm/alert even if they get a reference code and only those reference codes in alarms/alerts must be considered first.

General Process Flow

The automatic BER analysis activates the following functions:

- Analysis of the type and ID of the current BER with either:
  - Direct translation of this BER into a reference code.
  - 'Other BER' analysis, when the last BER refers to another one.
  - Secondary field analysis. Analysis of fields other than type and ID, according to a decision table.
- Correlation with BERs generated before (see correlation process in the *Service Functions* manual).
- Logging of the collected information into the alarm and the alert.

All the information collected in the above steps is stored in a data block called interface block.

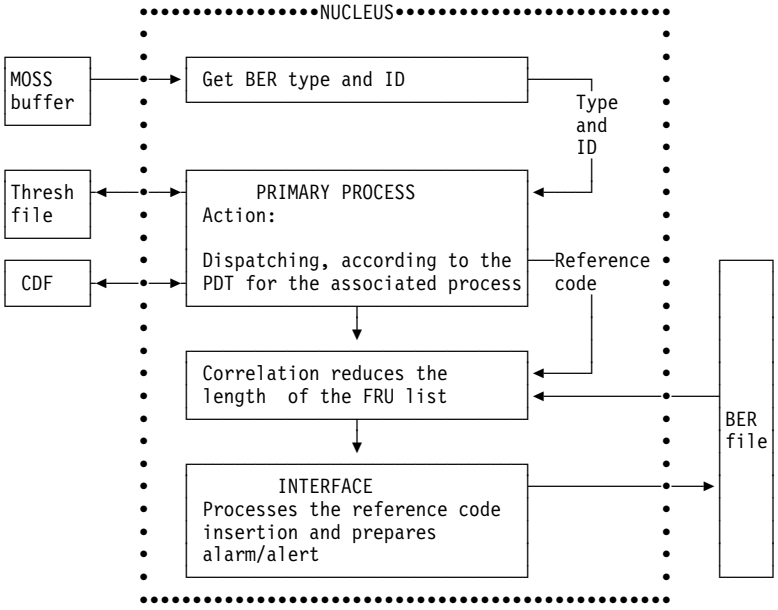


Figure 12-14. Automatic BER Analysis General Process

CE Field Updating

A 40-byte field (CE field), located at the end of the alarm, is made available to the CE so that he can leave some 'personal notes' for himsel or for another CE.

Refer to the *Service Functions* manual, for description and updating of that field.

BER Reference Code

In case of a non-permanent failure, different BERs can be logged in the BER file at different times for this intermittent failure.

The automatic process gives, for each BER, a reference code pointing either at an FRU list, or a software/microcode problem. Then the network operator can call the HCS when too many hits occur in a given period.

When the CE arrives at the customer's site and diagnostics do not reproduce the error, the CE will first try to change the FRU(s) which has (have) been called previously (see reference code interpretation), but if this method fails (immediately or in the few days following this intervention), the CE or HCS/HSC will use the MOSS BRC function through RSF:

- **Reference Code Interpretation**

  This function displays the FRU list and location, or the list of primary causes associated to a given reference code. It also displays additional information (other causes to be suspected).

Note: Reference code interpretation is also available through RETAIN/URSF and 3745 RDB.

- **Manual FRU Correlation**

  Correlation over a user's defined range of BERs.

  Correlation only applies to reference code pointing to hardware FRUs. It is only meaningful in the context of a single fault at a time.

Manual FRU Correlation

This procedure ignores the diagnostic BERs (BER type 03) reference codes.

This process correlates all FRUs called by reference codes in the range, to produce a list of suspected FRUs with a priority order based on occurence times. This process is almost the same as the one described in the FRU correlation process of the automatic BER analysis. The only differences are:

- Manual correlation gives the complete ordered FRU list (by level of occurrence), rather than a reference code (given by the automatic correlation) pointing to the most probably failing FRU(s) (1 or 2).
- Manual correlation is done in a range of BER sequence numbers selected by the CE, whereas automatic correlation is done on a predefined time range.
- No alarm/alert is generated in manual correlation.
- No reference code is generated.

Thus, by looking at all BERs (with or without alarm) occuring at box malfunction time, additional FRU(s) to be suspected can be pointed out.

Procedure: The FRU correlation procedure is described in the *Service Functions* manual.

Automatic FRU Correlation

- **Triggering**

  The correlation is started if:

  – The current BER generates an alarm by itself, and
  – The current BER is related to a hardware FRU list.

- **Correlation Range**

  The correlation process is done starting from the current BER, and going back up to the BERs logged during the last three minutes, or to the end of the file if needed.

The objective is to reduce a list of three FRUs to either two FRUs or one FRU only (as the most probable cause). If successful, the produced Refcode will be of BX... type. Refer to Figure 12-18 on page 12-26.

Reference Code Structure

3745 reference codes are generated by the microcode which runs in the MOSS to provide an automatic analysis of box event records (BERs). The reference code has eight significant digits (D1 to D8).

According to the combinations of the values of:

- D1
- D2-D3

the other fields may provide different kinds of information. (See Figure 12-18 on page 12-26 after the 2 examples below).

Reference code related to a hardware problem:

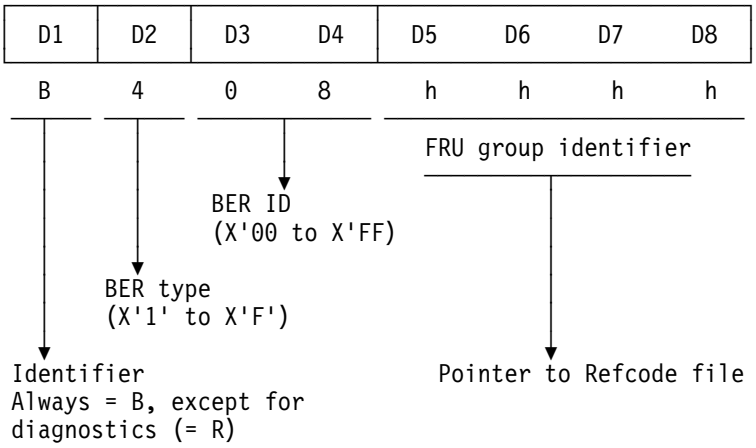


Figure 12-15. Example of a Power BER Type 4 ID 08

Reference code related to a multiple source problem:

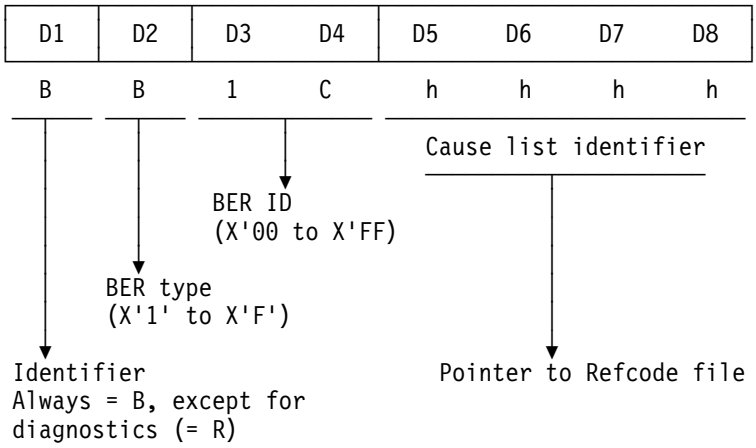
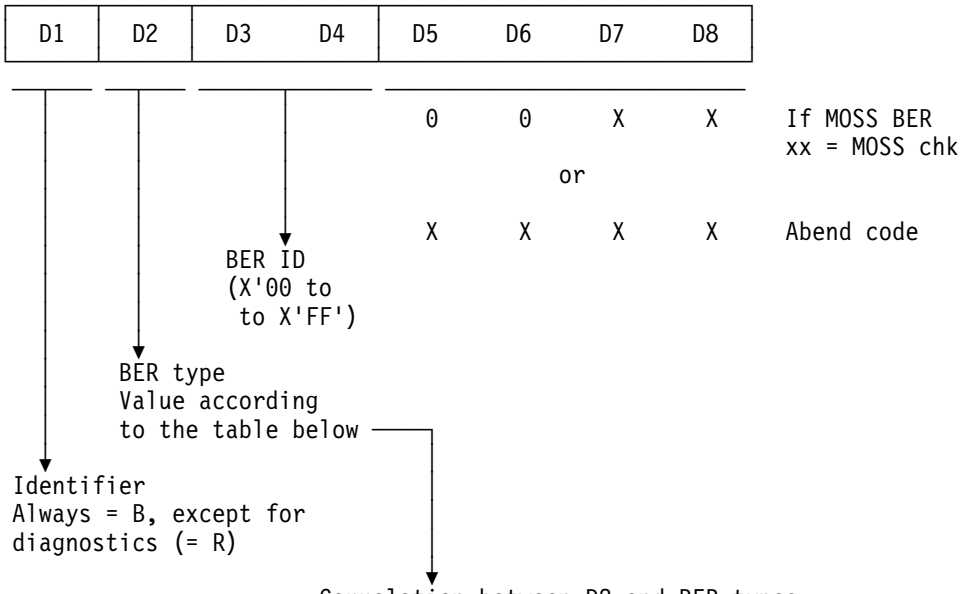


Figure 12-16. Example of a Power BER Type 11 ID 1C

Reference code related to a software/microcode problem:



Correlation between D2 and BER types

D2 value	I	L	P	Q	R	S	T	U	V	W
BER type	01	04	08	09	10	11	12	13	14	15

Figure 12-17. Example of a Software/Microcode Problem

Reference Codes.

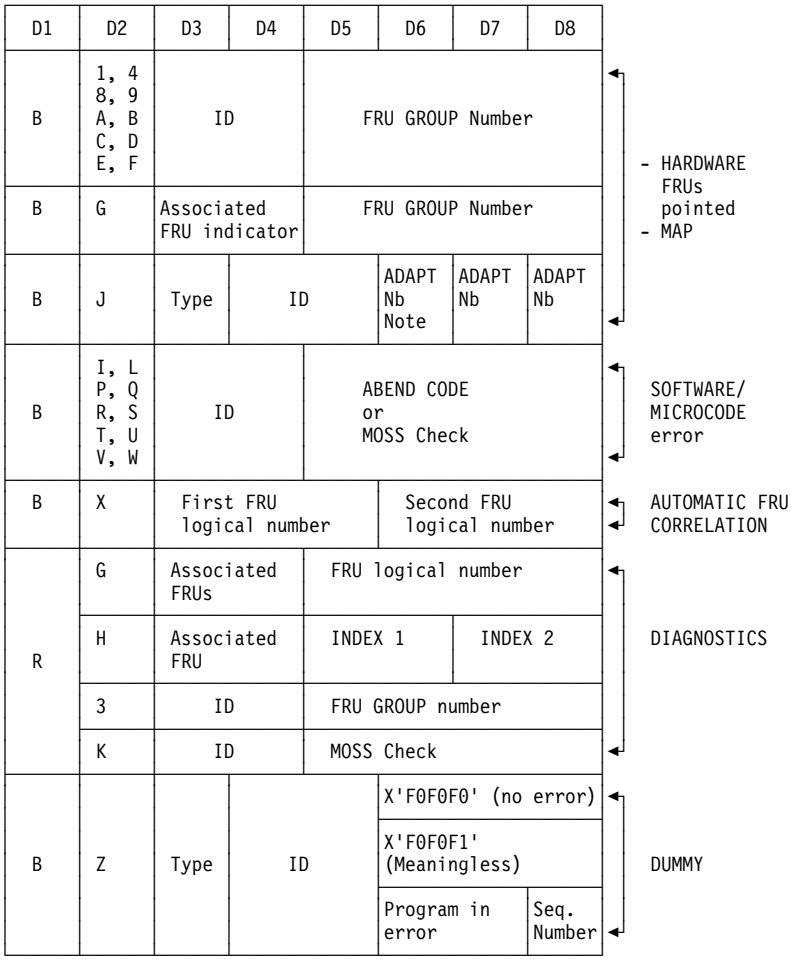


Figure 12-18. Reference Code Structure

Note: ADAPT Nb. is actually CA absolute number (displayable digit 0 to F).

The FRU list associated to a FRU group or the FRU associated to a logical number is found using the MOSS BRC function.

BER Recovery Procedures

Before being logged and stored on the disk, BERs are kept in MOSS and/or CCU storage. While in this transition stage, the BERs are volatile, and are lost if a power-OFF or power-ON reset occurs.

MOSS Handling of Catastrophic Errors

The MOSS has stored a BER in the BER stack (in MOSS storage), but could not log it on the disk. In that case, the MOSS will display the error code of the MOSS BER 01 ID 00. Display the BER using the procedure given in the *Service Function, SY33-2055*.
The remaining two digits may be interpreted by referring to page 12-45.

IOC Bus and Adapters

The following three BER types can occur for failures in this area:

- BER Type 10

  This BER occurs if an error is detected while the control program is involved in a transaction with a channel adapter.

- BER Type 08/11

  This BER occurs:

  – If an error is detected while the control program is involved in a transaction with a communication subsystem **and** the control program has identified the scanner concerned.
  – If a specific communication subsystem reports an error to the control program.

- BER Type 14

  This BER occurs if an error is detected while the control program is involved in a transaction with an adapter **and** no adapter can be identified as the source of the error.

Note: A single intermittent error can be reported as BER types 10, 11, or 14, depending on the time at which the error occurred, and the control program or microcode transaction that was taking place at that time. In this case, correlation may be useful to narrow down the range of possible failing components.

Scanner Errors Without BERs

Some errors in a communication scanner may not lead to a BER, although information within the scanner is available to help in fault isolation. Use the following procedure:

1. Start an internal or external SIT. Refer to the 3745 Service Functions.
2. When the problem occurs, stop the SIT.
3. Analyse the SIT. Use the TSS services to display the scanner storage:

   For internal SIT see also Chapter 13 of this manual.

Unresolved Interrupts

The control program logs BERs based on 'unresolved situations' (see "BER/Alarm/Alert/Mechanisms" page 12-14).

Unresolved Level 1 CA Adapter Error (BER 10 ID 9E)

There are two possible types of unresolved CA level 1 interrupts.

- A CA level 1 occurs and no bit is ON in CA external register X"E".
- There is a CA level 1 and none of the following bits is ON in CA external register X'D':
  - 0.0 IOC bus parity error
  - 0.1 internal bus parity error
  - 0.2 CCIN card check
  - 0.4 CHIN card check
  - 0.5 address compare error
  - 1.0 output exception check
  - 1.1 PIO halt remember latch
  - 1.2 cycle steal halt remember latch
  - 1.3 bus in check interface A
  - 1.5 bus in check interface B
  - 1.6 CADR card check interface A
  - 1.7 CADR card check Interface B.

The following bits are checked in X'0'. If none is ON, the control program builds a BER 10 B1:

- 0.0 (normal) initial selection interrupt
- 0.1 interface disconnect
- 0.2 selective reset
- 0.3 channel bus out check
- 0.5 stacked initial status
- 0.6 ESC status byte cleared
- 0.7 system reset.

Unresolved Level 3 CA Data/Status (BER 10 ID B2)

The following bits in are checked in X'2'. If none of these bits is set and the system reset bit in X'0' is not set (bit 0.7), the control program builds a BER 10 B2:

- 0.0 outbound data transfer sequence
- 0.1 inbound data transfer sequence
- 0.2 (final) status transfer sequence
- 0.5 channel stop/interface disconnect
- 0.6 suppress out monitor interrupt
- 1.1 data/status selective reset
- 1.3 stacked ending status.

Unresolved Level 3 CA Interrupt

If, in NCP/EP/PEP, there is no CA control block that has selected bits matching those of the interrupting CA, then a BER 10 33 is built.

Scanner, TSS, or ESS AIO Unresolved Errors (BER 08 ID 92, BER 11 ID 92)

- X'7E', bit 0.7 (IOC level 1 summary) is ON.
- X'76', bit 0.6 (adapter-initiated operation) is ON.
- X'75', bit 0.0 (AIO CSCW) is ON.

  Then, following the IOH to read the error status, one of the following bits is ON in X'76':
  - 0.4 IOC time out.
  - 0.5 IOC bus in parity error.

Scanner, TSS, or ESS Adapter Unresolved Error (BER 08 ID 9A, BER 11 ID 9A)

- In X'7E' bit 0.5 IOC adapter level 1 request.
- The error status returned an IOH read error status command = 0.

Scanner, TSS, or ESS Level 2 Unresolved (BER 08 ID A1, BER 11 ID A1)

There are 3 types of unresolved/undefined interrupts:

- A level 2 interrupt that occurs on a non-SYSGENed line.
- A level 2 interrupt from a SYSGENed line with the SCF, SES, and LCS all zero.
- A level 2 interrupt from a SYSGENed line, but the received status does not match the expected one.

CCU Level 1 Unresolved Interrupts (BER 13 ID 91)

The following bits are checked in X'7E'. If none is set, the control program builds a BER 13 91:

- 0.0 MOSS inoperative
- 0.1 any CCU hard error
- 0.3 level 5 I/O error
- 0.4 invalid operation
- 0.5 IOC adapter level 1 request
- 1.0 address compare level 1
- 1.1 address exception I fetch
- 1.2 storage protect I fetch
- 1.3 address exception program execution
- 1.4 storage protect program execution
- 1.6 IPL level 1 request.

CCU Level 3 Unresolved Interrupt (BER 13 ID B1)

This condition occurs in three different environments:

- NCP only
- PEP
- Remote NCP (from the host standpoint)

The checks are then different.

- **NCP Only**

  The following bits are checked. If none of them is set, the control program builds a BER 13 B1:

  – X'77' bit 1.0 CA level 3 interrupt
  – X'77' bit 1.1 CA level 3 interrupt
  – X'F' bit 0.2 CA level 3 initial selection request
  – X'F' bit 0.3 CA level 3 data/status request
  – X'7F' bit 0.6 user interrupt request level 3
  – X'7F' bit 1.5 internal timer interrupt level 3
  – X'7F' bit 1.6 PCI level 3.

- **PEP**

  The following bits are checked. If none of them is set, the control program builds a BER 13 B1:

  – X'F' bit 0.2 CA level 3 initial selection request
  – X'F' bit 0.3 CA level 3 data/status request
  – X'7F' bit 0.6 user interrupt request
  – X'7F' bit 1.5 internal timer level 3
  – X'7F' bit 1.6 PCI level 3.

- **Remote NCP**

  If X'77' bit 1.0 or bit 1.1 is set, and none of the following bits is set, the control program builds a BER 13 B1:

  – X'7F' bit 0.6 user interrupt request
  – X'7F' bit 1.5 internal timer level 3
  – X'7F' bit 1.6 PCI level 3.

  A BER 10 B7 is built if:

  – X'77' bit 1.0 or bit 1.1 is reset, and
  – CA is attached and installed (not defined).

  Otherwise, a BER 13 32 (level 3 interrupt configuration check) is built.

CCU Unresolved Level 4 Router (BER 13 IDs C1/C2/C3)

Two conditions may be detected by the level 4 router:

- General unresolved condition
- Unresolved with respect to a PCI Level 4.

- **General Unresolved Condition**

  If none of the following bits is set in the X'7F' when a level 4 interrupt occurs, the control program builds a BER 13 C1:

  – X'7F' bit 0.3 MOSS request service
  – X'7F' bit 0.4 MOSS response service
  – X'7F' bit 0.7 PCI level 4 interrupt
  – X'7F' bit 1.7 service request.

- **Unresolved Level 4 PCI**

  The control program builds a:

  – BER 13 C2 if X'7F' bit 0.7 is set, and no reason byte is set in the level 4 router control block.

  – BER 13 C3 if the control program cannot reset the level 4 PCI latch.

Unresolved IOC Bus Errors (BER 14 IDs 91/92)

- **Unresolved Adapter Level 1** (BER 14 91)
  – In X'7E' bit 0.5, IOC adapter level 1 request, is ON.
  – Following an IOH broadcast poll command to identify the board with the adapter problem, X'7E' bit 0.7, IOC level 1 summary, is ON.

- **Unresolved AIO Level 1** (BER 14 92)
  – X'7E' bit 0.7, IOC level 1 summary, is ON.
  – X'76' bit 0.6, adapter initiated operation, is ON.
  – X'75' is invalid. This is true when:
    - **Either**

      X'76' bit 0.2, (IOC invalid CSCW) is ON

    - **Or**

      X'76' bit 0.4, (IOC timeout) is ON
      and IOC status (X'76' bits 0.0 to 0.3) = 2.
      (No response to TA tag or cycle steal grant.

    - **Or**

      X'76' bit 0.5 (IOC Bus In parity error) is ON
      and IOC status (X'76' bits 0.0 to 0.3) = B.
      (Loading the CSCW).

- **Unresolved PIO Level 1** (BER 14 93)
  – X'7E' bit 0.7 (IOC level 1 summary) is ON.
  – X'76' bit 0.6 (adapter-initiated operation) is OFF.
  – X'76' bits 0.4 (IOC time out) and 0.5, (IOC bus in parity error) are OFF.

MOSS BER Type 01

Hexadecimal Codes

During MOSS IML, hexadecimal codes appear on the operator's panel. They are either progression codes (events), or errors.

Hexadecimal codes and BERs: The hexadecimal codes may be related to a BER. In other cases, a BER is created when the hexadecimal code is displayed.

The connection between the hexadecimal code and the BER may be done by using the time stamp (indicating when the BER was built), and by the field **Hexa Display** bytes 34 and 35 of MOSS BER foM0 page 12-128. For error decoding, see “MOSS Check Error Decoding” on page 12-33.

Table 12-6. Hexadecimal Codes Summary (Errors Only)

Hex codes	Meaning	Action	BER Created	Type of Info
001-04F	Power errors		NO	
050-17F	Error during ROS/Storage/DFA diags		NO	
180-1FE	Error during diags in RAM MOSS test		NO	
1FF	MOSS storage diag OK		NO	
Axx-Bxx	IML Stop on error (Doesn't force re-IML)	MOSS Lvl 0 interrupt	ID 00	
Cxx	MOSS re-IML threshold reached (xx MOSS IML attempts within a given period of time)	MOSS Lvl 0 interrupt	ID 00	
D00-DFF	IML Stop on Disk/Diskette error (Doesn't force re-IML) (D00 = MOSS dump complete)	MOSS Lvl 0 interrupt	ID 00	
	MOSS Level 0 re-entry (re-IML)	MOSS Lvl 0 interrupt		
	MOSS Level 0 re-entry while in re-IML	MOSS Lvl 0 interrupt		
F00	Start of MOSS dump			
F01	MOSS dump complete			
F10-F61	IPL check		ID 00 ERR 06	Code to suspected FRU list
FD0	Fallback complete		ID 06 ERR 11 or ID 20 ERR 02	Indications about anomaly
FD1	Fallback complete with error		ID 06 ERR 03 EXT 02 or ID 22	Indications about anomaly
FD2	Switchback complete		ID 20 ERR 03	Indications about anomaly
FD3	Swichback complete with error		ID 06 ERR 06 EXT 03	Indications about anomaly
FEx	IML complete with error		ID 19	
FFA	Status/Progression steps wich occur during the IPL sequence; IPL has completed but has detected a PCA1 adapter error. Local console may not be accessible.		ID 06 ERR 03	
FFE	IPL complete with error		ID 06 ERR 03	
FFF	IPL canceled after error detection		ID 06 ERR 06	

Hexadecimal Codes Versus MOSS BER ID 00

The control panel displays a blinking hexadecimal code when the MOSS is unable to build the corresponding BER. You may find the information concerning this BER, by using the following procedure:

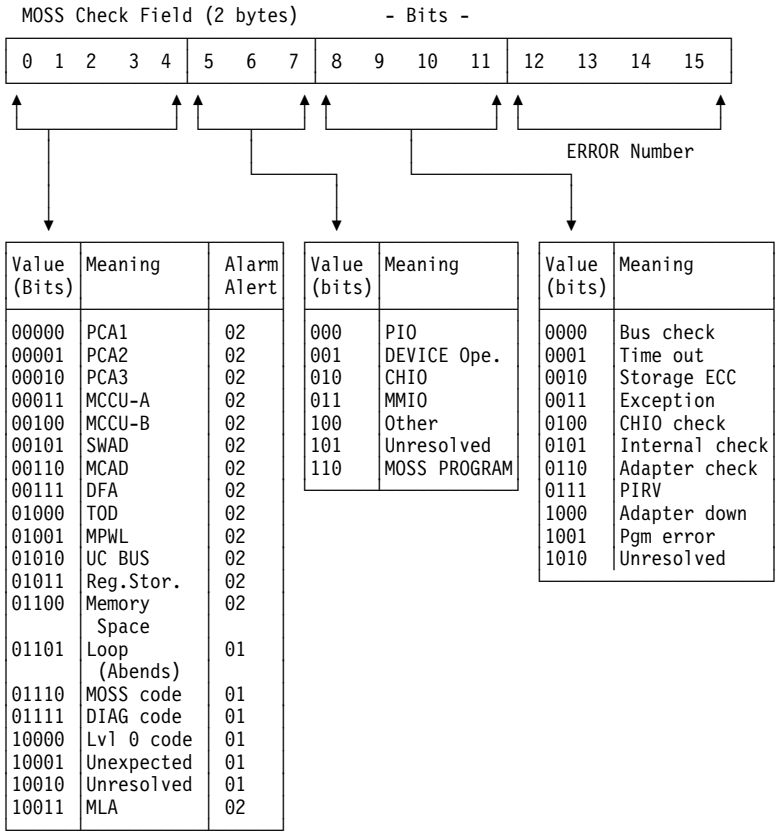
1. Try to re-IML the MOSS
2. Use the function DDD (dump, display, delete), with the address given by the parameter 'CHGHVBER', see *Service Functions, SY33-2055*. (See “MOSS BER Type 01 ID 00 - Error Code Description” on page 12-45 for details).

MOSS Check Error Decoding

All the MOSS check codes described in the list on Table 12-9 on page 12-45 have the following decoding.

When the faulty FRU or FRUs given by the hexadecimal code list in the 3745 MIP is exhausted and the error persists, or is transient (intermittent), it is advisable to analyze the corresponding BER, if any.

In the MOSS BER ID 00, the contents of the **MOSS CHECK** field (see: Figure 12-18 on page 12-26) is very helpful to analyze the error. The figure below shows the information provided in this field.



Value (Bits)	Meaning	Alarm Alert
00000	PCA1	02
00001	PCA2	02
00010	PCA3	02
00011	MCCU-A	02
00100	MCCU-B	02
00101	SWAD	02
00110	MCAD	02
00111	DFA	02
01000	TOD	02
01001	MPWL	02
01010	UC BUS	02
01011	Reg.Stor.	02
01100	Memory Space	02
01101	Loop (Abends)	01
01110	MOSS code	01
01111	DIAG code	01
10000	Lvl 0 code	01
10001	Unexpected	01
10010	Unresolved	01
10011	MLA	02

Value (bits)	Meaning
000	PIO
001	DEVICE Ope.
010	CHIO
011	MMIO
100	Other
101	Unresolved
110	MOSS PROGRAM

Value (bits)	Meaning
0000	Bus check
0001	Time out
0010	Storage ECC
0011	Exception
0100	CHIO check
0101	Internal check
0110	Adapter check
0111	PIRV
1000	Adapter down
1001	Pgm error
1010	Unresolved

Figure 12-19. Decoding of the MOSS Check Field

Alert/alarm 02 indicates that during the error, a re-IML is performed and a dump is taken.

Composite BER

The MOSS stacks all BERs which can be produced all along a given request, in a composite BER (Type 01 ID 85) and only the last BER stacked asks for the queueing in the BER buffer pool. the example above The composite BER is a variable-byte buffer (see page 12-133).

Scrolling over a composite BER detail, and using key F8 (F8: NEXT), you get only the last part of the composite BER whose description appears in the BER list. The other parts of the BER can be displayed using key F7 (F7: PREVIOUS).

Four cases lead to a BER reporting activity:

1. A MOSS function requests an I/O operation and a hardware error is reported to the level 0 of the adapter code and finally, to the task itself.

   The selected command sets a pointer to the composite BER buffer, clears the data area, initializes the composite BER header and sends the I/O request. When the I/O error is reported to the level 0 of the MOSS control code, and only when that error is not recoverable, the level 0 identifies the failing adapter, and stacks the BER (Type 01 ID 00).
   The level 0 control code then schedules the machine check information of the adapter.

   According to the kind of event or error, one of the following BERs is created:

   - `Moss/MAC HLIR   ..... Type 01 ID 02`
   - `Moss/MAC CAC    ..... Type 01 ID 02`
   - `Disk file adapter CAC ..... Type 01 ID 03`
   - `Keyboard display adapter ... Type 01 ID 04`
   - `Power adapter ..... Type 01 ID 39`

   MOSS gets control back at the end of the invoked command and calls, when an error is found, a control code function which stacks a second BER according to the called function:

   - `Disk function  ..... Type 01 ID 10, 11, 12`
   - `MOSS console ..... Type 01 13`
   - `MIOC function  ..... Type 01 14`
   - `Mailbox interface function.. Type 01 15`
   - `MOSS-CP interface ..... Type 01 16`
   - `RSF MOSS function ..... Type 01 17`

   Then this function queues the composite BER in the buffer pool. The composite BER may contain a variable number of BERs, but usually, it contains three BERs.

   Composite BER (Type 01, ID 85) example: If a MOSS Lvl 0 occurs during a disk I/O operation related to a LOAD request from an application, a BER 01 85 is logged. (Assume that, for this example, it is **SEL# 233**). This BER contains:

   - SEL# 233.3 BER 01 11 Disk adapter
   - SEL# 233.2 BER 01 03 CAC
   - SEL# 233.1 BER 01 00 Level 0

   A selection number for a BER 01 85 is displayed with the event description related to the latest BER put into the BER 01 85. You may scroll from the BER

DETAIL screen to display the other BERs contained in BER 01 85 using F7: PREVIOUS.

In the previous example, the event description first displayed on the BER DETAIL screen for SEL# 233 will refer to SEL# 233.3 BER 01 11.

- Pressing 'F7: PREVIOUS' will display SEL# 233.2 BER 01 03.
- Pressing 'F7: PREVIOUS' a second time will display SEL# 233.1 BER 01 00.

If you scroll forward to SEL# 233 from SEL# 232 using 'F8: NEXT', the first detail displayed is SEL#233.3. You must then use 'F7: PREVIOUS' to display SEL# 233.2 and SEL# 233.1 as described above.

2. A MOSS function has requested an I/O operation and a hardware error is reported to the adapter code and finally to the task itself.

   This case is basically identical to case 1, except for level 0 processing. In the above case, the composite BER contains two BERs.

3. No active MOSS function requests an I/O operation, but a hardware error is reported to MOSS level 0 and to the adapter code. Level 0 handles the process and uses its own composite BER buffer. The machine check micro-code queues the composite BER in a buffer. In this case, the composite BER contains two BERs.

4. No active MOSS function requests an I/O operation, but a hardware error is reported to the adapter.

   This case is basically identical to case 3 except for the level 0 processing. In this case, the composite BER contains one BER. The composite BER process is automatically done by the microcode.

MOSS BERs Used With the IPL Application:

The following BERs are used by the MOSS in connection with an IPL application:

ID	Err. code	Ext	Description	Format
06	03	01	IPL complete + errors (1)	FoM6
	03	02	IPL after fallback complete + errors (standby mode) (1)	"
	03	03	IPL after switchback complete + errors (1)	"
	06	01	IPL check	"
	06	02	IPL after fallback check (standby)	"
	06	03	IPL after switchback check	"
	05	05	CCU hardcheck as alert support	F0M19
	05	07	Program request as alert support	"
	08	05	CCU hardcheck as alarm support	FoM9
	08	07	Program request as alarm support	FoM19
	09		CLDP abend as alarm support	FoM10
	10		Fallback check	FoM13
	11		Switchback check	"
	12		Request to network operator	FoM11
20	01		IPL complete without errors	FoM21
	02		IPL after fallback complete W/O errors (standby)	"
	03		IPL after switchback complete W/O errors	"
	04		Fallback complete without errors	"
	05		Switchback complete without errors	"
21	01		IPL started	FoM23
	02		IPL after fallback started (standby)	
	03		IPL after switchback started	
	04		Fallback started	
	05		Switchback started	
22			Fallback complete with errors	FoM20
40			Switchback twin backup	FoM20

Figure 12-20. MOSS BER Used With IPL Application

Note: (1) Non-blocking errors.

MOSS BER Type 01 - Summary

Table 12-7 (Page 1 of 6). MOSS BER Type 01 Summary

BER ID	MOSS Chk code	BER Add Fld	Event Description	Recovery or PGM Action	ALERT	ALARM
00			See MOSS-CHECK code for software error See MOSS-CHECK code for hardware error		01 02	01 02
01	01		See MOSS 01 ID 01 field description	MOSS retry	NO	NO
01	02		See MOSS 01 ID 02 field description	MOSS retry	NO	NO
01	02		IOC operation error during MIOH (CCU to MOSS status A register, X'11', bit 0)	MOSS retry	NO	NO
01	02		IOC operation error (limit threshold)	MOSS down	NO	03
01	03		Adapter clock check (MCC status register 2, bit 4)	MOSS retry	NO	NO
01	03		Adapter clock check (limit threshold)	MOSS down	NO	03
01	04		CCU clock check (MCC status register 2, bit 3)	MOSS retry	NO	NO
01	04		CCU clock check (limit threshold)	MOSS down	NO	03
01	05		CCU hardcheck detected (CCU to MOSS status A register, X'11', bit 6). Upon detection of this event, MOSS will automatically start a CCU automatic re-IPL. See Specific Mechanism, page 12-14	NCP re-IPL		
01	07		MOSS TRSS interface		NO	NO
01	08		CA dump function		NO	NO
01	09		Address exception check in CCU (CCU to MOSS status A register, X'11', bit 5)	MOSS down	NO	03
01	0A		MOSS/MIOC operation check, CCU detected (CCU to MOSS status A register, X'11', bit 7)	MOSS down	NO	03
02	any		CCU logical interface	MOSS down	NO	03
02	any		CCU logical interface	MOSS fnct message	NO	NO
03	any		Disk drive and/or adapter error CNT=10 DEVICE CODE=X'02', X'04', X'06'	MOSS inop	07	07
03	any		Diskette file error CNT not 10 and DEVICE CODE = X'07'	MOSS inop	06	06
03	any		Disk drive and/or adapter error CNT = 10 and DEVICE CODE = X'01'	MOSS inop	04	04
03	any		Disk file error CNT not 10 and DEVICE CODE = X'03', X'05'	MOSS inop	05	05
04	0A		Local console CAC detected exception interface	Console not available	0A	0A
04	0C		Local console CAC detected error (interface)		0A	0A
04	40		Local console error (device) (CCA basic status register bits 4 and 5)		0B	0B
04	8A, 8C		Remote console interface error		0C	0C
04	C0		Remote console error (device)		0D	0D

Table 12-7 (Page 2 of 6). MOSS BER Type 01 Summary

BER ID	MOSS Chk code	BER Add Fld	Event Description	Recovery or PGM Action	ALERT	ALARM
05	F0		MOSS-scanner interface error. SOFT re-IML OK, DUMP OK. Error detected by MOSS levels 1 or 4, when communicating with a scanner: • MCC status register 1, bit 6, at level 4 • CCU to MOSS status A register X'11' bit 0	MOSS fnct message	61	61
05	F0		MOSS-scanner interface error. SOFT re-IML OK, DUMP KO. Error detected by MOSS levels 1 or 4, when communicating with a scanner: • MCC status register 1, bit 6, at level 4 • CCU to MOSS status A register X'11' bit 0, and X'76' bits 0.6 or 0.7, at level 1	MOSS funct. message	65	65
05	F0		MOSS-scanner interface error SOFT re-IML KO, DUMP OK. Error detected by MOSS levels 1 or 4, when communicating with a scanner: • MCC status register 1, bit 6, at level 4 • CCU to MOSS status A register X'11' bit 0, and X'76' bits 0.6 or 0.7, at level 1	MOSS funct. message	TSS: 62 HPTSS: 72	TSS: 62 HPTSS: 72
05	F0		MOSS-scanner interface error HARD re-IML OK, DUMP OK. Error detected by MOSS levels 1 or 4, when communicating with a scanner: • MCC status register 1, bit 6, at level 4 • CCU to MOSS status A register X'11' bit 0, and X'76' bits 0.6 or 0.7, at level 1	MOSS funct. message	67	67
05	F0		MOSS-scanner interface error HARD re-IML OK, DUMP KO Error detected by MOSS levels 1 or 4, when communicating with a scanner: • MCC status register 1, bit 6, at level 4 • CCU to MOSS status A register X'11' bit 0, and X'76' bits 0.6 or 0.7, at level 1	MOSS funct. message	68	68
05	F0		MOSS-scanner interface error HARD re-IML KO, DUMP OK. Error detected by MOSS levels 1 or 4, when communicating with a scanner: • MCC status register 1, bit 6, at level 4 • CCU to MOSS status A register X'11' bit 0, and X'76' bits 0.6 or 0.7, at level 1)	MOSS funct. message	TSS: 6B HPTSS: 72	TSS: 6B HPTSS: 72
05	F0		MOSS-scanner interface error. HARD re-IML KO, DUMP KO. Error detected by MOSS levels 1 or 4, when communicating with a scanner: • MCC status register 1, bit 6, at level 4 • CCU to MOSS status A register X'11' bit 0, and X'76' bits 0.6 or 0.7, at level 1.	MOSS funct. message	TSS: 66 HPTSS: 72	TSS: 66 HPTSS: 72
06	01		BER file deleted (via MOSS command)	File purged	NO	NO
06	02		BER stack overflow in MOSS storage.(MOSS maintains a 5K-bytes buffer to stack incoming BERs, before logging on)		NO	NO

Table 12-7 (Page 3 of 6). MOSS BER Type 01 Summary

BER ID	MOSS Chk code	BER Add Fld	Event Description	Recovery or PGM Action	ALERT	ALARM
06	03	01	IPL complete with errors. Some errors do not prevent the completion of IPL: • Scanner not IMLed successfully • Bad parameters passed by control program • Errors in CA monitoring task • Error found on the diskette which is not detrimental for the IPL • Console or console adapter error Corresponding BERs are in the BER File. There is a message on the console.	IPL completion	D1	D1
06	03	01	IPL of stand-by is complete with errors (see before)		D4	D4
06	03	02	Fallback in stand-by mode check (manual)		BB	BB
06	03	03	Switchback check		BC	BC
06	04		LAxx (Lines xxxx-yyyy) IML failed		6A	6A
06	05	05	NCP re-IPL end and no dump MOSS creates this entry to end the re-IPL and generate the Alert reporting the error which caused the re-IPL. CCU hardcheck BER as alert support (see Specific Mechanism, page 12-14)		20	20
06	05	05	NCP re-IPL end and dump MOSS creates this entry to end the re-IPL and generate the Alert reporting the error which caused the re-IPL. CCU hardcheck BER as alert support (see Specific Mechanism, page 12-14)		27	27
06	05	05	Dump of failing CCU is available after fallback in stand-by mode		28	28
06	05	07	NCP re-IPL end and no dump. MOSS creates this entry to end the re-IPL and generate the Alert reporting the error which caused the re-IPL. CCU re-IPL on program request (see Specific Mechanism, page 12-14)		46	46
06	05	07	NCP re-IPL end and dump, and ABENDs : 910, 911, 930, 931. MOSS creates this entry to end the re-IPL and generate the Alert reporting the error which caused the re-IPL. CCU re-IPL on program request (see Specific Mechanism, page 12-14)		41	41
06	05	07	NCP re-IPL end and dump and ABENDs : 912, 915 (mismatch sysgen/re-IPL). MOSS creates this entry to end the re-IPL and generate the Alert reporting the error which caused the re-IPL. CCU re-IPL on program request (see Specific Mechanism, page 12-14)		42	42

Table 12-7 (Page 4 of 6). MOSS BER Type 01 Summary

BER ID	MOSS Chk code	BER Add Fld	Event Description	Recovery or PGM Action	ALERT	ALARM
06	05	07	NCP re-IPL end and dump, and ABEND 7FFF. MOSS creates this entry to end the re-IPL and generate the Alert reporting the error which caused the re-IPL. CCU re-IPL on program request (see Specific Mechanism, page 12-14)		48	48
06	05	07	NCP re-IPL end and dump, other abends. MOSS creates this entry to end the re-IPL and generate the Alert reporting the error which caused the re-IPL. CCU re-IPL on program request (see Specific Mechanism, page 12-14)		47	47
06	05	07	Dump of failing CCU is available after fallback		28	28
06	06	01	IPL complete with check, hardware cause. The MOSS microcode action is dependent upon the kind of NCP IPL or IML error found, see hexadecimal display. IPL check Fxx		NO	25
06	06	01	IPL complete with errors, dump on disk. The MOSS microcode action is dependent upon the kind of NCP IPL or IML error found, see hexadecimal display. IPL check Fxx		NO	44
06	06	01	IPL complete with errors, no dump on disk The MOSS microcode action is dependent upon the kind of NCP IPL or IML error found, see hexadecimal display. IPL check Fxx		NO	49
06	06	01	IPL of stand-by CCU failed	Stopped	D3	D3
06	06	02	IPL after fallback failed (manual)		B3	B3
06	06	03	IPL after switchback failed		BD	BD
06	07		MOSS off-line request by operator	MOSS off-line	B7	B7
06	08	05	NCP re-IPL for CCU hardcheck. CCU to MOSS status A register, bit 6. See BER 01 01 05 which precedes it. This BER allows MOSS to create an Alarm. See Specific Mechanism, page 12-14	IPL process phase 1B	NO	24
06	08	07	NCP re-IPL for Control Program abend Control Program abend, no BER in CRP (Ext register X'79' bit 0.2, raising CCU to MOSS register X'11' bit 1 in MOSS). See BER 01 01 07 which precedes it. This BER allows MOSS to create an Alarm. See Specific Mechanism, page 12-14	IPL process phase 1B	NO	40
06	09		CLDP check. (Output X'70' with cause of check in external register X'72' bytes 0 and 1). Hex display indication at control panel.	IPL stopped	NO	D2
06	09		CLDP check on stand-by CCU		D3	D3
06	10 10 11 11 12 12		Fallback check (manual) Automatic fallback check Switchback check Automatic fallback on a twin back-up complete without error Request for switchback Request to network operator for fallback on a twin stand-by		B3 22/4C BD 23 B4 B0	B3 22/4C BD 23 B4 B0
06	13		Timed IPL will occur soon		NO	D9

Table 12-7 (Page 5 of 6). MOSS BER Type 01 Summary

BER ID	MOSS Chk code	BER Add Fld	Event Description	Recovery or PGM Action	ALERT	ALARM
06	14		Timed IPL is cancelled		NO	D8
06	18		LSSD string first part		NO	NO
06	28		LSSD string second part		NO	NO
07			TRSS MOSS BER		NO	NO
08			Error on MOSS/TRSS interface		NO	NO
10			DISK macro		NO	NO
11			DISK macro		NO	NO
12			DISK macro		NO	NO
13			KBD macro		NO	NO
14			MIOC function, MOSS to CCU		NO	NO
15			Mailbox in request		NO	NO
16			CCU buffer request		NO	NO
17			RSF BER (See Specific Mechanism, page 12-14)		NO	NO
18			Scanner re-IMLed successfully		09	NO
19			MOSS IML successful or with non-blocking errors		0F	0F
1A			CHIO		NO	NO
1B			Power error		NO	NO
1C			SWAD adapter error		NO	NO
1D			MCAD adapter error		NO	NO
1E			LAN handler check		NO	NO
20	01 02 03 04 05 06		IPL completed without error, IPL W/O error after fallback manual, stand-by IPL W/O error after switchback Fallback completed without error Switchback without error IPL complete on standby		D0 B1 B5 B1/23/4A B5 NO	NO B1 B5 B1/23/4A B5 NO
21	01 02 03 04 05 06		IPL started IPL after fallback IPL after switchback Fallback started Switchback started IPL started on standby		NO NO NO NO NO NO	NO NO NO NO NO NO
22			Manual fallback complete with error		BB	BB
22			Automatic fallback complete with error		26/4B	26/4B
23			37CS RE-IML complete		13	13
24			Concurrent maintenance started		C0	C0
25			Concurrent maintenance ended		C1	C1
26			Concurrent maintenance cancelled		C2	C2
27			Concurrent maintenance rejected due to traffic		C3	C3
28			Concurrent maintenance CA installed		C5	C5
29			Concurrent maintenance CA deleted		C4	C4
2A			ESCA RE-IPL failed		14	14
2B			See ORIGIN field page 12-112.			
2C			DL2 call completion		NO	NO

Table 12-7 (Page 6 of 6). MOSS BER Type 01 Summary

BER ID	MOSS Chk code	BER Add Fld	Event Description	Recovery or PGM Action	ALERT	ALARM
2D			CP dump transfer error. Dump purged		NO	NO
2E			3746-900 general IML		6C	NO
2E			LAN selective IML		6C	NO
2E			ESCA selective IML		6E	NO
30			MOSS warning adapter(s) during IML		10	10
31			MOSS SWAD error		02	02
32			MOSS MCAD error		02	02
33			Back-up resources test during IPL		NO	NO
36			Cyclic hour notification		NO	NO
37			Concurrent maintenance CA changed		C6	C6
38			Concurrent maintenance NCP request to cancel		C7	C7
39			MMIO interface error		AB	AB
40			Switchback back-up requested		NO	NO
41			Repair action started		NO	NO
42			Repair action end		NO	NO
50			Remote console rejected		NO	10
85			Composite BER is handled for each BER		NO	NO
91			Lvl 1 interrupt MOSS down passed to Control Program by MOSS (MCC status reg 1, bit 3 giving a X'7E' input register bit 0.0 in the CCU) BER built by Control Program, and saved in the CRP. If this BER is in the diskette BER file, it means that it has been passed to the MOSS, when the MOSS was re-IMLed and set on-line. Reason for MOSS down might be found in the BER file itself, by looking at other BERs built by the MOSS, which triggerred the MOSS inop bit in MCC status register.	MOSS down	03	NO
A0			MOSS/MOSS-E token ring adapter error	NO	NO	
A1			MOSS/MOSS-E link lost		11	11
A2			MOSS/MOSS-E link re-opened		12	12
A3			MOSS transient error		NO	NO
A4			See page 12-122 for details.		NO	NO
B3			CP/MOSS connection OUT mailbox command. Time out at level 3 in Control Program	MOSS down	03	NO
C1			CP/MOSS connection OUT mailbox request error at level 4 in Control Program	MOSS down	03	NO
C2			CP/MOSS connection IN mailbox command error at level 4 in Control Program	MOSS down	03	NO

MOSS BER Type 01 ID 00 - Detailed BER Display

BER format foM0: see page 12-128. The MOSS microcode level 0 generates 3 displays. They consist in a fixed part and a part which displays the fields concerned by the type of error.

Fixed part:

```
                                  ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:00 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                <REF. CODE IN CHAR.> CCCCCCCC
  MOSCHK:hhhh CPLLPL:hh CM:hh  MM:hh CHM:hh CHCV:hhhh CHIOP:hhhhhhhh
  MODULE:hhhhhhhh  DUMP:hh hh IA:hhhhhhhh MS:hhhhhhhh RS:hhhh
  DIV:hhhh EIRV:hh IOIRV:hh PIRV:hh PSCI:hhhhhhhh OP:hhhhhhhh
  DIV:hhhh EIRV:hh IOIRV:hh PIRV:hh PSCI:hhhhhhhh OP:hhhhhhhh
  REGS:hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh
       hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh


 (Here are displayed the two lines of the changing part - group 1, 2
  or 3-  the groups are described below)

  ..............................................................
  ..............................................................
```

Changing Part of MOSS BER Type 01 ID 00

1. Errors about the PCAs (hex codes A01-A0F), the DFA or TOD (hex codes A8D, AAA, and Dxx), and MOSS BER Type 01 ID 80:

   ```
   DFA:hh hh hh  TOD:hh
   PCA1:hh hh hh hh hh  PCA2:hh hh hh hh hh  PCA3:hh hh hh hh hh
   ```

2. Errors about the MCCU-A or MCCU-B or the SWAD (hex codes A10 to A83):

   ```
   MCCU A:hhhh hhhh hhhh hhhh hhhh hhhh    SWAD:hh hh hh hh
   MCCU B:hhhh hhhh hhhh hhhh hhhh hhhh
   ```

3. Errors about the MCAD, without any register displayed (hex codes A84 to A8C, and AAB to CFF):

   ```
   MCAD:hh hh hh hh hh hhhh hh hhhh hh
   SNAP:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
   ```

4. MLA error (hex code AE8 to AEB)

   ```
   MLA:hhhhhhhh hhhh
   ```

MOSS BER Type 01 ID 00 - Field Description

Table 12-8. MOSS BER Type 01 ID 00 Field Description

Field name	Meaning	Refer to
MOSS-CHECK	MOSS error code.	page 12-33
EIRV	Error interrupt request vector	page 12-51
DIV	Diagnostic information vector	page 12-51
IOIRV	I/O interrupt request vector	page 12-51
PIRV	Program interrupt request vector	page 12-51
CPLLPL	Current/last priority level	page 12-51
CM	Common mask	page 12-52
MM	Master mask	page 12-52
CHM	Channel mask	page 12-52
CHCV	Channel control vector	page 12-52
IA	Instruction address of the last level interrupted by level 0	page 12-52
PSCI	Program status code indicator of the interrupted level	page 12-52
LOPC	Last operation code.	page 12-52
MS	Main storage address (Parity detected)	
RS	Register storage address (parity detected in MSC)	
OP	Op code at error time	
SNAP	Snapshot dump	page 12-57
STAT CNT	Error count for each adapter	
CHIOP	CHIO pointer register (current)	
DUMP	Dump/IML request	page 12-53
EIRV1	EIRV in case of MOSS level 0 re-entry.	page 12-51
IOIRV1	IORV in case of MOSS level 0 re-entry	page 12-51
PIRV1	PIRV in case of MOSS level 0 re-entry	page 12-51
DIV1	DIV in case of MOSS level 0 re-entry	page 12-51
LOPC1	Last operation code (level 0 re-entry)	page 12-52
PCA1	PCA1 status registers	page 12-55
PCA2	PCA2 status registers	page 12-55
PCA3	PCA3 status registers	page 12-55
MCCU-A	MCCU-A status registers	page 12-53
MCCU-B	MCCU-B status registers	page 12-53
SWAD	SWAD status registers	page 12-54
MCAD	MCAD status registers	page 12-54
DFA	DFA status registers	page 12-56
TOD	TOD status register	page 12-56
REGS	MOSS processor registers	page 12-52
MLA	MOSS LAN adapter (only for MOSS check 9800)	page 12-57

MOSS BER Type 01 ID 00 - Error Code Description

The encoding of the MOSS-CHECK bytes is explained on page 12-33.

Table 12-9 (Page 1 of 6). MOSS BER Type 01 ID 00 Error Codes Description

Field Name	Hexa Code	MOSS Check Code (Hexa)	Description
PCA1	A01	0580	Adapter down
	A02	0000	PIO bus check (inbound parity)
	A03	0001	PIO bus check (adapter not detected)
	A04	0010	PIO time out (outbound address parity check)
	A05	0011	PIO time out (outbound cmd/data parity check)
PCA2	A06	0D80	Adapter down
	A07	0800	PIO bus check (inbound parity)
	A08	0801	PIO bus check (adapter not detected)
	A09	0810	PIO time out (outbound address parity check)
	A0A	0811	PIO time out (outbound cmd/data parity check)
PCA3	A0B	1580	Adapter down
	A0C	1000	PIO bus check (inbound parity)
	A0D	1001	PIO bus check (adapter not detected)
	A0E	1010	PIO time out (outbound address parity check)
	A0F	1011	PIO time out (outbound cmd/data parity check)

Table 12-9 (Page 2 of 6). MOSS BER Type 01 ID 00 Error Codes Description

Field Name	Hexa Code	MOSS Check Code (Hexa)	Description
MCCU-A	A10	1D80	Adapter down
	A11	1D81	Adapter down (too many spurious error)
	A12	1C60	Adapter check (bus counter parity)
	A13	1C61	Adapter check (MIOC/CCU time out parity)
	A14	1A00	CHIO bus check
	A15	1A10	CHIO time out
	A16	1A20	CHIO storage ECC (RS data parity during MS)
	A17	1A21	CHIO storage ECC (multiple bits in DIV)
	A18	1A22	CHIO storage ECC (no bit in DIV)
	A19	1A30	CHIO exception address (MS data access)
	A1A	1A31	CHIO exception oper (CHCV invalid)
	A1B	1A32	CHIO exception register (CHP 0 7 not zero)
	A1C	1A33	CHIO exception spec (inv addr MS data access)
	A1D	1A34	CHIO exception (multiple bits in DIV)
	A1E	1A35	CHIO exception (no bit in DIV)
	A1F	1A50	CHIO internal check (cache parity)
	A20	1A51	CHIO internal check (inv addr on CHP access)
	A21	1A52	CHIO internal check (multiple bits in DIV)
	A22	1A60	CHIO adapter check (step counter parity)
	A23	1A61	CHIO adapter check (hw/burst counter parity)
	A24	1A62	CHIO adapter check (CCU busy time out)
	A25	1A63	CHIO adapter check (MIOC time out)
	A26	1A64	CHIO adapter check (MIOC parity check in)
	A27	1A65	CHIO adapter check (MIOC parity check out)
	A28	1A66	CHIO adapter check (adapter failure)
	A29	1A67	CHIO adapter check (multiple bits in STAT register)
	A2A	1A68	CHIO adapter check (no CHIO in progress in ACB)
	A2B	1AA0	CHIO (multiple bits in EIRV)
	A2C	1AA1	CHIO (no CHIO in progress in ACB)
	A2D	1960	Dev adapter check (step counter parity)
	A2E	1961	Dev adapter check (MIOC time out)
	A2F	1962	Dev adapter check (MIOC parity check in)
	A30	1963	Dev adapter check (MIOC parity check out)
	A31	1964	Dev adapter check (adapter failure)
	A32	1965	Dev adapter check (multiple bits in STAT register)
	A33	1966	Dev adapter check (no CAC running)
	A34	1800	PIO bus check (inbound parity)
	A35	1801	PIO bus check (adapter failure)
	A36	1802	PIO bus check (adapter not detected)
	A37	1810	PIO time out (invalid command)
	A38	1811	PIO time out (outbound parity check)
	A39	1812	PIO time out (adapter not detected)
	A3A	1813	PIO time out (adapter failure)
	A3B	1814	PIO time out (multiple bits in STAT register)

Table 12-9 (Page 3 of 6). MOSS BER Type 01 ID 00 Error Codes Description

Field Name	Hexa Code	MOSS Check Code (Hexa)	Description
MCCU-B	A3C	2580	Adapter down
	A3D	2581	Adapter down (too many spurious error)
	A3E	2460	Adapter check (bus counter parity)
	A3F	2461	Adapter check (MIOC/CCU time out parity)
	A40	2200	CHIO bus check
	A41	2210	CHIO time out
	A42	2220	CHIO storage ECC (RS data parity during MS)
	A43	2221	CHIO storage ECC (multiple bits in DIV)
	A44	2222	CHIO storage ECC (no bit in DIV)
	A45	2230	CHIO exception address (MS data access)
	A46	2231	CHIO exception oper (CHCV invalid)
	A47	2232	CHIO exception register (CHP 0 7 not zero)
	A48	2233	CHIO exception spec (inv addr MS data access)
	A49	2234	CHIO exception (multiple bits in DIV)
	A4A	2235	CHIO exception (no bit in DIV)
	A4B	2250	CHIO internal check (cache parity)
	A4C	2251	CHIO internal check (inv addr on CHP access)
	A4D	2252	CHIO internal check (multiple bits in DIV)
	A4E	2260	CHIO adapter check (step counter parity)
	A4F	2261	CHIO adapter check (hw/burst counter parity)
	A50	2262	CHIO adapter check (CCU busy time out)
	A51	2263	CHIO adapter check (MIOC time out
	A52	2264	CHIO adapter check (MIOC parity check in)
	A53	2265	CHIO adapter check (MIOC parity check out)
	A54	2266	CHIO adapter check (adapter failure)
	A55	2267	CHIO adapter check (multiple bits in STAT register)
	A56	2268	CHIO adapter check (no CHIO in progress in ACB)
	A57	22A0	CHIO (multiple bits in EIRV)
	A58	22A1	CHIO (no CHIO in progress in ACB)
	A59	2160	Dev adapter check (step counter parity)
	A5A	2161	Dev adapter check (MIOC time out)
	A5B	2162	Dev adapter check (MIOC parity check in)
	A5C	2163	Dev adapter check (MIOC parity check out)
	A5D	2164	Dev adapter check (adapter failure)
	A5E	2165	Dev adapter check (multiple bits in STAT register)
	A5F	2166	Dev adapter check (no CAC running)
	A60	2000	PIO bus check (inbound parity)
	A61	2001	PIO bus check (adapter failure)
	A62	2002	PIO bus check (adapter not detected)
	A63	2010	PIO time out (invalid command)
	A64	2011	PIO time out (outbound parity check
	A65	2012	PIO time out (adapter not detected)
	A66	2013	PIO time out (adapter failure)
	A67	2014	PIO time out (multiple bits in STAT register)

Table 12-9 (Page 4 of 6). MOSS BER Type 01 ID 00 Error Codes Description

Field Name	Hexa Code	MOSS Check Code (Hexa)	Description
SWAD	A68	2D80	Adapter down
	A69	2D81	Adapter down (too many spurious error)
	A6A	2C60	Adapter check (internal clock check 1)
	A6B	2C61	Adapter check (internal clock check 2)
	A6C	2C62	Adapter check (multiple bits in DI register)
	A6D	2960	Dev adapter check (state counter parity)
	A6E	2961	Dev adapter check (shift pulse counter parity)
	A6F	2962	Dev adapter check (ground fault detection)
	A70	2963	Dev adapter check (interface check)
	A71	2964	Dev adapter check (interface time out)
	A72	2965	Dev adapter check (interface parity check)
	A73	2966	Dev adapter check (multiple bits in EBSTAT)
	A74	2967	Dev adapter check (switch interface error)
	A75	2968	Dev adapter check (switch driver fault)
	A76	2969	Dev adapter check (switch serial link parity)
	A77	296A	Dev adapter check (switch invalid command)
	A78	296B	Dev adapter check (multiple bits in dv STAT)
	A79	296C	Dev adapter check (adapter failure)
	A7A	296D	Dev adapter check (no CAC running)
	A7B	2800	PIO bus check (inbound parity)
	A7C	2801	PIO bus check (adapter failure)
	A7D	2802	PIO bus check (adapter not detected)
	A7E	2810	PIO time out (invalid command)
	A7F	2811	PIO time out (outbound parity check)
	A80	2812	PIO time out (overrun)
	A81	2813	PIO time out (adapter not detected)
	A82	2814	PIO time out (adapter failure)
	A83	2815	PIO time out (multiple bits in STAT register)
MCAD	A84	3580	Adapter down
	A85	3000	PIO bus check (inbound parity)
	A86	3001	PIO bus check (adapter failure)
	A87	3002	PIO bus check (adapter not detected)
	A88	3010	PIO time out (invalid command)
	A89	3011	PIO time out (outbound parity check
	A8A	3012	PIO time out (adapter not detected)
	A8B	3013	PIO time out (adapter failure)
	A8C	3013	PIO time out (multiple bits in STAT register)

Table 12-9 (Page 5 of 6). MOSS BER Type 01 ID 00 Error Codes Description

Field Name	Hexa Code	MOSS Check Code (Hexa)	Description
DFA	A8D	3D80	Adapter down
	A8E	3A00	CHIO bus check
	A8F	3A10	CHIO time out
	A90	3A20	CHIO storage ECC (RS data parity during MS)
	A91	3A21	CHIO storage ECC (multiple bits in DIV)
	A92	3A22	CHIO storage ECC (no bit in DIV)
	A93	3A30	CHIO exception (oper CHCV invalid)
	A94	3A31	CHIO exception (register CHP 0-7 not zero)
	A95	3A32	CHIO exception (spec inv addr MS data access)
	A96	3A33	CHIO exception (address MS data access)
	A97	3A34	CHIO exception (multiple bits in DIV)
	A98	3A35	CHIO exception (no bit in DIV)
	A99	3A50	CHIO internal check (cache parity)
	A9A	3A51	CHIO internal check (inv addr on CHP access)
	A9B	3A52	CHIO internal check (multiple bits in DIV)
	A9C	3AA0	CHIO multiple bits in EIRV
	A9D	3AA1	CHIO no CHIO in progress in ACB
	A9E	3800	PIO bus check (inbound parity)
	A9F	3801	PIO bus check (adapter failure)
	AA0	3802	PIO bus check (adapter not detected)
	AA1	3810	PIO time out (invalid command)
	AA2	3811	PIO time out (outbound address parity check)
	AA3	3812	PIO time out (outbound cmd/data parity check)
	AA4	3813	PIO time out (adapter failure)
	AA5	3814	PIO time out (multiple bits in STAT register)
TOD	AA6	4580	Adapter down
	AA7	4000	PIO bus check (inbound parity)
	AA8	4001	PIO bus check (adapter not detected)
	AA9	4010	PIO time out (outbound address parity check)
	AAA	4011	PIO time out (outbound cmd/data parity check)
PLC	AAB	4B80	Adapter down
	AAC	4B00	MMIO write error
	AAD	4B10	MMIO time out
	AAE	4B30	MMIO exception (address)
	AAF	4B20	MMIO read error
	AB0	4BA0	MMIO not authorized on this level
UC bus	AB1	5580	Adapter down
Register storage	AB2	5820	PIO storage ECC (MPC data parity)
	AB3	5821	PIO storage ECC (MSC data parity)
	AB4	5822	PIO storage ECC (unresolved)
	AB5	5C20	Storage ECC (during PSV swap)
Storage	AB6	6220	CHIO storage ECC (data parity)
	AB7	6520	Storage ECC (data parity)
	AB8	6521	Storage ECC (I-fetch parity)
Loop	AB9	6DA0	Detected
MOSS code	ABA	7590	Pgm error (IO address not authorized)
Diag	ABB	7C90	Pgm error (POR/start unresolved)

Table 12-9 (Page 6 of 6). MOSS BER Type 01 ID 00 Error Codes Description

Field Name	Hexa Code	MOSS Check Code (Hexa)	Description
Level0	ABC	8590	Pgm error (WHO invalid in CPRET)
	ABD	8591	Pgm error (WHO invalid in PPRET)
	ABE	8592	Pgm error (WHO invalid in XPRET)
	ABF	8593	Pgm error (pgm state unexpected)
	AC0	8594	Pgm error (invalid adapter ID in CHGH0BUS)
	AC1	8595	Pgm error (RAM processor state unexpected)
	AC2	8596	Pgm error (ROS processor state unexpected)
	AC3	8597	Pgm error (CALL stack full)
	AC4	8598	Pgm error (RET stack empty)
	AC5	8599	Pgm error (error code not in BER table)
	AC6	859A	Pgm error (MOSS IMLed routine before IML)
Unexpected	AC7	8A40	CHIO
	AC8	8DA0	Interrupt level 0
	AC9	8D60	IOIRV interrupt level 0
	ACA	8800	PIO bus check (no last level)
	ACB	8801	PIO bus check (not IO instruction)
	ACC	8802	PIO bus check (on level 2)
	ACD	8803	PIO bus check (unexpected on level 6)
	ACE	8810	PIO time out (no last level)
	ACF	8811	PIO time out (not IO instruction)
	AD0	8812	PIO time out (on level 2)
	AD1	8813	PIO time out (unexpected on level 6)
	AD2	8C70	PIRV pgm request
Unresolved	AD3	9530	Exception address (I fetch)
	AD4	9531	Exception address(MS data access)
	AD5	9532	Exception fixed point overflow
	AD6	9533	Exception (inv addr on non MS access)
	AD7	9534	Exception (multiple bits in DIV)
	AD8	9535	Exception (multiple bits in EIRV)
	AD9	9536	Exception oper (invalid opcode)
	ADA	9537	Exception register (precision)
	ADB	9538	Exception spec (inv addr on I fetch)
	ADC	9539	Exception spec (inv addr on MS data access)
	ADD	953A	Exception spec (inv addr on non GPR access)
	ADE	953B	Exception spec (inv execution of ki)
	ADF	953C	Exception spec (PSV bits 40-44-47 not zero)
	AE0	9550	Internal check (cache register parity check)
	AE1	9551	Internal check (inv address on GPR access)
	AE2	9552	Internal check (inv address on PSV swap)
	AE3	9553	Internal check (multiple bits in DIV)
	AE4	9554	Internal check (multiple bits in EIRV)
	AE5	9520	Storage ECC (multiple bits in DIV)
	AE6	9521	Storage ECC (multiple bits in EIRV)
	AE7	9522	Storage ECC (no bit in DIV)
MLA	AE8	9B80	Adapter down
	AE9	9B30	MMIO exception
	AEA	9B20	MMIO read error
	AEB	9BA0	MMIO not authorized on this level
Specific	Cxx	76xx	PIRV (abend request)
	Dxx	3Cxx	Disk adapter return code

BER Type 01 ID 00 - Fields Details

Some of the following fields may not appear on the BER detail display, but they are part of the BER and they are listed as they appear in the BER file. See the section 'BER Formats on Disk' page 12-128.

Table 12-10 (Page 1 of 7). BER Type 01 ID 00 Field Details

Field Name	Bit Pattern	Description
DIV (byte 1)		Diagnostic information
	0 0	Sector must be zero
	. . 1	Error occurred during main store operation.
	. . . 1	Error occurred during a register backing store operation
	. . . . 0 0 0 0	DMA identification must be zero
DIV (byte 2)		Sector specification
	1	Exception memory subsystem detected an invalid address
	. 1	Error occurred during a PSV swap operation
	. . 1	Operation exception: attempt to execute an invalid instruction
	. . . 1	A register precision occurred (result > 24 bits)
	. . . . 1 . . .	Address exception: address > '7FFFFF'X or wrapped to zero
	. . . . . 1 . .	Error occurred during an instruction fetch
	. . . . . 1 .	Fixed point overflow
	 1	External error loaded in EIRV/DIV
EIRV		Error interrupt request vector
	1	I/O control check
	. 1	Time out check
	. . 1	Storage data/ECC check
	. . . 1	Exception (addr,op,spec.)
	. . . . 1 . . .	Channel I/O check
	. . . . . 1 . .	Internal control check
	. . . . . 1 .	Instruction address modifier (IA points to the beginning of the instruction)
	 0	Unused (must be zero)
IOIRV		I/O interrupt request vector
	1	MAC adapter check
	. 1	MAC high LVL interrupt or 100 ms timer interrupt
	. . 0	Power control interrupt request
	. . . 1	MCA interrupt request
	. . . . 1 . . .	MAC low level interrupt
	. . . . . 1 . .	DFA interrupt request
	. . . . . 0 0	Unused (must be zero)
PIRV		Programmed interrupt request vector
	1	MOSS error level 0 handler
	. 1	MOSS error level 0 process
	. . 1	Power control interrupt request
	. . . 1	MOSS MCA level 3 handler
	. . . . 1 . . .	MOSS MAC level 4 handler
	. . . . . 1 . .	MOSS DFA level 5 handler
	. . . . . 1 .	MOSS suervisor level 6 and task scheduler
	 1	MOSS task level 7 programms
CPLLPL		Current/last priority level
	0	Unused (must be zero)
	. x x x	Current priority level (000 to 111)
	. . . . 0 . . .	Unused (must be zero)

Table 12-10 (Page 2 of 7). BER Type 01 ID 00 Field Details

Field Name	Bit Pattern	Description
	. . . . . x x x	Last priority level (000 to 111)
CM		Common mask interrupt vector
	1	Level 0 enabled
	. 1	Level 1 enabled
	. . 1	Level 2 enabled
	. . . 1	Level 3 enabled
	. . . . 1 . . .	Level 4 enabled
	. . . . . 1 . .	Level 5 enabled
	. . . . . 1 .	Level 6 enabled
	 1	Level 7 enabled
MM		Master mask interrupt vector
	0000 000 .	Unused (must be zero)
	 1	Enabled
CHM		Channel mask interrupt vector
	0000 000.	Unused (must be zero)
	 1	Enabled
CHCV (byte 1)		Channel control vector
	0000 0 . . .	Unused (must be zero)
	. . . . . x . .	Channel pointer number 0 = CPR within set 12-15 1 = CPR within set 8-11
	. . . . . x .	Indirect operation 0 = Mode determined by bit 1.1 1 = Indirect mode
	 x	0 = Short address 1 = Long address
CHCV (byte 2)		
	x	0 = Write 1 = Read
	. x	0 = Indirect mode (Must be 0 if bit 0.6 is 1) 1 = Direct mode
	. . x x x x x .	CHCV pointer number
	 x	0 = CHCV (0-6) used 1 = CHCV (0-6) not used
IA (byte 1)		Interrupted address
	0000 0000	Unused (must be zero)
IA (bytes 2-4)		Address
PSCI (byte 1)		Program status code indicator register space
	0000 0000	Unused (must be zero)
PSCI (byte 2)	0000 0 . . 0	Unused (must be zero)
	. . . . . 1 . 1	Restricted address branch mode (64 K domain only)
	. . . . . 1 .	Master mode PIO and Reg indirect
PSCI (byte 3)	1	Z indicator
	. 1	H indicator
	. . xx xxxx	Secondary set number
PSCI (byte 4)	1	C indicator
	. 1	V indicator
	. . xx xxxx	Primary set number
LOPC1		Last operation code address
bytes 1-2	hh hh	1st part of the address
bytes 3-4	hh hh	2nd part of the address
REGS		Registers of interrupted level

Table 12-10 (Page 3 of 7). BER Type 01 ID 00 Field Details

Field Name	Bit Pattern	Description
28-51 Prim. set 52-75 Sec. set	xxxxxx xxxxxx xxxxxx xxxxxx	
Dump		MOSS dump/IML info
IML information	1	Dump requested
(IML request)	. 1	Re-IML requested
	. . 00	Unused (must be zero)
	 xxxx	Re-IML count
DUMP status		MOSS dump file status
	0000 0000	File free
	 1	Enabled
MCCU-A/B		MCCU-A/B status register 0
byte 1	1	MOSS inoperative
	. 1	Step/bus counter parity
	. . 1	MIOC/CCU counter parity
	. . . 1	HW/Burst counter parity
	. . . . 1 . . .	CCU busy time out
	. . . . . 1 . .	MIOC time out
	. . . . . 1 .	MIOC parity check in
	 1	MIOC parity check out
byte 2	1	Invalid PIO Cmd
	. 1	UC bus parity check
	. . 1	Unused
	. . . 1	MIOC busy
	. . . . 1 . . .	CHIO halt
	. . . . . 1 . .	Equipment check
	. . . . . 1 .	Enable interrupt level 0
	 1	Interrupt level 0 (read only)
MCCU A/B		MCCU A/B status register 1
byte 3	0000 0 . . .	Unused
	. . . . . 1 . .	Enable CCU HLIR
	 00	Unused
byte 4	0000 0 . . .	Unused
	. . . . . 1 . .	CCU HLIR
	. . . . . 1 .	Enable all interrupts
	 1	Interrupt level 1
MCCU A/B		MCCU A/B status register 4
byte 5	000	Unused
	. . . 1	Enable cycle steal end
	. . . . 1 . . .	Enable CCU LLIR
	. . . . . 1 . .	Enable CSP IOC1 interrupt
	. . . . . 1 .	Enable CSP IOC2 interrupt
	 0	Unused
byte 6	1	Programm wait
	. 00	Unused
	. . . 1	Cycle steal end
	. . . . 1 . . .	CCU LLIR
	. . . . . 1 . .	CSP IOC1 interrupt
	. . . . . 1 .	CSP IOC2 interrupt
	 1	Interrupt level 4
MCCU A/B		MCCU A/B MMOD register (see notes on page 8-18)
byte 7	1	Not used
	. 1	Step 0
	. . 1	Step 1
	. . . 1	Freeze
	. . . . 1 . . .	MIOC direct oper mode
	. . . . . 1 . .	MIOC write mode (CHIO)
	. . . . . 1 .	MIOC read mode (CHIO)
	 1	DREG full

Table 12-10 (Page 4 of 7). BER Type 01 ID 00 Field Details

Field Name	Bit Pattern	Description
byte 8		Reserved for diagnostics
	1	Parity prediction diag 1
	. 1	Parity prediction diag 0
	. . 1	MIOC diag 2
	. . . 1	MIOC diag 1
	. . . . 1 . . .	MIOC diag 0
	. . . . . 1 . .	MOSS diag 2
	. . . . . 1 .	MOSS diag 1
	 1	MOSS diag 0
byte 9	xxxx xxxx	MCCU A/B count register
byte 10	xxxx xxxx	MCCU A/B count register
byte 11	xxxx xxxx	CHCV register
byte 12	xxxx xxxx	CHCV register
SWAD byte 1		SWAD basic status register
	000	Device address
	. . . 1	Command rejected (Inv.PIO)
	. . . . 1 . . .	UC bus parity check
	. . . . . 1 . .	Equipment check
	. . . . . 1 .	Enable interrupt level 0
	 1	Interrupt level 0
SWAD byte 2		SWAD extend basic status register
	1	Overrun (EIRV error)
	. 1	State counter parity check
	. . 1	Shift counter parity check
	. . . 1	Ground fault detection
	. . . . 1 . . .	TOD interrupt
	. . . . . 1 . .	Interface check
	. . . . . 1 .	Interface time out
	 1	Interface parity check
SWAD byte 3		SWAD device status register
	xxx	Device address phase 2
	. . . 1	Switch device interrupt error
	. . . . 1 . . .	Switch device driver fault
	. . . . . 1 . .	Serial link parity check
	. . . . . 1 .	Switch device invalid command
	 1	Phase 1/2 status
SWAD byte 4		SWAD disconnect register
	1	Switch / MOSS inoperative
	. 1	Sense disconnect SWL-A
	. . 1	Sense disconnect SWL-B
	. . . 1	Sense Switch/MOSS inoperative
	. . . . 1 . . .	Internal clock check Nb 1
	. . . . . 1 . .	Internal clock check Nb 2
	. . . . . 1 .	Disconnect SWL-A
	 1	Disconnect SWL-B
MCAD (byte 1)		MCAD INTP1 register
	1	Invalid PIO command
	. 1	UC bus parity check
	. . 00 0 . . .	Unused
	. . . . . 1 . .	Equipment check
	. . . . . 1 .	Enable interrupt level 1
	 1	Interrupt level 1
MCAD (byte 2)		MCAD EINTP1 register
	1	Enable timer
	. 1	Enable CA 1-8 HLIR
	. . 1	Enable CA 9-16 HLIR
	. . . 1	Unused
	. . . . 1 . . .	100 ms timer
	. . . . . 1 . .	CA 1-8 HLIR
	. . . . . 1 .	CA 9-16 HLIR
	 1	Unused
MCAD (byte 3)		MCAD INTP4 register

Table 12-10 (Page 5 of 7). BER Type 01 ID 00 Field Details

Field Name	Bit Pattern	Description
	1	Enable fault flags
	. 1	Enable CA 1-8 LLIR
	. . 1	Enable CA 9-16 LLIR
	. . . 1	Unused
	. . . . 1 . . .	Fault flags
	. . . . . 1 . .	CA 1-8 LLIR
	. . . . . . 1 .	CA 9-16 LLIR
	 1	Interrupt level 4
MCAD (byte 4)		MCAD sense fault flags
	1	Fault ENA/REST 1-2
	. 1	Fault ENA/REST 3-4
	. . 1	Fault ENA/REST 5-6
	. . . 1	Fault ENA/REST 7-8
	. . . . 1 . . .	Fault ENA/REST 9-10
	. . . . . 1 . .	Fault ENA/REST 11-12
	. . . . . 1 .	Fault ENA/REST 13-14
	 1	Fault ENA/REST 15-16
MCAD (byte 5)		MCAD diagnostics register
	1	All CAs disabled
	. 000	Unused
	 xxxx	Force error (See note 7 on page 8-21)
MCAD (byte 6)		MCAD sense CA enable
	1	CA 1 enabled
	. 1	CA 2 enabled
	. . 1	CA 3 enabled
	. . . 1	CA 4 enabled
	. . . . 1 . . .	CA 5 enabled
	. . . . . 1 . .	CA 6 enabled
	. . . . . 1 .	CA 7 enabled
	 1	CA 8 enabled
MCAD (byte 7)		MCAD sense CA enable
	1	CA 9 enabled
	. 1	CA 10 enabled
	. . 1	CA 11 enabled
	. . . 1	CA 12 enabled
	. . . . 1 . . .	CA 13 enabled
	. . . . . 1 . .	CA 14 enabled
	. . . . . 1 .	CA 15 enabled
	 1	CA 16 enabled
MCAD (byte 8)		MCAD CAMPOR register
	0000	Unused
	. . . . 1 . . .	CA 1-8 nohold(reset by 'reset adapter' cmd)
	. . . . . 1 . .	CA 9-16 nohold (reset by 'reset adapter' cmd)
	. . . . . 1 .	CA 1-8 MOSS POR
	 1	CA 9-16 MOSS POR
MCAD		MCAD ENCA register
bytes 9-10	xxxx xxxx	Each bit enables a CA from 1 to 16
	xxxx xxxx	
MCAD		MCAD CARST register
bytes 11-12	xxxx xxxx	Each bit resets a CA from 1 to 16
	xxxx xxxx	
PCA1, PCA2, or PCA3		PCA1, PCA2, or PCA3 basic status register
byte 1	1	Input request
	. 1	Output request
	. . 1	DCE interrupt
	. . . 1	Timer interrupt
	. . . . 1 . . .	Exception
	. . . . . 1 . .	Equipment check
	. . . . . 1 .	Enable
	 1	Interrupt request
byte 2		PCA1, 2,or 3 A status register
	1	Overrun

Table 12-10 (Page 6 of 7). BER Type 01 ID 00 Field Details

Field Name	Bit Pattern	Description
	. 1	Underrun
	. . 1	Receive clock running
	. . . 1	SDLC invalid sequence
	. . . . 1 . . .	SDLC flag
	. . . . . 1 . .	Invalid character
	. . . . . 1 .	Break byte detected
	 1	Adapter in sync
byte 3		PCA A control register
	1	Receive mode
	. 1	Transmit mode
	. . 1	Inhibit zero insert
	. . . x x . . .	Mode select
	. . . . . xx .	Code length
	 1	NRZI/break
byte 4		PCA M status register
	1	Data set ready
	. 1	Clear to send
	. . 1	Receive line signal det
	. . . 1	Ring indicator
	. . . . 1 . . .	Data set ready transit
	. . . . . 0 . .	Unused (must be zero)
	. . . . . 1 .	RLSD transition
	 1	Clear to send transition
byte 5		PCA M control register
	1	Data terminal ready
	. 1	Request to send
	. . 1	Wrap
	. . . 1	Test
	. . . . 1 . . .	Select stand by
	. . . . . 1 . .	Select half-speed
	. . . . . 1 .	New sync
	 1	DCE interrupt disable
DFA (Byte 1)		DFA basic status register
	xx	Attachment status: • 0 0 = idle • 0 1 = busy attn loaded • 1 0 = busy reset • 1 1 = busy CHIO
	. . 1	UC bus parity check
	. . . 1	Invalid PIO command
	. . . . 1 . . .	CHIO halt
	. . . . . 1 . .	Equipment check
	. . . . . 1 .	Enable
	 1	Interrupt request
DFA (byte 2)		DFA attention register
	1	Command control block
	. 1	Command specification
	. . 1	Sense summary block
	. . . 1	Data request bit
	. . . . 1 . . .	Drive select high bit
	. . . . . 1 . .	Drive select low bit
	 00	Unused (must be zero)
DFA (byte 3)		DFA interrupt status register
	1	Termination error
	. 1	Invalid command
	. . 1	Command reject
	. . . 1	Parity error
	. . . . 1 . . .	Drive select high bit
	. . . . . 1 . .	Drive select low bit
	. . . . . 1 .	ERP invoked
	 1	Equipment check
TOD		TOD status register
	0000 0 . . .	Unused (must be zero)

Table 12-10 (Page 7 of 7). BER Type 01 ID 00 Field Details

Field Name	Bit Pattern	Description
	. . . . . 1 . .	Equipment check
	. . . . . 1 .	Enable
	 1	Interrupt request
SNAP		Snapshot dump (abend)
byte 1	000x xxxx	Length of snapshot
bytes 2-27	xxxx xxxx	Dump
MLA byte 1-2		Status flag used by the retry process
MLA byte 3	0000 0001	Retry OK
	0000 0010	No retryable. Force reopen line connection
	0000 0011	Hardware failure MLA register
MLA byte 4	100x xxxx	Unimplemented storage violation
	010x xxxx	Read only violation
	001x xxxx	Parity error
MLA bytes 5-6		Previous MOSS check

MOSS BER Type 01 - ID 01

Format foM1: see page 12-128. The MOSS microcode level 1 generates the following BER:

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:01
LVL1 < error description line >                  <REFER.CODE IN CHAR.> CCCCCCCC
 WHO-WHAT:bbbbbbbb  -CHECK:hh  -ABEND:hh
 MCCUA  REGS:hhhh  hhhh  hhhh  hhhh  hhhh  hhhh   CMSA:bbbbbbbb
 X75:hhhhhh  X76:hhhhhh  LSR:hhhhhh  CP-ABEND:hhhh  TA:hhhh  STATUS:bbbbbbbb
 MCCUB  REGS:hhhh  hhhh  hhhh  hhhh  hhhh  hhhh   CMSA:bbbbbbbb
 X75:hhhhhh  X76:hhhhhh  LSR:hhhhhh  CP-ABEND:hhhh  TA:hhhh  STATUS:bbbbbbbb
 MCAD   REGS:hh hh hh hh hh hhhh hh hhhh hhhh
 CCU:hh IOC:hh  NUM:hh

 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Note: All values except the fields 'WHO' and 'WHAT' are in hexadecimal notation (X'0' to X'F').

MOSS BER Type 01 ID 01 - Field Description

Table 12-11. MOSS BER Type 01 ID 01 Field Description

Field Name	Meaning	Refer to
WHO	In binary (first part of error explanation)	page 12-59
WHAT	In binary (second part of error explanation)	page 12-59
ABEND	Level 1 Abend Code • 4E: Permanent HLIR • 4F: Too many spurious errors • FF: No abend code	
CMSA	CCU-to-MOSS status register A (X'11')	page 8-30
CHECK	Error	page 12-59
STATUS	Level 1 status	page 12-59
X75	X'75' - AIO CSCW byte X, byte 0, byte 1 (only used with ERROR code 07, program request IPL)	page 2-28
X76	X'76' - IOC level 1 interrupt request (only used with ERROR code 07, program request IPL)	page 2-28
TA		page 5-37 and 5-30
LSR	Local store register	page 2-25
MCCUA/B	MOSS to CCU A or B registers	page 12-53
MCAD	MOSS to CA registers	page 12-54
CCU	CCU selected for CA • hh = 01: CCUA • hh = 02: CCUB	
IOC	IOC selected for CA • hh = 01: IOC1 • hh = 02: IOC2	
NUM	CA number	

MOSS BER Type 01 ID 01 - Field Details

Some of the following fields may not appear on the BER detail display, but they are part of the BER and they are listed as they appear in the BER file.
See the section 'BER Formats on Disk' page 12-128

Table 12-12. MOSS BER Type 01 ID 01 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
WHO		Gives the origin of the error
	0000	Unresolved
	0001	CCU A
	0010	CCU B
	0011	CA 1 to 8
	0100	CA 9 to 16
	0101	Timer
	0110	MCAD
	0111	Unused
	1000	CCU A power OFF
	1001	CCU B power OFF
WHAT		Gives the type of error
	0000	Unused
	0001	Under DIAGS
	0010	CCU hardcheck
	0011	Program IPL request
	0100	Host IPL request
	0101	Multiple IPL request
	0110	I/O error Alert
	0111	CCU stop
	1000	IOC operation error
	1001	Address exception
	1010	Operation check
	1011	CA MIOH error
	1100	Timer interrupt
	1101	Unresolved
	1110	CCU power OFF
	1111	ESCA IPL request
Check	00	No error on Lvl 1
	01	MOSS OK
	02	Adapter OK
	03	No error during CHIO
	04	Unable to reset HLIR
	05	CCU not IPLed
	06	IPL already in progress
	07	Unable to read CCU information
	08	Unable to read adapter registers
	09	Unable to read CCU registers
	0A	Multiple bit in CMSA
	0B	No bit in CMSA
	0C	CAC not running
	0D	Unexpected interrupt
	0E	Unresolved interrupt
	0F	No interrupt in AMAC card
	10	No interrupt in IORV
	11	No action for MOSS level 1
Status	20	CCUA/B X'76'
	40	CCUA/B CMSA
	80	MCCUA/B status Register 1

Note: For the list of suspected FRUs, refer to the MIP.

MOSS BER Type 01 ID 02

Format foM2: see page 12-129. The MOSS microcode generates the following BERs when an error occurs during CCU/MOSS exchanges.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:02
MIOC < error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
 MOSS-CHECK:hh  ADNO:hh  CMD:hh  PIRV:hh  IOIRV:hh  CMSB:hh  STAC:hh
 CAC-RC:hh  STAT1:hhhh   STAT4:hhhh  ADDR:hhhhhhhh
 PCW:hhhhhhhh hhhhhhhh hhhhhhhh  FLAGS:hh  CA:hh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS  F8:NEXT
```

MOSS BER Type 01 ID 02 With MOSS Check 04

Format foM2b: see page 12-129. The MOSS microcode generates the following BER for a MIOC invalid mail box on level 4 process.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:02
MIOC < error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
 MOSS-CHECK:04  CMD:hh
 NCP MB REQUEST:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
 NCP MB RESPONSE:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS  F8:NEXT
```

MOSS BER Type 01 ID 02 - Field Description

Table 12-13 (Page 1 of 2). MOSS BER Type 01 ID 02 Field Description

Field Name	Meaning	Refer to
CMD	Logical command (used in the error description line)	page 12-62
MOSS-CHECK	MOSS-CHECK error code (used in the error description line)	page 12-62
CA	Channel adapter number (1 to 16)	
ADNO	• CA adpapter number, or • Adapter CCU number (05 for CCUA, 06 for CCUB) or • Switch CCU adapter on IOC1 (40). See page 3-22 • Switch CCU adapter on IOC2 (C0). See page 3-22	
PIRV	Programmed interrupt request vector	page 12-51
IOIRV	I/O interrupt request vector	page 12-51
CMSB	CCU-to-MOSS status register B (X'06')	page 8-31
CAC-RC	CAC return code or error code	page 12-62
STAT1	MAC status reg 1	page 8-16
STAT4	MAC status reg 2	page 8-16
ADDR	PCW list address.	
FLAGS	Adapter control block flags	page 12-63
STAC	CCU to MOSS C register	page 8-31
PCW	Program control word. Command sent by the CCU.	For PE only
NCP MB REQUEST	NCP mailbox request	

Table 12-13 (Page 2 of 2). MOSS BER Type 01 ID 02 Field Description		
Field Name	**Meaning**	**Refer to**
NCP MB RESPONSE	NCP mailbox response	

MOSS BER Type 01 ID 02 - Field Details

Some of the following fields may not appear on the BER detail display, but they are part of the BER and they are listed as they appear in the BER file.
See the section 'BER Formats on Disk' page 12-128

Table 12-14 (Page 1 of 2). MOSS BER Type 01 ID 02 Field Details

Field Name	Bit pattern or Hex value	Meaning
CMD		Logical command
	01	Read B register error impossible
	02	MIOC request
	04	Interrupt level 4 processing
	08	Display registers
	20	Control program buffer reading
	21	Control program buffer writing
	40	Out mailbox request
	41	Out mailbox response
	80	In mailbox request
	81	In mailbox response
	90	CHIO command
MOSS-CHECK		MOSS-CHECK Error codes
	01	LSSD string select error
	02	Invalid PCW request
	04	Invalid out-mailbox request
	08	In-mailbox time out response
	10	Unexpected in-mailbox response from CP
	20	Unresolved interrupt
	21	C-clock stop
	22	Invalid interrupt level 4
	40	CCU busy bit ON
	41	Devices busy bit ON
	42	CCU power down
	80	Physical error reported
	86	CHIO assynchronous error
	87	CHIO synchronous error
	88	CHIO time out
CAC-RC		CAC return code or error code
	00	Return code OK
	01	Adapter down
	02	LSSD string ID error
	03	LSSD residual count
	04	CCU busy bit ON
	05	Device busy bit ON
	06	IOC error
	07	Op check
	08	Exception
	09	Scanner error 1
	0A	CHIO abort
	0B	Unexpected interrupt
	0C	I/O interrupt canot be reset
	20	CA to MOSS level 1
	40	Abend request
	80	CCU power down
	81	Invalid PCW
	FF	Abort

Table 12-14 (Page 2 of 2). MOSS BER Type 01 ID 02 Field Details		
Field Name	**Bit pattern or Hex value**	**Meaning**
FLAGS		Adapter control block flags
	80	
	40	Adapter down
	20	Adapter checkpoint retry
	10	Adapter Xparent retry thresh.
	08	Time out on adapter
	04	Mail box in request
	02	Timer set for mail box in
	01	Moss Off line Cmd in mail box
	81	Moss On line Cmd in mail box
	82	CHIO opereation in process
	83	Timer set for CHIO ope
		CHIO retry has been done

MOSS BER Type 01 - ID 03

Format foM3: see page 12-129. The MOSS microcode generates the following BERs when an error occurs in the disk/diskette drive or disk drive adapter.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:03
< error description line >                    <REFER.CODE IN CHAR.> CCCCCCCC
MOSS-CHECK:hh DEV:hh FILE:hhhhhhhh  CMD:hh  REQ:hh
F:hh  CNT:hh  ARC:hh  BSTAT:hhhh  ADDR:hhhhhhhh
BCLE:hhhhhhhh hhhhhhhh  SSB:hhhhhhhh hhhhhhhh hhhhhhhh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 03 - Field Description

Table 12-15. MOSS BER Type 01 ID 03 Field Description		
Field Name	**Meaning**	**Refer to**
CMD	Logical command	page 12-64
MOSS-CHECK	MOSS-CHECK error codes	page 12-64
DEV	Device in error	page 12-64
REQ	Function request code	page 12-64
ARC	Adapter return code	page 12-66
BSTAT	Basic status register	page 12-68
F	Flag indicator, last BCLE executed (internal to MOSS)	page 12-64
CNT	BCLE-related byte count	
ADDR	Last BCLE-related address	
BCLE	Last executed buffer control list element (CAC-related information)	page 12-64
SSB	Sense summary block adapter status	page 12-65
FILE	File name or load module (in EBCDIC)	

MOSS BER Type 01 ID 03 - Field Details

Some of the following fields may not appear on the BER detail display, but they are part of the BER and they are listed as they appear in the BER file.
See the section 'BER Formats on Disk' page 12-128

Table 12-16 (Page 1 of 2). MOSS BER Type 01 ID 03 Field Details

Field Name	Bit pattern or Hex value	Meaning
MOSS CHECK		
	01	Bad track but no alternate track assigned.
	02	Alternate track successful assigned.
	03	Alternate track assignment failure.
	04	Disk or diskette down
CMD		Logical command
	00	Open
	01	Write
	02	Read
	03	Close
	04	Load
	05	Direct execute
DEV		
	01	Adapter failure for disk operations
	02	Adapter failure for diskette operations
	03	Disk drive
	04	Diskette drive
	05	Adapter or disk drive
	06	Adapter or diskette drive
	07	Diskette media (floppy disk)
REQ		Function request code
	00	Execute
	05	Read operational statistics
	07	No-op
	25	Read SCA state
	83	Open adapter
	A3	Open SCA
	AB	Close SCA
	EB	Terminate (adapter)
F (flag)		CAC error record
	1	Error code indicator
	. . 1	Last record indicator
BCLE byte 0	hh	Flag: hh = 00: No command chaining hh = 01: Command chaining
BCLE byte 1	hh	Command field
BCLE bytes 2-3	hh	Count field
BCLE bytes 4-7	hh	Data address

Table 12-16 (Page 2 of 2). MOSS BER Type 01 ID 03 Field Details

Field Name	Bit pattern or Hex value	Meaning
SSB byte 0		Drive status
	1	Drive ready
	. 1	Seek end (HDD only)
	. . 1	Write protected (FDD only)
	. . . 1	Write fault (HDD only)
	. . . . 1 . . .	Disk change
	. . . . . x x .	Unused
	 1	Track 0
SSB byte 1		SSB error status byte 0
	x	CRC/ECC error x = 0: Data x = 1: ID
	. 1	CRC/ECC error
	. . 1	Address mark not found
	. . . 1	Bad track
	. . . . 1 . . .	Wrong cylinder
	. . . . . 1 . .	Control address mark
	. . . . . 1 .	Format error
	 1	ID not found
SSB byte 2		SSB error status byte 1
	x	Unused
	. 1	Data adapter error
	. . 1	Retry corrected
	. . . 1	Defective sector
	 xxxx	Unused
SSB bytes 3-6		Last data adapter ID field processed
SSB bytes 7-8		Cylinder and head location
SSB byte 9		Number of sectors corrected by ECC
SSB byte 10		Number of retries
SSB byte 11		Processor state at reset time

Notes:

1. All values are in hexadecimal notation (X'0' to X'F'), except for the file name or module name (FILE), which is in EBCDIC.
2. The CAC will make several retries (up to 10). The retry count contains the number of retries before the disk operation was successfully terminated.
   - If RCNT is lower than 10, the last I/O operation was successful. The error was intermittent.
   - If RCNT = 10, the decision (recovery or program action) is taken by the MOSS application that activated the diskette operation. The error is permanent (solid).

Adapter Return Codes (ARC)

The error description line is built from the contents of the ARC.

Table 12-17. MOSS BER Type 01 ID 03 Adapter Return Codes

Field Name	Hex Value	Meaning
ARC		EXCEPTION/SUCCESS CLASS
	22	SCA ready (exception)
	23	SCA not ready (exception)
	30	SCA not ready (no error)
	31	Control record found
ARC		ERROR / NOT SUCCESSFUL CLASS
		SEQUENCE ERRORS
	01	Adapter busy-attention
	02	FRB busy.
	05	Adapter busy-CHIO
	06	Adapter busy-reset
	08	SCA 1 not open
	09	SCA 2 not open
	0A	Adapter not open
	0D	SCA 1 already open
	0E	SCA 2 already open
		PARAMETER PROBLEMS
	11	FRB program check
	12	BCL program check
	13	Invalid PIO command
		HARDWARE AND EQUIPMENT CHECKS
	20	Undetermined equipment check (hardware error in adapter)
	28	Seek check
		DATA TRANSMISSION PROBLEMS
	30	Termination error with no specific error
	32	Sect buffer parity error
	34	Cylinder overrun
	37	HALT during a CHIO operation
	38	I/O bus parity error
	39	CCB with no active CSB
	3A	Invalid command in CCB or SSB
	3B	ERP invoked by thresher
	3C	Internal parity error
	3E	Record not found
		PREEMPTIVE REQUEST CLASS
	0B	Preemptive request complete
	0C	Preemptive request rejected
		L/OPERATOR INTERVENTION REQUIRED
	62	SCA not ready (error)
	6F	Invalid diskette format
		I/O MACHINE CHECK
	76	PIO MCK (non-recursive)
	F6	PIO MCK (recursive)

MOSS BER Type 01 ID 04

Format foM4: see page 12-129. The MOSS microcode generates the following BER when an error occurs on the console or its adapter cards:

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:04
DPLY< error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
 MOSS-CHECK:hh  CMD:hh  BSTAT:hh  ASTAT:hh  CSTAT:hhhh  MSTAT:hh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 04 - Field Description

Table 12-18. MOSS BER Type 01 ID 04 Field Description

Field Name	Meaning	Refer to
ASTAT	Adapter error status register	page 12-67
BSTAT	CCA card basic status register	page 12-68
CMD	Logical command	page 12-68
CSTAT	Console status	page 12-68
MOSS-CHECK	Error code	page 12-68
MSTAT	Modem status register	page 12-69

Note: All values are in hexadecimal notation (X'0' to X'F').

MOSS BER Type 01 ID 04 - Field Details

Some of the following fields may not appear on the BER detail display, but they are part of the BER and they are listed as they appear in the BER file. See the section 'BER Formats on Disk' page 12-128

Table 12-19 (Page 1 of 3). MOSS BER Type 01 ID 04 Field Details

Field Name	Bit Number or Hex Value	Meaning
ASTAT		MOSS-CHECK = X'0A' Adapter exception status
	x	Read/open halted
	. x	XMIT/RCV contention occurred
	. . x	BREAK character received
	. . . x xxxx	Unused
ASTAT		MOSS-CHECK = X'0C' or '8C'
	x	Parity error on receive data
	. x	DCE error
	. . x	RCV line at space
	. . . x	RCV data buffer too short (overflow)
	. . . . x . . .	Unused
	. . . . . x . .	Machine check error
	. . . . . . x .	RCV text time out
	 x	Lost data (overrun)

Table 12-19 (Page 2 of 3). MOSS BER Type 01 ID 04 Field Details

Field Name	Bit Number or Hex Value	Meaning
ASTAT		MOSS-CHECK = X'8A' Adapter exception status
	x	Parity error on received data
	. x	DCE error
	. . x	RCV line at space
	. . . x	RCV data line too short
	. . . . x . . .	Unused
	. . . . . x . .	Machine check error
	. . . . . . x .	RCV text time out
	 x	Data lost (overrun)
BSTAT		CCA Basic status register bit assignment
	01	Adapter interrupt pending
	02	Adapter enabled
	04	MCPC interrupt
	08	Exception interrupt
	10	Timer interrupt
	20	Modem interrupt
	40	CSR - output request
	80	CSR - input request
CMD		Logical commands
	08	Lock keyboard
	10	Close adapter
	20	Read/write adapter
	40	Write adapter
	80	Open CCA adapter
	81	Open console
CSTAT		Console status ERROR: X'40','C0'
	Bits	
	0-0	Parity bit
	0-1	Not bit 2
	0-2	Communication buffer overrun
	0-3	Line parity error detected
	0-4	Command error detected
	0-5	Unused
	0-6	Keyboard locked
	0-7	Unused
	1-0	Parity bit
	1-1	Not bit 2
	1-2	Block mode
	1-3	Half-duplex mode
	1-4	Unused
	1-5	Unused
	1-6	Program mode
	1-7	Unused
MOSS-CHECK codes	0A	CAC detected exception (local) ASTAT = adapter exception
	0C	CAC detected error (local) ASTAT = adapter error
	40	Console error (local)
	40	Console error (remote)
	8A	CAC detected exception ASTAT = adapter exception status (remote)
	8C	CAC detected error (remote) ASTAT = adapter error

Table 12-19 (Page 3 of 3). MOSS BER Type 01 ID 04 Field Details

Field Name	Bit Number or Hex Value	Meaning
MSTAT		CCA modem status register bit assignment
	01	CTS transition
	02	RLSD transitions
	04	Reserved
	08	DSR transition
	10	Ring indicator
	20	Received line signal detector (RLSD)
	40	Clear to send (CTS)
	80	Data set ready (DSR)

Note: The correct console status is X'4030'.

MOSS BER Type 01 ID 05

Format foM5: see page 12-129. The MOSS microcode generates the following BERs when an error occurs on a scanner or on the MOSS/scanner connections.

```
                                  ELD DETAIL
    < error description line >                 <REFER.CODE IN CHAR.> CCCCCCCC
SEL#:hhhh   FLAG:xx  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:05
< Error description line>
<MOSS-CHECK:xx ADDR:hh>=Unexpected interrupt received
<MOSS-CHECK:xx ADDR:hh CSCHK:hhhh>
<MOSS-CHECK:xx ADDR:hh MBST:hhhh>
<MOSS-CHECK:xx ADDR:hh TD:hhhh>
<MOSS-CHECK:xx ADDR:hh DUMP:hh hh
 hhhh hhhh hhhh hhhhhhhh hhhh
 hhhh hhhh hhhh hhhhhhhh hhhh>

 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Table 12-20. MOSS BER Type 01 ID 05 MOSS-CHECK Details

MOSS Check	Meaning
01	Scanner failure during IPL
02	Mailbox contains the error status
04	Unexpected interrupt received
05	Scanner is inoperative
09	Scanner checkout failure
0A	Scanner mailbox error status
0B	Scanner time out
18	Scanner IML complete
F0	Scanner dump and IML
F1	Scanner IML and dump full
F2	Scanner IML and disk error on dump
F3	Scanner IML and MAC error on dump
F4	Scanner dump or reinitialization failure
F5	Scanner dump and IML/CP time out on connection
F6	Scanner dump and IML/MAC error connection
F7	Scanner dump and IML/connection maibox reject
F8	Scanner IML failure and dump full
F9	Scanner IML failure and disk error on dump
FA	Scanner IML failure and MAC error on dump
FB	Scanner down
FC	Scanner down

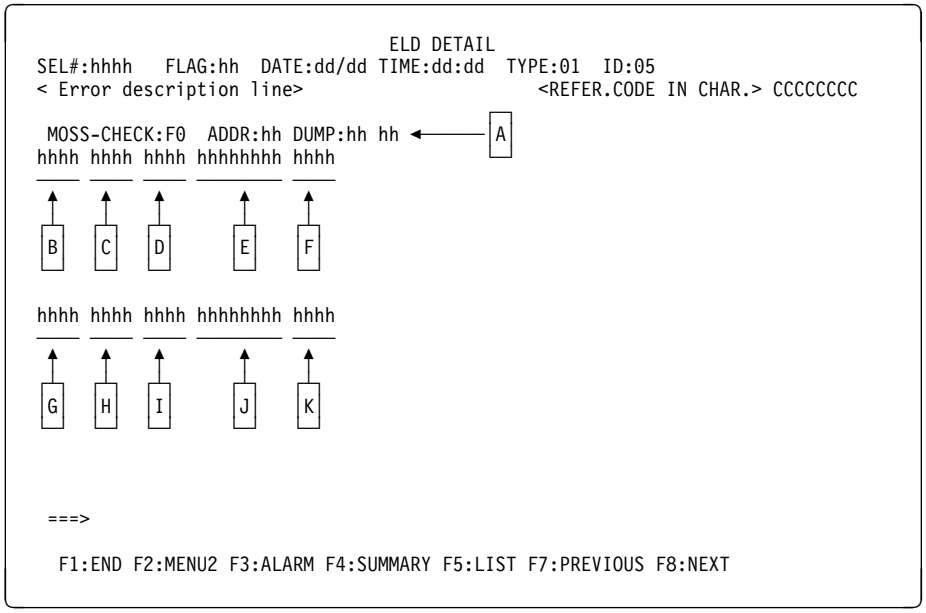
MOSS BER Type 01 ID 05: Format foM5, see page 12-129. The MOSS microcode generates the following BER when an error occurs on MOSS or during IOH operations.

```
                                ELD DETAIL
    < error description line >                 <REFER.CODE IN CHAR.> CCCCCCCC
SEL#:hhhh   FLAG:xx  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:05
<MOSS-CHECK:hh ADDR:hh X76:hhhhhh STATUS:hhhh>


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Table 12-21. MOSS BER Type 01 ID 05 MOSS-CHECK Details

MOSS Check	Detected by LVL	Meaning	Status
08	1	Get error status IOH	Type 1, 2, or 3
10	4	NO information	No status available
20	4	Mailbox status in BER	Command completion
40	4	Get error status IOH	Type 1, 2, or 3
80	1		No status available

MOSS BER Type 01 ID 05: Format foM5a, see page 12-130.



The field indicated by the letter **A** contains:

- The **DUMP error code** in the first byte
- The **IML error code** in the second byte, as follows:

Table 12-22. 'A' Field Details

Field Name	Value	Meaning
Dump error code	00	Dump available
	01	Dump not taken (dump file already full)
	02	Dump not available (diskette error)
	03	Dump not available (hardware error MIOC/TSS)
	FF	Dump not taken
IML error code	01	Re-IML not successful
	02	Connect not successful, CP not answering (re-IML OK)
	03	Connect not successful (MIOC operation failed)
	04	Connect not successful, rejected by CP
	05	Threshold (no dump and no re-IML)
	10	Re-IML successful
	FF	Re-IML successful

Note: All other combinations of byte values for the DUMP field are not valid

The other fields indicated by the letters **B** to **K** have the following meaning:

Table 12-23. 'B' to 'K' Field Details

Field ID	Meaning
B	Last in TA for dump
C	Last out TA for dump
D	Last TD for dump
E	Last MB for dump. This field contains the first four bytes
F	Last disk ECB for dump
G	Last in TA for re-IML
H	Last out TA for re-IML
I	Last TD for re-IML
J	Last MB for re-IML.This field contains the first four bytes
K	Last disk ECB for re-IML

Note: Invalid fields contain all 'F's.

MOSS BER Type 01 ID 05 - Field Description

Table 12-24. MOSS BER Type 01 ID 05 Field Description

Field Name	Meaning	Refer to
ADDR	Scanner address as shown in "Scanner Addressing" (Hex)	MIP chapter 4
X76	X'76' (bytes X, 0, and 1 of field X76 on screen) or MOSS command completion (bytes 0 and 1; X not used)	page 2-28 and page 4-202
STATUS	Error status or mailbox status depending on the error code	page 12-71
TD	Last command (DB0 and DB1 at TD time)	Chapter 8
MBST	Mailbox status	Chapter 8
CSCHK	Scanner status	page 6-15 (HPTSS) page 4-120 (TSS)
ADAPTER ID	IOC bus ID	-

Notes:

1. All values are in hexadecimal notation (X'0' to X'F').
2. For details of scanner/MOSS communication, see Chapter 8.

MOSS BER Type 01 ID 06 (Error 01 or 02)

BER format foM7: see page 12-130. The MOSS microcode generates the following BER when an error occurs in the BER file outside controller initialization.

The error description line contains information such as the CP abend code, the scanner address, or the number of BERs lost.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:06
APPL< error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
 MOSS-CHECK:hh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Note: For software information on BERs originated by NCP/PEP, refer to the associated product documentation.

MOSS BER Type 01 ID 06 (Error 03 or 06)

This BER corresponds to one of the following cases:

- IPL check
- IPL after fallback check (standby mode)
- IPL after switchback check
- IPL complete + errors
- IPL after fallback complete + errors (standby mode)
- IPL after switchback complete + errors.

For 'IPL complete with errors' the BER is always 'normal' (in opposition to 'composite BERs').

For 'IPL check', 'fallback in standby mode check', and 'switchback check' the BER logged will be a 'composite BER' for physical errors and a normal one for logical errors.

BER format foM6: see page 12-130, IPL error.

```
                                ELD DETAIL
 SEL#:hhhh   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:06
 APPL< error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
  MOSS-CHECK:hh CCU:hh  REQ:hh  LVL1-REQ:hh  F2:hhhh  X71:hhhhhh  X72:hhhhhh  F1:hh
  MIS:hh hh hh hh hh hh hh hh hh hh hh hh hh hh hh hh hh hh hh hh hh hh hh hh hh hh
  LA:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
     hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
     hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
     hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
  CA:hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh
  hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh
  hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh
  3746-900:hhhh


  ===>

:  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 06 (Error 04)

BER format foM7a: see page 12-130. The MOSS microcode generates the following BER when an error occurs on scanner IML check at the end of IPL.

```
                                ELD DETAIL
 SEL#:hhhh   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:06
 APPL< error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
  MOSS-CHECK:hh



  ===>

   F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Note: For software information on BERs originated by NCP/PEP, refer to the associated product documentation.

MOSS BER Type 01 ID 06 - Field Details

Some of the following fields may not appear on the BER detail display, but they are part of the BER and they are listed as they appear in the BER file.
See the section 'BER Formats on Disk' page 12-128

According to the ERROR type, the MIS field contents differs:

Error 03 MIS is made from the fields DISK, DISK2, IPL mode and IPLCHECK of the next table.

Error 06 As described in the field MIS (page 12-79) of the following table.

Table 12-25 (Page 1 of 6). MOSS BER Type 01 ID 06 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
MOSS-CHECK		MOSS error code
	03	Complete with errors
	05	NCP re-IPL succesful after CCU hard check or NCP abend
	06	Check
	08 Ext 05	CCU hard check
	08 Ext 07	NCP abend
	09	CLDP abend
	10	Fallback check
	11	Switchback check
	12	Fallback/switchback request to network operator
	13	Timed IPL will occur soon
	14	Timed IPL is cancelled
	18	LSSD string first part
	28	LSSD string second part
IPL info		Complementary information to MOSS-CHECK
	01	IPL
	02	IPL after fallback
	03	IPL after switchback
CCU		CCU identification
	01	CCU A
	02	CCU B
REQ	01	IPL on power-On reset
	02	CCU + scanners IPL req from keyboard
	03	IPL requesting IPL of other CCU
	04	IPL requesting fallback
	05	Fallback requesting IPL
	06	Switchback requesting IPL
	07	IPL is requested by the level 1
	08	Scheduled or network power-On reset
	09	IPL after fallback
	0A	Normal fallback requested
	0B	IPL of standby CCU requested
	0C	Timed IPL requested by MSD
LVL1-REQ		ID of CCU IPL request
	02	CCU hardcheck
	03	Program request IPL
	04	Channel request IPL
	07	CCU power drop

Table 12-25 (Page 2 of 6). MOSS BER Type 01 ID 06 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
STATUS		System status
	00	MOSS only
	01	MOSS disconnected
	10	System running
	. . x	MOSS has reached the MOSS init part 2, then normal MCPC must be used
	. . . x	Unused
	. . . . x . . .	Scanner not IMLed, alert sent by loop detection task
	. . . . . 10 .	IPL drive: hard disk
	. . . . . 00 .	" " : diskette
	 x	When ON, no local console available
Abend code	xxxx xxxx xxxx xxxx	IPL abend code
LA byte 1		32 blocks (1 per CSP) of 4 bytes, displayed as 8 hexadecimal characters
	x	LPTSS found present in CDF
	. x	TRA found present in the CDF
	. . x	Adapter power ON
	. . . x	Scanner/TRA is presently the scanner selected
	. . . . x . . .	TIC1 found present in CDF
	. . . . . x . .	TIC2 found present in CDF
	. . . . . x .	LA under control of the CP
	 x	Scanner successfully IMLed
LA byte 2	x	Automatic re-IML has failed, or scanner went down twice in the minimum time range, or CSP could not be IMLed at general IPL.
	. x	CMD engaged with scanner failed with a LVL1 interrupt on MOSS: Interrupt handler failed in trying a get error status register
	. . x	Scanner successfully IMLed, no action (stop, go, connect, disconnect, reset) performed and no scanner error detected: scanner is initialized
	. . . x	Scanner failure during fallback
	. . . . x . . .	Scanner failure during fallback on MOSS area High/low commands
	. . . . . x . .	Scanner failure during fallback on IML command
	. . . . . x .	Scanner failure during fallback on INIT command
	 x	HPTSS/ESS found present in the CDF
LA byte 3		
	x	Unused
	. xxx	LA type: xxx = 001: TSS xxx = 010: HPTSS xxx = 011: TRSS xxx = 110: ESS
	 xxxx	Target CCU for curent scanner: xxxx = 0001: CCU A xxxx = 0010: CCU B

Table 12-25 (Page 3 of 6). MOSS BER Type 01 ID 06 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
LA byte 4	01	Mismatch between CDF and data returned from the scanner (MUX presence and EXTEND bit)
	02	Bad IOC bus test
	03	Error during loading of CSP load module
	04	Bad CSP checkout result
	05	Time out during IOH on CSP
	06	Bad block transfer between CCU and CSP
	07	Bad CSP initialization
	08	Bad return from CHGCDLA access function
	09	Bad selective POR
	0A	Invalid position on power block returned by CDF
	0B	Scanner responsible of time out at IOC bus test
	0C	Scanner with the same power source as one with bad UC bus test return
	0D	Scanner which can not be powered ON
	0E	Scanner not accessible in CDS
	0F	MOSS area high/low problem during fallback
	10	IML count 1 problem during fallback
	11	Init problem during fallback
	12	Scanner already down before fallback
	13	Scanner not powered UP at fallback start
	14	Outstanding dump request when fallback
	15	Scanner not powered UP at IPL start
DISK	See DISK bytes 1-2 for details	5 halfwords: • 1: OPEN • 2: READ • 3: LOAD • 4: WRITE • 5: CLOSE
DISK byte 1	x	Unused
	. x	Full instruction test load module
	. . x	IOC bus tests load module
	. . . x	CLDP load module
	. . . . x . . .	Scanner load module
	. . . . . x . .	Scanner load module member 1
	. . . . . . x .	Scanner load module member 2
	 x	Scanner load module member 3
DISK byte 2	x	HPTSS/ESS load module
	. x	HPTSS/ESS load module member 1
	. . x	HPTSS/ESS load module member 2
	. . . x	HPTSS/ESS load module member 3
	. . . . x . . .	SALT load module
	. . . . . x . .	Stand alone utilities
	. . . . . . x .	Port swap file
	 x	Unused
DISK2		5 bytes, same allocation as 'halfwords' above
	x	Roll in/out file
	. x	LSR file
	. . x	CCU dump file
	. . . x	First dump record file
	. . . . x . . .	Last dump record file
	. . . . . x . .	Control program load module file
	 xx	Unused

Table 12-25 (Page 4 of 6). MOSS BER Type 01 ID 06 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
F2 byte 1	x . . . . x . . . . x . . . . x . . . . x . . . . x . . . . x x	Bad branch trace buffer length Bad check record pool Bad control program interface table LVL 1 on CA during CA monitoring X71 register is not readable CLDP did a pseudo abend Loading scanner table failed (ph3) Control info length error: MB error
F2 byte 2	x . . . . x . . . . x . . . . x . . . . x . . . . x . . . . x x	IPL from disk length error: MB error IPL complete with port swap errors LSSD dump incorrect Adapter dump requested, not performed (bad return from CHGCDLA access function) Error during save on disk Error during load from disk Error during dump on disk (phase 4) Error during roll-in roll-out of top 64 K of storage to/from HDD
X71		X71 register, see page 2-32
X72		X72 register, see page 2-32
IPL mode	x . . . . x . . . . 1 . . . . 1 . . . . x . . . . 1 . . . . 1 1	IPL Mode (IPLMODE) x = 0 <==> Operator x = 1 <==> Automatic Customer / Maintenance (MTMENU) x = 0 <==> Customer x = 1 <==> Maintenance Force switching authorization has been used by IPL application A forced reset of the switch has been performed with the disconnect latch set ON Standalone dump status x = 0 Not requested or failed x = 1 Successfully performed Previous fallback completed with error Previous switchback completed with error Previous fallback was automatic
CCU	 01 02 01 02 01 02 03	Configuration Single configuration Twin configuration Default CCU: CCU A is the default CCU CCU B is the default CCU 3745 mode: Standby mode Dual mode Backup mode
MIS		Miscellaneous. Following byte description is only for **error 06** (IPL check). For **error 03** MIS is made from the fields DISK, DISK2, IPL mode and IPLCHECK of this table.
Bytes 1		BER error code initialized at IPL
Bytes 2		IPL fallback or switchback

Table 12-25 (Page 5 of 6). MOSS BER Type 01 ID 06 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
Byte 3		Valid field indicators
	x	IAR is valid
	. x	SAR is valid
	. . x	LAR is valid
	. . . x	IN70 is valid
	. . . . x . . .	IN76 is valid
	. . . . . x . .	IN7D is valid
	. . . . . . x .	IN7E is valid
	 x	IN7X is valid
Bytes 4-6		IAR
Bytes 7-9		SAR
Bytes 10-12		LAR
Bytes 13-14		INPUT X'70', see page 2-31
Bytes 15-16		INPUT X'76', see page 2-36
Byte 17		IN76 IOC1 STATE LATCH (see page 2-37)
	. . . . x . . .	Time out
	. . . . . x . .	Bus IN parity
	. . . . . . x .	AIO
	 x	PIO
Byte 18		IN76 IOC2 STATE LATCH (see page 2-37)
	. . . . x . . .	Time out
	. . . . . x . .	Bus IN parity
	. . . . . . x .	AIO
	 x	PIO
Bytes 19-20		INPUT X'7D', see page 2-42
Bytes 21-22		INPUT X'7E', see page 2-43
Bytes 23-24		INPUT X'7E' extension, see page 2-43
F1	x	Disk IPL facility failed
	. x	PCA of local console not available
	. . x	PCA of remote console not available
	. . . x	PCA of RSF console not available
	. . . . x . . .	MCAD detected KO by MOSS diags
	. . . . . x . .	SWAD detected KO by MOSS diags
	. . . . . . x .	MCCUA detected KO by MOSS diags
	 x	MCCUB detected KO by MOSS diags
RC from CDF	xxxx xxxx xxxx xxxx	CDF return code from CDF access function
CA byte 1		6 bytes per CA (16 CAs)
	x	MIOH failure
	. x	Bad return from CHGCDCA
	. . x	Power OFF
	. . . x	Verify data error
	. . . . x . . .	Bad checkout result
	. . . . . x . .	Chaining error
	. . . . . . x .	Mismatch about TPS between CDF and HW
	 x	Unused

Table 12-25 (Page 6 of 6). MOSS BER Type 01 ID 06 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
Byte 2	x . . . . x . . . . x . . . . x . . . . x . . . . x xx	Init error Bad return from MCAD adapter CA not found in 'CONNECTED' status during phase 1B/fallback Chaining not performed due to 2 errors on the bus MCAD error when enabling MCAD error when disabling Unused
Bytes 3-4	xxxx xxxx xxxx xxxx	CA checkout result (see page7-39)
Byte 5	 0000 0001 0000 0010	CCU for CA CCU A CCU B
Byte 6		Unused
IPLCHECK Byte 1 Byte 2	 0000 1111 x . . . . x . . . . x . . . . x . . . . x . . . . x . . . . x x	**Error 03 only** (IPL complete with errors) Unexpected IPL option Unexpected CCU option Unexpected/undefined F key No CCU under IPL, IPL started No CCU specified for BER Unknown switch request Unexpected display request Unused
3746-900	 8 h h h 4 h h h 2 h h h 1 h h h	 Bad NCP version for the 3746-900 Coupler ready bit No port swap exchange Port swap error for the 3746-900

MOSS BER Type 01 ID 06 (Error 05/08 Ext 05/07)

BER format foM9a: MOSS-check 08 EXT 05, see page 12-131. The MOSS microcode generates the following BER when a CCU hardcheck occurs. The BER fields contain information fetched from the LSSD strings saved when the error occurs on CCU hardcheck. Then a re-IPL is started.

```
                                ELD DETAIL
 SEL#:hhhh   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:06
 '3745 RE-IPL STARTED FOR CCU HARDCHECK'.      <REFER.CODE IN CHAR.> CCCCCCCC
  MOSS-CHECK:08 EVENT-EXT:05 CCU:hh
  IAR:hhhhhh  LAR:hhhhhh  SAR:hhhhhh
  X70:hhhhhh  X76:hhhhhh  X7D:hhhhhh  X7E:hhhhhh
  HDCK:hhhh


  ===>

   F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

BER format foM9: see page 12-131, MOSS-check: 05 EXT: 05/07. The MOSS microcode generates the following BER when a successful re-IPL after a CCU hardcheck occurs for an Ext 05, and after a CLDP abend for an Ext 07. The BER fields contain information fetched from the LSSD strings and saved when the error occurs on CCU hardcheck. Then a re-IPL is started.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:06
APPL< error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
 MOSS-CHECK:05 CCU:hh  DUMP:hh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 06 (Error 05/08 Ext 05/07) - Field Details

Table 12-26. MOSS BER Type 01 ID 06 (Ext 05/07) Field Details

Field Name	Bit Pattern or Hex Value	Meaning
CCU	05	CCU hardcheck code convention
CCU	 01 02	CCU identification CCU A CCU B
NCP Abend	xxxx xxxx xxxx xxxx	NCP abend code for alert: see page 12-39.
Dump status	 01 02	Stand-alone dump status Not requested or failed Successfully performed
HDCK	Byte 1 xxxx . . . . x . . . . x . . . . x x	Unused Unused Alu compare error X Alu compare error 0 Alu compare error 1 Level 1 error reentry

MOSS BER Type 01 ID 06 (Error 07)

BER format foM10a: see page 12-131.

```
                                ELD DETAIL
APPL< error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
SEL#:hhhh   DATE:dd/dd TIME:dd:dd  TYPE:01  ID:06
MOSS OFFLINE
MOSS-CHECK:hh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS-CHECK: hh = 07: MOSS is offline

MOSS BER Type 01 ID 06 (Error 08 Ext 07)

BER format foM19: see page 12-133. The MOSS microcode generates the following BER on CLDP abend and related re-IPL request.

```
                                  ELD DETAIL
APPL< error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
SEL#:hhhh   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:06

MOSS-CHECK:08 EVENT-EXT:07 CCU:hh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 06 (Error 09)

BER format foM10: see page 12-130. The MOSS microcode generates the following BER when CLDP abends (code X'F1B'). This BER does not follow the 'composite BER' mechanism. The X72 field contains the CLDP abend code (see Chapter 11 for CLDP abend code meanings).

```
                                  ELD DETAIL
SEL#:hhh FLAG:hh  DATE:hh/hh TIME:hh:hh  TYPE:01  ID:06
APPL< error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
 MOSS-CHECK:09 EVENT-EXT:hh CCU:hh  IAR:hhhhhh  X71:hhhhhh  X72:hhhhhh
 WKR1:hhhhhh  WKR2:hhhhhh  WKR3:hhhhhh  WKR4:hhhhhh  WKR5:hhhhhh  WKR6:hhhhhh
 WKR7:hhhhhh
 X7E:hhhh  X7D:hhhh  X76:hhhh
 CA: XE:hhhh  XD:hhhh  X50:hhhh  X51:hhhh  X52:hhhh  X60:hhhh
 LA:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
    hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER 01 ID 06 (Error 09) - Field Description

Table 12-27. MOSS BER Type 01 ID 06 (Error 09) Field Description

Field Name	Meaning	Refer to
X76	Contents of register INPUT X'76'	page 2-31
X7D	Contents of register INPUT X'7D'	page 2-31
X7E	Contents of register INPUT X'7E'	page 2-31
WKR1-7	Work registers, contents depend on type of CLDP abend	PE only
LA	LA error status	page 4-200
X50	Adapter bus control module check	page 7-40
X51/X52	Channel A/B control module check	page 7-40
XE	CA level 1 interrupt request	page 7-28
XD	CA check register	page 7-27
X60	Initiale selection control. See CA reg. X00.	page 7-20

Note: The registers are described in Chapter 2 of this manual.

MOSS BER Type 01 ID 06 (Err 09) - Field Details

Some of the following fields may not appear on the BER detail display, but they are part of the BER and they are listed as they appear in the BER file. See the section 'BER Formats on Disk' page 12-128

Table 12-28. MOSS BER Type 01 ID 06 (Err 09) Field Details

Field Name	Bit Pattern or Hex Value	Meaning
X71 bytes 0-1	xxxx xxxx xxxx xxxx	CA or Link address according to IOC bus format
X71 byte x	xx . . . . x . . . . x . . . . x . . . . x . . . . x x	Unused CLDP abend RPO detected Load Dump CA IPL Link IPL
X72		Contains the CLDP codes. For details, see the CLDP table in Chapter 11

MOSS BER Type 01 ID 06 (Error 10/11)

BER format foM13: see page 12-132, fallback/switchback check.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:hh
APPL < error description line >                 <REFER.CODE IN CHAR.> CCCCCCCC
MOSS-CHECK:10 MODE:hh  DEFAULT:hh  TO:hh  STATUS:bbbbbbbb MB:hhhhhh
SWITCH:hhhhhh LA:hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh
                 hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh
                 hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh
                 hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh
CA:hhhh hhhhhhh hhhh hhhhhhhh hhhh hhhhhhhh hhhh hhhhhhhh
   hhhh hhhhhhh hhhh hhhhhhhh hhhh hhhhhhhh hhhh hhhhhhhh
MB:hhhhhh  SWITCH:hhhhhh
SENSE FROM:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
  SENSE TO:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

- **See page 12-108 for 'SENSE FROM' and 'SENSE TO' description.**
- **See Table 12-30 on page 12-88 for 'MODE', 'DEFAULT', and 'TO' description.**

MOSS BER Type 01 ID 06 (Error 10/11) - Field Details

Table 12-29 (Page 1 of 3). MOSS BER Type 01 ID 06 (Err 10 to 11) Field Details

Field Name	Bit Pattern or Hex Value	Meaning
STATUS		System status
		Fallback origine
	00	Operator
	10	Automatic
		Fallback nature
	01	Dynamic
MB byte 1		FALLBACK
	x	Error during mailbox exchange
	. x	Port swap error
	. . x	Time out during mailbox
	. . . x	Port swap refused by CP
		SWITCHBACK
	. . . . x . . .	Error during mailbox exchange
	. . . . . x . .	Time out during mailbox
	. . . . . x .	Function not supported
	 x	Not whole configuration
MB byte 2		FALLBACK
	x	MB fallback sent to CP
	. x	Request FB port swap received
	. . x	MB FB port swap sent to CP
	. . . x	FB complete received from CP
		SWITCHBACK
	. . . . x . . .	MB switchback conditional
	. . . . . x . .	MB switchback forced
	. . . . . x .	MB switchback complete
	 x	MB switchback to be sent

Table 12-29 (Page 2 of 3). MOSS BER Type 01 ID 06 (Err 10 to 11) Field Details

Field Name	Bit Pattern or Hex Value	Meaning
MB byte 3	1 xx	Return code from CP xx = 00 MB receive after FB processing xx = 01 No request from NCP xx = 10 CP has half the configuration
SWITCH byte 1		SWITCH PROCESSING
	x	First read of switch
	. x	CA tag reset
	. . x	LA tag reset via normal way
	. . . x	LA tag reset via other way
	. . . . x . . .	Disconnect
	. . . . . x . .	Connect
	. . . . . x .	Last read of switch
	 x	Unused
SWITCH byte 2		SWITCH PROCESSING
	x	Set DMA disable for disconnection
	. x	Reset DMA disable for disconnect
	. . x	Set DMA disable for connection
	. . . x	Reset DMA disable for connection
	. . . . x . . .	Force authorization
	. . . . . x . .	Latch disconnect
	. . . . . x .	Unused
	 x	Unused
SWITCH byte 3		ERROR PROCESSING
	x	Request disconnect
	. x	Request connect
	. . x	Request display
	. . . x	Intervention required on CCU from
	. . . . x . . .	Intervention required on CCU to
	. . . . . x . .	Request stop
	. . . . . x .	Request init of table
	 x	Intervention required
LA		3 bytes per CSP (32 CSPs)
Byte 1		SCB
	x	LPTSS found present in CDF
	. x	TRA found present in the CDF
	. . x	Adapter power ON
	. . . x	Scanner/TRA is presently the scanner/TRA selected
	. . . . x . . .	TIC1 found present in CDF
	. . . . . x . .	TIC2 found present in CDF
	. . . . . x .	LA under control of the CP
	 x	Scanner successfuly IMLed
Byte 2	x	Automatic re-IML failed, or scanner went down twice in the minimum time range or CSP could not be IMLed at general IPL
	. x	Command engaged with scanner failed with a LVL 1 interrupt on MOSS: Interrupt handler failed in trying a get error status register
	. . x	Scanner successfully IMLed and no action (stop, go, connect, disconnect, reset) performed and no scanner error detected: Scanner is initialized
	. . . x	Scanner failure during fallback process
	. . . . x . . .	Scanner failure during fallback on MOSS area high/low commands
	. . . . . x . .	Scanner failure during fallback on IML command
	. . . . . x .	Scanner failure during fallback on INIT command
	 x	HPTSS/ESS found present in the CDF

Table 12-29 (Page 3 of 3). MOSS BER Type 01 ID 06 (Err 10 to 11) Field Details

Field Name	Bit Pattern or Hex Value	Meaning
Byte 3		
	x	Unused
	. xxx	LA type: xxx = 001: TSS xxx = 010: HPTSS xxx = 011: TRSS xxx = 110: ESS
	 xxxx	Target CCU for curent scanner: xxxx = 0001: CCU A xxxx = 0010: CCU B
CA		4 bytes per CA, 16 CAs
Byte 1		Error identification
	x	MIOH failure
	. x	Bad return from CHGCDCA
	. . x	Power OFF
	. . . x	Verify data error
	. . . . x . . .	Bad checkout result
	. . . . . x . .	Chaining error
	. . . . . . x .	Mismatch about TPS between CDF and HW
	 x	Bad return code from CHGCDLCA
Byte 2	x	Bad return code from CHGCAINI
	. x	Bad return from MCAD adapter
	. . x	CA not found in CONNECTED status during p1B/fallback
	. . . x	Chaining not performed due to 2 errors on the bus
	. . . . x . . .	MCAD error when enabling
	. . . . . x . .	MCAD error when disabling
	. . . . . . x .	Discrepancy between CDF and hardware
	 x	Unused
Bytes 3-4	xxxx xxxx xxxx xxxx	CA checkout result

MOSS BER Type 01 ID 06 (Error 12)

Format foM11: see page 12-131. Request to network operator.

```
                                  ELD DETAIL
SEL#:hhhh FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:06
CP< error description line >                 <REFER.CODE IN CHAR.> CCCCCCCC

MOSS-CHECK:12 EVENT-EXT:hh REQ:bbbbbbbb  MODE:hh  DEFAULT:hh  FROM:hh  TO:hh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 06 (Error 12) Field Description

Table 12-30. MOSS BER Type 01 ID 06 (Err 12) Field Details

Field Name	Bit Pattern or Hex Value	Meaning
REQ	 bbbbbbbb = 00010000 bbbbbbbb = 00000001	Switching type: Fallback requested Switchback requested
CONFIG.	hh = 01 hh = 02	Single configuration Twin configuration
DEFAULT	hh = 01 hh = 02	CCU A is the default CCU CCU B is the default CCU
MODE	hh = 01 hh = 02 hh = 03	Standby mode Dual mode Backup mode
FROM-TO FROM TO 	 hh = 01 hh = 02 hh = 01 hh = 02	Fallback / switchback direction CCU FROM which the buses are to be detached CCU A CCU B CCU TO which the buses are to be attached CCU A CCU B

MOSS BER Type 01 ID 06 (Error 13)

Format foM34: see page 12-136. This BER is generated to indicate that a timed IPL will occur soon.

```
                                ELD DETAIL
SEL#:hhhh FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:06
CP< error description line >                <REFER.CODE IN CHAR.> CCCCCCCC

MOSS-CHECK:13  CCU:hh
LOAD MODULE:xxxxxxxx
TIMED IPL DATE/TIME:MM/DD/YY  HH:MM
REFERENCE DATE/TIME:MM/DD/YY  HH:MM


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 06 (Error 14)

Format foM35: see page 12-136. This BER is generated when a timed IPL is cancelled.

```
                                ELD DETAIL
SEL#:hhhh FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:06
CP< error description line >                <REFER.CODE IN CHAR.> CCCCCCCC

MOSS-CHECK:14  CCU:hh
LOAD MODULE:xxxxxxxx
TIMED IPL DATE/TIME:MM/DD/YY  HH:MM
REFERENCE DATE/TIME:MM/DD/YY  HH:MM
MOSS CANCEL ORIGIN:hh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 06 (Error 18)

Format foM47: see page 12-138. This BER is generated for a LSSD string firt part.

```
                                ELD DETAIL
SEL#:hhhh FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:06
CP< error description line >                <REFER.CODE IN CHAR.> CCCCCCCC

LSSD STRING: 192 bytes long


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 06 (Error 28)

Format foM48: see page 12-138. This BER is generated for a LSSD string second part.

```
                                ELD DETAIL
SEL#:hhhh FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:06
CP< error description line >                 <REFER.CODE IN CHAR.> CCCCCCCC

LSSD STRING: 317 bytes long


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 06 (Error 13 and 14) Field Description

Table 12-31. MOSS BER Type 01 ID 06 (Error 13 and 14) Field Details

Field Name	Bit Pattern or Hex Value	Meaning
CCU	hh = 01 hh = 02	CCU A CCU B
LOAD MODULE	xxxxxxxx	Load module name (eight characters max)
TIMED IPL DATE/TIME	MM/DD/YY HH:MM	Date and time of the timed IPL
REFERENCE DATE/TIME	MM/DD/YY HH:MM	Host date and time reference when the timed IPL command is sent
MOSS CANCEL ORIGIN	 hh = 01 hh = 02 hh = 03 hh = 04	 Clock lost Too late MOSS not online IPL running on the other CCU

MOSS BER Type 01 ID 07

Format foM29: see page 12-135. The MOSS microcode generates the following BERs when an error occurs in the MOSS/TRSS interface.

```
                                ELD DETAIL
SEL#:hhhh    FLAG 00 DATE:04/29 TIME:23:45  TYPE:01 ID:07
<ERROR DESCRIPTION>                          <REFER.CODE IN CHAR.> CCCCCCCC
ERROR:hh  TRA ADDR:hhhh      X76:hhhhhh
GET COMMAND  COMPLETION:hhhh
MOSS    ERROR STATUS:hhhh
LEVEL1 ERROR STATUS:hhhh
LEVEL2 ERROR STATUS:
TIC1:hhhh    TIC2:hhhh
TIC CTL REGISTER
bbbbbbbb bbbbbbbb


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Table 12-32. MOSS BER Type 01 ID 07 Field Details		
Field Name	**Bit Pattern or Hex Value**	**Meaning**
ERROR	 hh = 04 hh = 08 hh = 40 hh = 80	Error description No interrupt from TRM Error detected on level 1 Error detected on level 4 Error detected on level 1
TRA ADDR	hhhh	TRA address, see page 3-74.
GET COMMAND COMPLETION	hhhh	See page 5-35
MOSS ERROR STATUS	hhhh	See page 5-52
LEVEL1 ERROR STATUS	hhhh	See page 5-49
LEVEL2 ERROR STATUS TIC1 TIC2	hhhh	See page 5-50
TIC CTL REGISTER	bbbbbbbb bbbbbbbb	See page 5-32

Format foM29a: see page 12-135. The MOSS microcode generates the following BERs when an error occurs on the MOSS/TRSS interface.

```
                                ELD DETAIL
SEL#:hhhh    FLAG 00 DATE:04/29 TIME:23:45  TYPE:01 ID:07
 <ERROR DESCRIPTION>                          <REFER.CODE IN CHAR.> CCCCCCCC
 ERROR:hh  TRA INPUT ADDR:hhhh  TRA OUTPUT ADDR:hhhh
 TIC NBR:hh
 2K BLOCK:  INITIAL    REQUESTED   FINAL
            hhhh        hhhh       hhhh
 STOP COMMAND CNT:hh


  ===>

   F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Table 12-33. MOSS BER Type 01 ID 07 Field Details		
Field Name	**Bit Pattern or Hex Value**	**Meaning**
ERROR	 00 FE	Error description TIC dump completed TIC set storage failure
TRA INPUT ADDR	hhhh	TRA input address from PCW
TRA OUTPUT ADDR	hhhh	TRA output address from PCW
TIC NBR	hh	TRP number
2K BLOK: INITIAL REQUESTED FINAL	 hhhh hhhh hhhh	 Initial block number Requested block number Final block number
STOP COMMAND CNT	hh	Stop command loop count

Format foM29b: see page 12-135. The MOSS microcode generates the following BERs when an error occurs on the MOSS/TRSS interface.

```
                                ELD DETAIL
SEL#:hhhh    FLAG 00 DATE:04/29 TIME:23:45  TYPE:01 ID:07
 <ERROR DESCRIPTION>                            <REFER.CODE IN CHAR.> CCCCCCCC
 ERROR:FF  ERROR-EXT:hh  TRA NBR:hh  TIC NBR:hh
 CCU:hh   TRA ADDR:hhhh


  ===>

   F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Table 12-34. MOSS BER Type 01 ID 07 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
ERROR extension	 01 02 03 04 00	Error description Dump file full Disk error Hardware error Select TRA TIC error When the dump is available
TRA NBR	hh	TRA number (01-04)
TIC NBR	hh	TIC number (01-02)
CCU	hh	CCU 01 = CCUA 02 = CCUB
TRA ADDR	hhhh	TRA address, see page 3-74.

MOSS BER Type 01 ID 08

Format foM16: see page 12-133. The MOSS microcode generates the following BERs when an error occurs on the MOSS/CA interface.

```
        new BER not yet entered
                                ELD DETAIL
 SEL#:hhhh    FLAG 00 DATE:dd/dd TIME:hh:hh  TYPE:01 ID:08
 <ERROR DESCRIPTION>                          <REFER.CODE IN CHAR.> CCCCCCCC
 DUMP:hh TRACE:hh  CA:hh  CCU:hh


  ===>

   F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 08 - Field Details

Table 12-35. MOSS BER Type 01 ID 08 Field Details

Field Name	Hex Value	Meaning
DUMP	00 01 02 03	Dump available Dump full Disk error Threshold. Maximum number of auto-dump (maximun value 5)
TRACE	00 01	Restart trace successful Restart trace failed
CA	 xx	CA addresses from 1 to 16
CCU	 00 01 02	CCU use CCU A and B CCU A CCU B

MOSS BER Type 01 ID 0A

Format foM30a: see page 12-135. The MOSS microcode generates the following BER when an ESS dump is taken.

```
                                ELD DETAIL
SEL#:hhhh    FLAG 00 DATE:04/29 TIME:23:45  TYPE:01 ID:0A
 <ERROR DESCRIPTION>                          <REFER.CODE IN CHAR.> CCCCCCCC
 ERROR CODE:FF  ERROR-EXT:hh  ELA NBR:hh
 ELA ERR STATUS:hh  CCU:hh




  ===>

   F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Table 12-36 (Page 1 of 2). MOSS BER Type 01 ID 0A Field Details

Field Name	Bit Pattern or Hex Value	Meaning
ERR CODE	FF	Always set to FF

Table 12-36 (Page 2 of 2). MOSS BER Type 01 ID 0A Field Details		
Field Name	**Bit Pattern or Hex Value**	**Meaning**
ERROR-EXT	 00 01 02 03 Other	Error extension description Dump successfully completed Dump file already full Dump failed, disk error Dump failed, adapter error Dump failed, unknown cause
ELA NBR	hh	ELA number (01-08)
ELA ERR STATUS	hh	See 4-200.
CCU	hh	CCU 01 = CCUA 02 = CCUB

MOSS BER Type 01 IDs 10 and 11

Format foM14: see page 12-132.

```
                                ELD DETAIL
SEL#:hhhh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:hh
< error description line >                    <REFER.CODE IN CHAR.> CCCCCCCC
IORB:hhhh hhhh hhhh hhhh hh hh hh hh hhhhhhhh CCCCCCCC
     hhhhhhhh hhhhhhhh hhhhhhhh hhhh hhhh hhhh hhhh hhhh

PLIST:hhhhhhhh hhhh hhhh hhhhhhhh hhhhhhhh hhhhhhhh

OC1:CCCCCCCC  OC2:CCCCCCCC  CCUF:CCCCCCCC  CCUB:CCCCCCCC


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 IDs 12, 13, and 14

Format foM15: see page 12-132.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:hh
< error description line >                 <REFER.CODE IN CHAR.> CCCCCCCC
IORB:hhhh hhhh hhhh hhhh hh hh hh hh hhhhhhhh CCCCCCCC
     hhhhhhhh hhhhhhhh hhhhhhhh hhhh hhhh hhhh hhhh hhhh
OC1:CCCCCCCC  OC2:CCCCCCCC  CCUF:CCCCCCCC  CCUB:CCCCCCCC


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

The above screen shows the details of a MOSS BER ID 12

The IORB field pattern changes according to the BER ID:

ID 13

hhhh hhhh hhhhhhhh hh hh hh hh hhhhhhhh
hhhhhhhh hhhhhhhh hhhh hhhh hh

ID 14 hhhh hhhh hhhhhhhh hh hh hh hh hhhhhhhh

MOSS BER Type 01 ID 15

Format foM30: see page 12-135. MOSS-CP interface (mailbox).

```
                                ELD DETAIL
SEL#:hhhh FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:15
CP< error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
IORB: hhhh hhhh hhhhhhhh hh hh hh hh hhhhhhhh
 MRB: hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
      hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh


OC1:CCCCCCCC  OC2:CCCCCCCC  CCUF:CCCCCCCC  CCUB:CCCCCCCC


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 IDs 16 and 1A to 1D

Format foM18: see page 12-133, MOSS-CP interface.

```
                                ELD DETAIL
SEL#:hhhh FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:16
CP< error description line >                <REFER.CODE IN CHAR.> CCCCCCCC

IORB: hhhh hhhh hhhhhhhh hh hh hh hh hhhhhhhh

OC1:CCCCCCCC  OC2:CCCCCCCC  CCUF:CCCCCCCC  CCUB:CCCCCCCC


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Note: PLIST displayed only with BER ID 16.

MOSS BER Type 01 - ID 1E

This BER is generated when a LAN handler check occurs. Format foM36, see page 12-137.

```
                                ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01  ID:1E
  <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
IORB:hhhh hhhh hhhhhhhh hh hh hh hh hhhhhhhh hhhhhhhh
OC1:CCCCCCCC OC2:CCCCCCCC CCUF:CCCCCCCC CCUB:CCCCCCCC


===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 IDs 10 to 16 and 1A to 1E - Field Description

Table 12-37. MOSS BER Type 01 ID 10 to 16 and 1A to 1D Field Description

Field Name	Meaning	Refer to
IORB	Disk input/output request block	PE only
MRB	Mailbox info	"
OC1	Operating control transient area overlay name 8 bytes	"
OC2	Operating control transient area module name 8 bytes	"
CCUF	CCU function transient area module name 8 bytes	
CCUB	CCU background transient area module name 8 bytes	"

MOSS BER Type 01 ID 17

Format foM31: see page 12-136. The MOSS microcode generates the following BERs when an error occurs on the RSF function.

```
                              ELD DETAIL
SEL#:hhhh    FLAG 00 DATE:04/29 TIME:23:56  TYPE:01 ID:17
 <ERROR DESCRIPTION>                          <REFER.CODE IN CHAR.> CCCCCCCC
 MOSS-CHECK:hh  BCLE:hh  CMD:hh
             B STAT:hh A STAT:hh C STAT:hhhhhhhh M STAT:hh



  ===>

   F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 17 - Field Description

Table 12-38. MOSS BER Type 01 ID 17 Field Description

Field Name	Meaning	Refer to
A STAT	Adapter status register	page 12-68
B STAT	Adapter status register	page 12-68
BCLE	Buffer control list element	Page 12-99
CMD	Logical Cmd in the request function	Page 12-100
C STAT	Adapter status register	page 12-68
MOSS-CHECK	MOSS error code	page 12-68
M STAT	Modem status	page 12-69

MOSS BER Type 01 ID 19

BER format foM12: see page 12-132. BER for MOSS IML complete with error.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:19
  < error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
 F:hh
 PANEL NEW  REQ:hh  FCN:hh  SERV:hh
 PANEL OLD  REQ:hh  FCN:hh  SERV:hh
 HEXCODE:hhh hhh hhh hhh hhh hhh hhh hhh hhh hhh hhh hhh hhh hhh hhhhhh hhh
 CDF-RC:hhhh
 ECB DISK:hhhh MIOC  CCUA:hhhh  CCUB:hhhh
 MB CCUA  CMD:hh  STAT:hhhh
 MB CCUB  CMD:hh  STAT:hhhh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 19 - Field Description

Table 12-39. MOSS BER Type 01 ID 19 Field Description

Field Name	Meaning	Refer to
CDF-RC	CDF return code. Normally 0000, otherwise PE only	For PE only
CMD	Logical Cmd in the request function	Page 8-34
ECBDISK	ECB on disk/diskette operation	PE only
F	Error code. Information is collected in case hexadecimal code cannot be displayed on the panel.	Page 12-101
FCN	Selected function	Page 9-3.
MB	• Bytes 1 through 16 (hex 0 thru F): Mailbox REQUEST zone (in/out) (first line on the screen) • Bytes 17 through 32 (hex 10 thru 1F): Mailbox RESPONSE zone (IN/OUT) (second line of the screen)	Page 8-34
MIOC CCUA/B	MIOC ECB for operation on CCUA/B	Page 12-100
PANEL HEXCODE	Hexa code sequence, from the oldest to the more recent one	
PANEL NEW	Panel hex code	
PANEL OLD	Previous hex code	
REQ	Same as field 'ORIGI' in BER 01-20	Page 12-101
SEV	Service mode	Page 9-3.
STAT	Mail box status	Page 12-100

MOSS BER Type 01 ID 20

Format foM21: see page 12-133. IPL after fallback (standby mode), IPL after switchback, fallback, switchback complete without errors. This BER corresponds to one of the following cases:

- General IPL successfully performed.
- Fallback successfully performed.
- Switchback successfully performed.

Whatever the IPL trigger item is (control panel, keyboard, automatic, scheduled, fallback 3745 configured in twin standby mode, or switchback), this BER is logged at IPL completion.

This BER is logged for availability measurement purpose.

```
                                  ELD DETAIL
SEL#:hhhh   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:20
CP< error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
 ORIGI:hh  FUNCTION:hh  SERV:hh  CCU:hh
 STATUS:bbbbbbbb  REQ:hh  LVL1-REQ:bbbbbbbb
 MODE:hh DEFAULT:hh CONF:hh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 IDs 17 and 19 to 20 - Field Details

Some of the following fields may not appear on the BER detail display, but they are part of the BER and they are listed as they appear in the BER file. See the section 'BER Formats on Disk' page 12-128

Table 12-40 (Page 1 of 4). MOSS BER Type 01 IDs 17 and 19 to 20 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
BCLE		Buffer control list element
	00	Enable request
	01	Sense adapter request
	03	Read text/HDR request
	04	Bid preparation request
	06	Write SOH...ETX
	0C	Write bid request
	10	Write EOT request
	14	Disable request
	16	Write STX...ETX
	1E	Write STX...ETB
	3C	Write disconnected request
	80	Halt request flag

Table 12-40 (Page 2 of 4). MOSS BER Type 01 IDs 17 and 19 to 20 Field Details		
Field Name	**Bit Pattern or Hex Value**	**Meaning**
CMD		Logical Cmd in the request function
	80	Open
	40	Send
	20	Send/Receive
	08	Close
	04	Not used
	02	Receive for file Xfer
	01	Line survey
MIOC CCUA/B		MIOC ECB for operation on CCUA/B
Byte 1		
	00	Normal operation
	80	CC time out
	40	CC posted
	20	CC started
	10	CC BER
	08	CC warning
	04	CC adapter down
	02	CC request rejected
	01	CC I/O exception
Byte 2		
	40	No MCCU ID specified
	41	Invalid logical request
	42	Invalid PCW
	43	Channel I/O running
	61	Request truncated
	62	CCU busy bit On
	63	Abort
	64	IOC error
	65	NCP time out
	66	Mail box lock
	67	LSSD error residual count
	68	String select error
	69	No mail box allowed, CCU IPL
	6A	Buffer empty
	6B	MIOC/adapter busy bit On
	6C	MOSS address exception
	6D	MOSS OP check
	6E	CHIO asynchronous error
	6F	CHIO time out
STAT		Mail box status
Byte 1		
	80	Accepted
	40	Rejected
	20	Not used
	10	Not used
	08	Keep buffer
	04	Free buffer
	02	Not used
	01	Not used

Table 12-40 (Page 3 of 4). MOSS BER Type 01 IDs 17 and 19 to 20 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
Byte 2		
	80	Buffer not available
	40	Function not supported
	20	Invalid command
	10	Moss down or Off line
	08	Invalid parameters
	04	Fallback in process
	02	Not used
	01	Enable to queue SNA req.
MOSS-CHECK		IPL complete without errors BER complementary information
	01	IPL
	02	IPL after fallback
	03	IPL after switchback
	04	Fallback
	05	Switchback
	06	IPL complete on standby
F		Error code
	x	IML not successful
	. x	Alarm indicator A0 has to be generated
	. . xx	Unused
	. . . . xxx .	Operation with power failed for: x . . . Get end of IML data . x . . Get stacked error record . . x . Panel hex display
	 x	Unused
ORIGI		Origin of MOSS code activation
	x	Machine power-ON
	. x	Machine reset
	. . x	MOSS power-ON
	. . . x	MOSS reset
	. . . . x . . .	MOSS automatic re-IML
	. . . . . 1 . .	Forced origin The origin of the ROS code activation is forced to the previous activation (for example: machine power ON, machine reset, MOSS power ON) NOTE: this bit is meaningful when a MOSS reset occurs before all the MOSS control blocks initialization by the IML processor.
	. . . . . x .	Forced selection. This bit is set ON when the MOSS diags cannot get from the MPWL valid information defining the origin, the function or service mode. In such a case default values are Origin: MOSS power ON Function: MOSS IML from disk Service: CE mode
	 x	Unused
FUNCTION		Function selection
	00	General IPL with IML from disk
	01	MOSS IML from disk
	02	MOSS dump
	05	Remote console link test
	07	RSF console link test
	08	Local console link test
	09	Diskette mode
	0A	Loop on MOSS diagnostics

Table 12-40 (Page 4 of 4). MOSS BER Type 01 IDs 17 and 19 to 20 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
SERV		Service selection
	00	Normal Customer mode
	01	Maint 1 CE mode
	02	Maint 2 By-pass MOSS diags
	03	Maint 3 First installation
CCU		CCU identification
	01	CCU A
	02	CCU B
STATUS	x	IPL mode (IPLMODE) x = 0 <==> Operator x = 1 <==> Automatic
	. x	Customer / Maintenance (MTMENU) x = 0 <==> Customer x = 1 <==> Maintenance
	. . x	Previous fallback x = 0 <==> Manual x = 1 <==> Automatic
	. . . 1	Dynamic fallback
REQ	01	IPL on power ON reset
	02	CCU + scanners IPL req from KB/D
	03	IPL requesting IPL of other CCU
	04	IPL requesting fallback
	05	Fallback requesting IPL
	06	Switchback requesting IPL
	07	IPL is requested by the level 1
	08	Scheduled or network power ON reset
	09	IPL after fallback
	0A	Manual fallback requested
	0B	IPL of standby CCU requested
	0C	Timed IPL requested
LVLE-REQ		Identification of CCU IPL request
	0000 0010	CCU hardcheck
	0000 0111	Output 70 received
	0000 0011	Program request IPL
	0000 0100	Channel request IPL
CONF		3745 configuration
	01	Single configuration
	02	Twin configuration
DEFAULT		Default CCU:
	01	CCU A is the default CCU
	02	CCU B is the default CCU
MODE		3745 mode:
	01	Standby mode
	02	Dual mode
	03	Backup mode

MOSS BER Type 01 ID 21

Format foM23: see page 12-134. This BER is logged for availability measurement purposes.

IPL, IPL after fallback (standby mode), IPL after switchback, fallback, switchback started. This BER corresponds to one of the following cases:

- IPL has been requested from the KB/D
- Fallback started
- Switchback started.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:21
APPL < error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
EVENT-EXT:hh
STATUS:bbbbbbbb CCU:hh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 21 Field Details

Some of the following fields may not appear on the BER detail display, but they are part of the BER and they are listed as they appear in the BER file. See the section 'BER Formats on Disk' page 12-128

Table 12-41 (Page 1 of 2). MOSS BER Type 01 ID 21 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
EVENT-EXT		Complementary IPL information
	01	IPL
	02	IPL after fallback
	03	IPL after switchback
	04	Fallback
	05	Switchback
	06	IPL started on standby
STATUS	xxxx xx . .	Unused
	. . . . . x .	IPL mode (IPLMODE) x = 0 <==> operator x = 1 <==> automatic
	 x	Customer / Maintenance (MTMENU) x = 0 <==> customer x = 1 <==> maintenance
CCU		CCU identification
	01	CCU A
	02	CCU B

Table 12-41 (Page 2 of 2). MOSS BER Type 01 ID 21 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
CONFIG.		3745 configuration:
	01	Single configuration
	02	Twin configuration
		Default CCU:
	01	CCU A is the default CCU
	02	CCU B is the default CCU
		3745 mode:
	01	Standby mode
	02	Dual mode
	03	Backup mode

MOSS BER, Type 01 ID 22 and 40

Format foM20: see page 12-133. Fallback complete with errors (ID 22), and switchback complete with errors (ID 40).

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:hh
APPL < error description line >                 <REFER.CODE IN CHAR.> CCCCCCCC
MODE:hh  DEFAULT:hh  TO:hh  STATUS:bbbbbbbb
LA:hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh
   hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh
   hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh
   hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh
CA:hhhhhhhh hhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
   hhhhhhhh hhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
MB:hhhhhh  SWITCH:hhhhhh
SENSE FROM:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
  SENSE TO:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh  FLAGS:hh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER IDs 22 and 40 - Field Details

Some of the following fields may not appear on the BER detail display, but they are part of the BER and they are listed as they appear in the BER file. See the section 'BER Formats on Disk' page 12-128

Table 12-42 (Page 1 of 5). MOSS BER Type 01 IDs 22 and 40 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
STATUS	x . . . . 1 . . . . 1	Fallback requestor: x = 0 <==> manual request x = 1 <==> automatic request Error when reading the check record pool Dynamic fallback
CONFIG	 01 02	3745 CONFIGURATION Single configuration Twin configuration
DEFAULT	 01 02	 CCU A is the operational CCU CCU B is the operational CCU
MODE 01 02 03	 Standby mode Dual mode Backup mode	
TO	 01 02	Fallback target CCU CCU A supports the whole configuration CCU B supports the whole configuration
LA		32 blocks of 2 bytes (1 block per CS), displayed as 4 hexadecimal characters

Table 12-42 (Page 2 of 5). MOSS BER Type 01 IDs 22 and 40 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
Byte 1	x	LSS is found present in CDF
	. x	TRA is found present in the CDF
	. . x	Adapter is power ON
	. . . x	Scanner/TRA is presently the scanner selected
	. . . . x . . .	TIC1 found present in CDF
	. . . . . x . .	TIC2 found present in CDF
	. . . . . . x .	LA under control of the CP
	 x	Scanner successfully IMLed
Byte 2	x	Automatic re-IML has failed, or scanner went down twice in the minimum time range or CSP could not be IMLed at general IPL
	. x	Command engaged with scanner failed with a LVL 1 interrupt on MOSS: interrupt handler has tried a get error status register which failed
	. . x	The scanner has been successfully IMLed and no action (stop, go, connect, disconnect, reset) has been performed and no scanner error has been detected: Scanner is initialized
	. . . x	Scanner failure during fallback
	. . . . x . . .	Scanner failure during fallback on MOSS area high/low commands
	. . . . . x . .	Scanner failure during fallback on IML command
	. . . . . . x .	Scanner failure during fallback on INIT command
	 x	HPTSS/ESS found present in the CDF
Byte 3		
	x	Unused
	. xxx	LA type: xxx = 001: TSS xxx = 010: HPTSS xxx = 011: TRSS xxx = 110: ESS
	 xxxx	Target CCU for curent scanner: xxxx = 0001: CCU A xxxx = 0010: CCU B
CA		16 blocks of 4 bytes (1 block per CA), displayed as 4 hexadecimal characters
Byte 1		ERROR IDENTIFICATION
	x	MIOH failure
	. x	Bad return from CHGCDCA module
	. . x	Power OFF
	. . . x	Verify data error
	. . . . x . . .	Bad checkout result
	. . . . . x . .	Chaining error
	. . . . . . x .	Mismatch about TPS between CDF and HW
	 x	Unused
Byte 2	x	Init error
	. x	Bad return from MCAD adapter
	. . x	CA not found in 'CONNECTED' status during phase 1B/fallback
	. . . x	Chaining not performed due to 2 errors on the bus
	. . . . x . . .	MCAD error when enabling
	. . . . . x . .	MCAD error when disabling
	 xx	Unused
Bytes 3-4	xxxx xxxx xxxx xxxx	CA checkout result

Table 12-42 (Page 3 of 5). MOSS BER Type 01 IDs 22 and 40 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
IPL checking	x . . . . x . . . . x . . . . x . . . . x . . . . x . . . . x x	Unexpected IPL option Unexpected CCU selection Unexpected undefined PF key No CCU under IPL, IPL started No CCU specified for BER Unknown switch request Unexpected display request Unused
MB	 0000 0000	FALLBACK INFORMATION Initialization value
MB byte 1	 x . . . . x . . . . x . . . . x . . . . x . . . . x . . . . x x	FALLBACK Error during mailbox exchange Port swap error Time out during mailbox Port swap refused by CP SWITCHBACK Error during mailbox exchange Time out during mailbox Function not supported Not whole configuration
MB byte 2	 x . . . . x . . . . x . . . . x . . . . x . . . . x . . . . x x	FALLBACK MB fallback sent to CP Request FB portswap received MB FB port swap sent to CP FB complete received from CP SWITCHBACK MB switchback conditional MB switchback forced MB switchback completed MB switchback to be sent
MB byte 3	 1 . . . . . 00 1 . . . . . 01 1 10	Return code from CP MB receive after 4 FB processing No request from NCP CP has half the configuration
SWITCH		
Byte 1	 0000 0000 x . . . . x . . . . x . . . . x . . . . x . . . . x . . . . x x	SWITCH PROCESSING Initialization value First read of switch CA tag reset LA tag reset via normal way LA tag reset via other way Disconnect Connect Unused
Byte 2	 x . . . . x . . . . x . . . . x . . . . x . . . . x . . . . x x	SWITCH PROCESSING Set DMA disable for disconnection Reset DMA disable for disconnection Set DMA disable for connection Reset DMA disable for connection Force authorization Latch disconnect Unused Error during channel disabling

Table 12-42 (Page 4 of 5). MOSS BER Type 01 IDs 22 and 40 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
Byte 3		ERROR PROCESSING
	x	Request disconnect
	. x	Request connect
	. . x . . .	Request display
	. . . x . . .	Intervention required on CCU FROM
	. . . . x . . .	Intervention required on CCU TO
	. . . . . x . .	Request stop
	. . . . . x .	Request init of table
	 x	Intervention required
Sense FROM	1111 1110	Initialization value
8 bytes		IOC 1 - NORMAL WAY
	xxxx xxxx	DATA0 - primary
	xxxx xxxx	DATA0 - secondary
	xxxx xxxx	DATA1 - primary
	xxxx xxxx	DATA1 - secondary
	xxxx xxxx	TAG 1 - primary
	xxxx xxxx	TAG 1 - secondary
	xxxx xxxx	TAG 3 - primary
	xxxx xxxx	TAG 3 - secondary
8 bytes		IOC 2 - NORMAL WAY
	xxxx xxxx	DATA0 - primary
	xxxx xxxx	DATA0 - secondary
	xxxx xxxx	DATA1 - primary
	xxxx xxxx	DATA1 - secondary
	xxxx xxxx	TAG 1 - primary
	xxxx xxxx	TAG 1 - secondary
	xxxx xxxx	TAG 3 - primary
	xxxx xxxx	TAG 3 - secondary
8 bytes		DMA - NORMAL WAY
	xxxx xxxx	Unused
	xxxx xxxx	Unused
	xxxx xxxx	Unused
	xxxx xxxx	Unused
	xxxx xxxx	TAG 1 - primary
	xxxx xxxx	TAG 1 - secondary
	xxxx xxxx	TAG 2 - primary
	xxxx xxxx	TAG 2 - secondary
Sense TO	1111 1110	Initialization value
8 bytes		IOC 1 - OTHER WAY
	xxxx xxxx	DATA0 - primary
	xxxx xxxx	DATA0 - secondary
	xxxx xxxx	DATA1 - primary
	xxxx xxxx	DATA1 - secondary
	xxxx xxxx	TAG 1 - primary
	xxxx xxxx	TAG 1 - secondary
	xxxx xxxx	TAG 3 - primary
	xxxx xxxx	TAG 3 - secondary

Table 12-42 (Page 5 of 5). MOSS BER Type 01 IDs 22 and 40 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
8 bytes		IOC 2 - OTHER WAY
	xxxx xxxx	DATA0 - primary
	xxxx xxxx	DATA0 - secondary
	xxxx xxxx	DATA1 - primary
	xxxx xxxx	DATA1 - secondary
	xxxx xxxx	TAG 1 - primary
	xxxx xxxx	TAG 1 - secondary
	xxxx xxxx	TAG 3 - primary
	xxxx xxxx	TAG 3 - secondary
8 bytes		DMA - OTHER WAY
	xxxx xxxx	Unused
	xxxx xxxx	Unused
	xxxx xxxx	Unused
	xxxx xxxx	Unused
	xxxx xxxx	TAG 1 - primary
	xxxx xxxx	TAG 1 - secondary
	xxxx xxxx	TAG 2 - primary
	xxxx xxxx	TAG 2 - secondary
FLAGS		Automatic fallback causes:
	 111	CCU power drop
	 010	CCU hardcheck

MOSS BER Type 01 - ID 23

This BER is generated when a 37CS re-IML is completed. Format foM37, see page 12-137.

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01   ID:23
  <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
CCU:hh




===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 - ID 2A

This BER is generated when an ESCA RE-IPL failed. Format fom38, see page 12-137.

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01  ID:2A
  <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
TA:hh
SLID:hhhhhhhh
CCU:hh



===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 - ID 2B

This BER is generated when a RE-IPL has started on a line, a CA, or an ESCA. Format foM39, see page 12-137.

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01  ID:2B
  <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
TA BYTE 0:hh
TD BYTE 1:hh
CCU:hh
ORIGIN:hh


===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 - ID 2C

This BER is generated for a DL2 call completion. Format foM45, see page 12-138.

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01  ID:2C
  <ERROR DESCRIPTION>                             <REFER.CODE IN CHAR.> CCCCCCCC
COMPLETION CODE :hhhh
CPN :cccc
CCU :hh
REFERENCE CODE :cccccccc cccccccc cccccccc

===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 - ID 2D

This BER is generated for a CP dump transfer error, the dump is purged. Format foM46, see page 12-138.

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01  ID:2D
  <ERROR DESCRIPTION>                             <REFER.CODE IN CHAR.> CCCCCCCC
CCU :hh
REASON :hh

===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 - ID 2E

This BER is generated for a CP dump transfer error, the dump is purged. Format foM50, see page 12-139.

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01  ID:2E
  <ERROR DESCRIPTION>                             <REFER.CODE IN CHAR.> CCCCCCCC
IML ORIGIN :hh
LOW ADDR :hh
HIGH ADDR :hh
ADNO :hh

===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 23 and 2A to 2E Field Details

Field Name	Hex Value	Meaning
ADNO		LAN or ESCA adapter number

Field Name	Hex Value	Meaning
CCU	00	CCU A and B
	01	CCU A
	02	CCU B
IML ORIGIN	01	General 3746-900 IML
	02	LAN selective IML
	03	ESCA selective IML
ORIGIN	01	Re-IPL started on line xxxx (Alarm = 15)
	02	Re-IPL started on CA xxxx (Alarm = 17)
	03	Re-IPL started on ESCA xxxx (Alarm = 18)
	Other	Re-IPL started from RLA process xxxx (Alarm = 16)
SLID		System logical ID
TA		Page 3-64
TD		Page 3-64
COMPLETION CODE	01	Call RETAIN not successful
	02	Call RETAIN not authorized
	03	Call RETAIN OK hardware problem
	04	Call RETAIN OK microcode problem plus fix down loaded to MOSS-E
	05	Call RETAIN OK microcode problem without fix
CPN	ccc	Customer problem number
REASON	01	LAN error, link down
	02	MOSS-E microcode error
	03	HDD disk error
	04	Umacht block number
	05	Re-IML during transfer
REFERENCE CODE		Reference code reported to RETAIN

MOSS BER Type 01 IDs 24 to 29, and 37

Format f0M24: see page 12-134. CA concurrent maintenance BER.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:hh
APPL < error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
CA:hh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 30

Format foM25: see page 12-134. Adapter error.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:30
APPL < error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
FRU GROUP:hhhh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 31

Format fom26: see page 12-134. Adapter error.

```
                                ELD DETAIL
SEL#:ddd   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:31
APPL < error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
PLIST:hhhhhhhh  PRB:hhhhhhhh  SRB:hhhhhhhh  OP:hhhhhhhh  ERR:hhhh
DISC:bbbbbbbb  DATA:hh  CMD:hhhh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 32

Format foM27: see page 12-134. MCAD error.

```
                                ELD DETAIL
SEL#:ddd   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:32
APPL < error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
PLIST:hhhhhhhh  PRB:hhhhhhhh  DATA:hh  CMND:hhhh   ERR:hhhh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 IDs 30, 31, and 32 - Field Description

Table 12-43 (Page 1 of 2). MOSS BER Type 01 IDs 30, 31, 32 Field Description

Field Name	Meaning	Refer to
FRU GROUP	List of FRUs to exchange	MIP Chapter 1
PLIST	Pointer to IORB list	
PRB	Current IORB pointer value	
SRB	Switch request block	
OP	Current IORB multiple operation	
ERR	Return code from adapter	page 12-66
DISC	SWAD disconnect register	page 12-54

Table 12-43 (Page 2 of 2). MOSS BER Type 01 IDs 30, 31, 32 Field Description

Field Name	Meaning	Refer to
DATA CMD	Data sent to adapter Command sent to adapter	

MOSS BER Type 01 ID 33

Format foM32: see page 12-136. Backup resources test during IPL

```
                              ELD DETAIL
SEL# 3      FLAG 00 DATE:04/29 TIME:23:58  TYPE:01 ID:33
APPL BACKUP CCU TEST CHECK hhhh                <REFER.CODE IN CHAR.> CCCCCCCC
CCU:hh
IAR:hhhhhh  LAR:hhhhhh  SAR:hhhhhh
X70:hhhhhh  X76:hhhhhh  X7D:hhhhhh  X7E:hhhhhh
HDCK:hhhh
MIS:hh hh hh hh hh hh hh hh hh hh hh hh
    hh hh hh hh hh hh hh hh hh hh hh hh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Note: See Chapter 2 for IAR, LAR, SAR, X70, X76, X7D, and X7E registers.

BER TYPE 01 ID 33 - Field Details

Table 12-44. MOSS BER Type 01 ID 33 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
CCU TEST CHECK		
Byte 1	00 01 02	Complete Check (sfotware) Hardcheck (hardware)
Byte 2		Unused
CCU	 01 02	CCU identification CCU A CCU B
Abend code	0Fxx	Check code (see *MIP, Appendix A*)
Check out results		Diag error information (24 bytes). See 12-79

MOSS BER Type 01 ID 36

Cyclic hour notification

```
                                ELD DETAIL
SEL#:ddd   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:36
APPL < error description line >                <REFER.CODE IN CHAR.> CCCCCCCC


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 38

Format foM28: see page 12-134. CA concurrent maintenance NCP request to cancel

```
                                ELD DETAIL
SEL#:ddd   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:38
APPL < error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
ERR1:hhhh  ERR2:hhhh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 ID 39

Format foM33: see format page 12-136. MMIO interface.

```
                                ELD DETAIL
SEL#:ddd   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:39
APPL < error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
IORV:hh  PIRV:hh  PIC: STATUS:hh  REQ:hh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 IDs 38 and 39 - Field Description

Table 12-45. MOSS BER Type 01 IDs 38 and 39 Field Description

Field Name	Meaning	Refer to
ERROR 1	Error code 1 (contains CCU-OUTPUT X57 request from NCP)	page 12-117
ERROR 2	Error code 2 (contains CCU-INPUT X57 return from MOSS)	page 12-117
IORV	I/O request vector	page 12-51
PIRV	Program interrupt request vector	page 8-14
PIC	Controller IPL type	
REQ	Mailbox information	

MOSS BER Type 01 IDs 38 and 39 - Field Details

Table 12-46. MOSS BER Type 01 IDs 38 and 39 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
CCU INPUT X57 Byte 0	x	CA 5 MOSS request pending
	. x	CA 6 MOSS request pending
	. . x	CA 7 MOSS request pending
	. . . x	CA 8 MOSS request pending
	. . . . x . . .	CA 13 MOSS request pending
	. . . . . x . .	CA 14 MOSS request pending
	. . . . . . x .	CA 15 MOSS request pending
	 x	CA 16 MOSS request pending
Byte 1	x	CA 1 MOSS request pending
	. x	CA 2 MOSS request pending
	. . x	CA 3 MOSS request pending
	. . . x	CA 4 MOSS request pending
	. . . . x . . .	CA 9 MOSS request pending
	. . . . . x . .	CA 10 MOSS request pending
	. . . . . . x .	CA 11 MOSS request pending
	 x	CA 12 MOSS request pending
CCU OUTPUT X57 Byte 0	x	Set/reset CA 5 MOSS request
	. x	Set/reset CA 6 MOSS request
	. . x	Set/reset CA 7 MOSS request
	. . . x	Set/reset CA 8 MOSS request
	. . . . x . . .	Set/reset CA 13 MOSS request
	. . . . . x . .	Set/reset CA 14 MOSS request
	. . . . . . x .	Set/reset CA 15 MOSS request
	 x	Set/reset CA 16 MOSS request
Byte 1	x	Set/reset CA 1 MOSS request
	. x	Set/reset CA 2 MOSS request
	. . x	Set/reset CA 3 MOSS request
	. . . x	Set/reset CA 4 MOSS request
	. . . . x . . .	Set/reset CA 9 MOSS request
	. . . . . x . .	Set/reset CA 10 MOSS request
	. . . . . . x .	Set/reset CA 11 MOSS request
	 x	Set/reset CA 12 MOSS request

MOSS BER Type 01 ID 40

See MOSS BER Type 01 ID 22

MOSS BER Type 01 ID 50

This BER is logged after three unsuccessfull sign ON attempts on the remote console. There is no data in this BER. It only displays the message:

```
REMOTE CONSOLE REJECTED
```

MOSS BER Type 01 ID 80

See MOSS BER Type 01 ID 00, 12-43

MOSS BER Type 01 IDs 91, B3, C1, C2

Format foM8: see page 12-130.

NCP/PEP program level 4 generates BERs 91, B3, C1, and C2 if a MOSS error occurs during a mailbox exchange. This BER is transferred to MOSS if MOSS successfully recovers from the MOSS error.

These BERs should always be accompanied by MOSS BER IDs 00, 01, 02, or 03. When BER ID 91 is not accompanied by one of these BERs, it only means that the MOSS has been inoperative during a period of time (MOSS re-IML, MOSS dump) and the BER ID is logged for information only.

```
                                  ELD DETAIL
SEL#:ddd   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:hh
CP< error description line >                 <REFER.CODE IN CHAR.> CCCCCCCC
 MB:hh hh hhhh hh hhhhhh hhhh hhhh hhhh hhhh
    hhhh hh hhhhhh hhhh hhhhhhhh hhhhhhhh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 - ID A0

This BER is generated for a MOSS/MOSS-E token ring adapter error. Format fom40, see page 12-137.

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01  ID:A0
  <ERROR DESCRIPTION>                             <REFER.CODE IN CHAR.> CCCCCCCC
ERROR CODE :hhhh
PANEL CODE :ccc
IML REQUEST :hhhhhh
MOSS MODEL :hh
DIAG STATUS :hhhhhhhh


===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 - ID A1

This BER is generated for a MOSS/MOSS-E link problem. Format fom41, see page 12-137.

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01  ID:A0
  <ERROR DESCRIPTION>                             <REFER.CODE IN CHAR.> CCCCCCCC
REASON :hh
PANEL CODE :ccc


===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 - ID A2

This BER is generated for a MOSS/MOSS-E link re-opened problem. Format fom42, see page 12-137.

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01  ID:A2
  <ERROR DESCRIPTION>                             <REFER.CODE IN CHAR.> CCCCCCCC
OLD PANEL CODE :ccc



===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 - ID A3

Format fom43, see page 12-138.

This BER is generated for an invalid PICA message

```
                                ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01  ID:A3
  <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
MOSSCHK :01  SLID :hhhhhhhh
YYSTATUS :hh  TYPE :hh
CAUSE :hh  IA :hhhhhhhh
RCV MSG :hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
         hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
         hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhh

===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

This BER is generated for a FSM error

```
                                ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01  ID:A3
  <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
MOSSCHK :02  SLID :hhhhhhhh
YYSTATUS :hh  TYPE :hh
IA :hhhhhhhh
RCV MSG :hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
         hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
         hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhh


===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

This BER is generated for an invalid routing

```
                                ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01  ID:A3
  <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
MOSSCHK :03  SLID :hhhhhhhh
TRANID :hhhhhhhh  RESPONSE :hhhhhhhh
IA :hhhhhhhh


===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

This BER is generated for an invalid server name

```
                                ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01  ID:A3
  <ERROR DESCRIPTION>                               <REFER.CODE IN CHAR.> CCCCCCCC
MOSSCHK :04  SLID :hhhhhhhh
TRANID :hhhhhhhh  TYPE :hh
SERVER NAME :cccccccc  IA :hhhhhhhh


===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

This BER is generated for an unmatched SSA response

```
                                ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01  ID:A3
  <ERROR DESCRIPTION>                               <REFER.CODE IN CHAR.> CCCCCCCC
MOSSCHK :05  SLID :hhhhhhhh
TRANID :hhhhhhhh  REQUEST :hh hhhhhhhh hhhhhhhh
RESPONSE :hhhhhhhh  IA :hhhhhhhh


===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

This BER is generated for an expected message not received

```
                                ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01  ID:A3
  <ERROR DESCRIPTION>                               <REFER.CODE IN CHAR.> CCCCCCCC
MOSSCHK :06  SLID :hhhhhhhh
TRANID :hhhhhhhh  YYSTATUS :hh
CAUSE :hh  REQUEST :hh hhhhhhhh hhhhhhhh
IA :hhhhhhhh


===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 - ID A4

This BER is generated by a LAN interface code (MOSS level 3). Format fom44, see page 12-138.

```
                                ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01  ID:A4
  <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
MOSSCHK :hh  REASON :hh
MAJRQCOD :hh  MINRQCOD :hh  MAJRCCOD :hh
MINRCCOD :hh  OPENERRC :hhhh
RINGSTAT :hhhh  LINKSTAT :hhhh
LAN STATUS :hh  LAN MANAGER STATUS :hh
IA :hhhhhhhh  MAC ADDRESS :hhhh hhhhhhhh

                                                                   PAGE 1 OF 2
===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

This second page is generated when DLC or MAC counters are different of zero and when one of the MAC counters is ≥ 80, or when XMIT ERR or RCVD ERR counter is ≥ 80.

```
                                ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01  ID:A4
  <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
                 DLC COUNTERS
XMIT COUNT :hhhh  RCVD COUNT :hhhh  XMIT ERR :hh    RCVD ERR :hh
T1 EXPIRED :hhhh  RCVD CMD :hh      SEND CMD :hh    PRMY STATE :hh
SCDY STATE :hh    STATION VS :hh    STATION VR :hh  STATION VA :hh
                 MAC ERR COUNTERS
LINE :hh               INTERNAL :hh    BURST :hh           ARI/FCI :hh
ABORT DELIMITER :hh    LOST FRAME :hh  RECEIV CONGESTION :hh
FRAME COPIED :hh       FREQUENCY :hh   TOKEN :hh

                                                                   PAGE 2 OF 2
===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

This second page is generated when the MAC counters are = to zero and when one DLC counter is different of zero.

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01  ID:A4
  <ERROR DESCRIPTION>                             <REFER.CODE IN CHAR.> CCCCCCCC
                 DLC COUNTERS
XMIT COUNT :hhhh  RCVD COUNT :hhhh  XMIT ERR :hh    RCVD ERR :hh
T1 EXPIRED :hhhh  RCVD CMD :hh      SEND CMD :hh    PRMY STATE :hh
SCDY STATE :hh    STATION VS :hh    STATION VR :hh  STATION VA :hh

                                                                PAGE 2 OF 2
===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

This second page is generated when the DLC counters are = to zero and when one MAC counter is different of zero.

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:01  ID:A4
  <ERROR DESCRIPTION>                             <REFER.CODE IN CHAR.> CCCCCCCC
                 MAC ERR COUNTERS
LINE :hh               INTERNAL :hh    BURST :hh           ARI/FCI :hh
ABORT DELIMITER :hh    LOST FRAME :hh  RECEIV CONGESTION :hh
FRAME COPIED :hh       FREQUENCY :hh   TOKEN :hh

                                                              PAGE 2 OF 2
===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

MOSS BER Type 01 IDs A0 to A4 - Field Description

Field Name	Meaning	Refer to
ERROR CODE	Error code	See page 12-125
PANEL CODE	Control panel code	MIP Chapter 1
IML REQUEST	IML request	
	Byte 1 = Origin	See page 12-125
	Byte 2 = Fonction	See page 12-125
	Byte 3 = Service	See page 12-125
MOSS MODEL	MOSS model	See page 12-125
DIAG STATUS	Diagnostic status	*
REASON CODE	Reason code	See page 12-126
MOSSCHK	MOSS check	See page 12-126
SLID	System logical identification	-
TRANID	Transaction identification	-
YYSTATUS	Lan status (open phase)	See page 12-126
TYPE	FRB type in error	See page 12-127
CAUSE	MOSS check cause	See page 12-127
REQUEST	Previous request summary	*
RESPONSE	SSA command header	*
SERVER NAME	Server name	-
IA	Instruction address	-
MAJRQCOD	Major request code	*
MINRQCOD	Minor request code	*
MAJRCCOD	Major return code	*
MINRCCOD	Minor return code	*
OPENERRC	Open error code	*
RINGSTAT	Ring status	*
LINKSTAT	Link status	*
LAN STATUS	LAN status	*
LAN MANAGER STATUS	LAN manager status	*
MAC ADDRESS	MAC address	-
T1 EXPIRED	T1 timer expired counter	-
PRMY STATE	Primary state counter	-
SCDY STATE	Secondary state counter	-
STATION VS	Station VS counter	-
STATION VR	Station VR counter	-
STATION VA	Station VA counter	-

* = PE only

Table 12-47 (Page 1 of 3). MOSS BER Type 01 IDs A1 to A4 Field Details

Field Name Hex Value	Meaning	
ERROR CODE		
	01	MLA or MPC interface problem
	02	MLA problem
	03	MLA or MPC or MMIO bus problem level 0
ORIGIN		Origin of MOSS code activation
	x	Machine power-ON
	. x	Machine reset
	. . x	MOSS power-ON
	. . . x	MOSS reset
	. . . . x . . .	MOSS automatic re-IML
	. . . . . 1 . .	Forced origin The origin of the ROS code activation is forced to the previous activation (for example: machine power ON, machine reset, MOSS power ON) NOTE: this bit is meaningful when a MOSS reset occurs before all the MOSS control blocks initialization by the IML processor.
	. . . . . x .	Forced selection. This bit is set ON when the MOSS diags cannot get from the MPWL valid information defining the origin, the function or service mode. In such a case default values are Origin: MOSS power ON Function: MOSS IML from disk Service: CE mode
	 x	Unused
FUNCTION		Function selection
	00	General IPL with IML from disk
	01	MOSS IML from disk
	02	MOSS dump
	05	Remote console link test
	07	RSF console link test
	08	Local console link test
	09	Diskette mode
	0A	Loop on MOSS diagnostics
SERVICE		Service selection
	00	Normal Customer mode
	01	Maint 1 CE mode
	02	Maint 2 By-pass MOSS diags
	03	Maint 3 First installation
MOSS MODEL		
	40	1 MB storage invalid
	80	MLA card not plugged
	C0	3745 is a model 21A-61A

Table 12-47 (Page 2 of 3). MOSS BER Type 01 IDs A1 to A4 Field Details

Field Name Hex Value	Meaning	
REASON		
	8D	Solid MMIO error
	8E	Intermitent MMIO error
	8F	Adapter check
	90	Hardware initialization error
	91	Microcode error
	92	Lobe media test failure
	93	Signal loss while opening
	94	Wire fault while opening
	95	Open frequency error
	96	Time-out while opening
	97	Ring failure while opening
	98	Ring beaconing while opening
	99	Duplicate node address
	9A	Open request parameters
	9B	Open remove received
	9C	Open IMPL force received
	9D	No monitor for RPL at open
	9E	Lobe wire fault at open
	9F	Remote station connect time-out
	B0	Link lost
	B1	DM/DISC received/acknowledged
	B2	FRMR received
	B3	SABME received
	B4	TI timer expired
	B5	FRMR sent
	B6	Unexpected SABME received
	C0	Permanent ring beaconing
	C1	Lobe wire fault
	C2	Auto removal while beacon
	C3	Remove received
	C4	Auto removal
	D0	FSM time-out
MOSSCHK (BER 01 ID A3)		
	01	Invalid PICA message
	02	FSM error
	03	Invalid routing
	04	Invalid server name
	05	Unmatched SSA response
	06	Expected message not received
MOSSCHK (BER 01 ID A4)		
	01	MOSS/MOSS-E link hardware problem
	02	MOSS/MOSS-E link microcode problem
	03	Excessive MAC soft error or Excessive DLC soft error or DLC/MAC statistic adapter coumters or I-frame counters overflow or MAC error counters overflow
	04	Frame lost on MOSS/MOSS-E link
YYSTATUS		
	01	Closed
	02	Adapter opened
	03	Found detected
	04	IML complete
	05	OK detected
	06	Link connected
	07	Service connection opened
	08	Connection opened
	09	Dialog created
	0A	SSA-UP

Table 12-47 (Page 3 of 3). MOSS BER Type 01 IDs A1 to A4 Field Details

Field Name **Hex Value**	**Meaning**	
TYPE		
	01	PICA
	02	SSA
	03	Server connect
	04	Server disconnect
CAUSE		
	01	Not supported ILTOP
	02	Not supported POC
	03	Invalid path value
	04	Not supported PICA message
	05	SSA time-out
	06	FSM time-out

BER Formats on Disk

BERs Printed on Host

The length of the BERs printed from the disk on the host is not significant. When the BER detail is displayed on the console display, only the useful information is given. The remaining BER bytes, if any, printed but not displayed, have no meaning. Do not try to interpret them, they may lead to erroneous actions.

MOSS BER Type 01 - Formats

Format: foM0

IDs: 00 80	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30-31	MOSS CHECK
32-33	Action code
34-35	Hexadecimal code
36	EIRV
37-38	DIV
39	IORV
40	PIRV
41	CPLLPL
42	CM
43	MM
44	CHM
45	Spare
46-49	IA
50-53	PSCI
54-57	OP
58-105	Regs interrupt LVL
106-107	CHCV
108-109	Register space
110-113	Main storage loc.
114-117	CHIO (current)
118-119	DUMP
120	MOSS dump stat
121	EIRV (1)
122	IORV (1)
123	PIRV (1)
124-125	DIV (1)
130-133	PSCI (1)
134-137	OP (1)
138-142	PCA1
143-147	PCA2
148-152	PCA3
153	Unused
154-165	MCCUA
166-177	MCCUB
178-181	SWAD
182-193	MCAD
194-196	DFA
197	TOD
198-224	Snapshot dump
225-232	Module name
233-251	Spurious error cnt
252-289	Statistics count

Format: foM1

ID: 01	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	ABEND
31	Flag
32-33	WHO/WHAT - CHECK
34-35	Recovery action
36-47	MCCUA REGS
48	CCUA CMSA
49-51	CCUA X75
52-54	CCUA X76
55-57	CCUA LSR
58	STATUS
59	Unused
60-61	CCUA CP abend
62-63	CCUA TA
64-75	MCCUB REGS
76	CCUB CMSA
77-79	CCUB X75
80-82	CCUB X76
83-85	CCUB LSR
86	STATUS
87	Unused
88-89	CCUA CP abend
90-91	CCUA TA
92-103	MCAD REGS
104	Map of register value
105	CCU for CA
106	IOC for CA
107	NUM for CA
108-113	Reentry count.
114-120	Count for unexpected interrupt
121	CHGH1CAC return code
122	Unused

NOTE: The fields followed by (1) give information in case of a level 0 re-entry.

Figure 12-21 (Part 1 of 12). MOSS BER Type 01 Formats

Format: foM2

ID: 02	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK
31	ADNO
32	CMD
33	PIRV
34	IOIRV
35	CMSB
36	STAC
37	CAC-RC
38	CA
39-40	STAT0
44-45	STAT1
46-47	STAT4
48-49	Unused
50-53	ADDR
54-65	PCW
66	Flags (ACB)

Format: foM3

ID: 03	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK
31	DEV
32	CMD (log. cmnd)
33	REQ
34	Flag
35	CNT
36	Unused
37	ARC
38-41	ADDR
42-43	BSTAT
44-49	CCB
50-57	BCLE
58-69	SSB
70-77	FILE mod name

Format: foM2b

ID: 02	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK
31	CMD
32-47	NCP MB REQUEST
48-63	NCP MB RESPONSE

Format: foM4

ID: 04	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK
31	CMD
32	BSTAT
33	ASTAT
34-35	CSTAT
36	MSTAT

Format: foM5

ID: 05	
MOSS Check 00 01 02 04 05 08 10 20 40 80 FF	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK
31	ADDR
32-34	X76
35-36	STATUS
37	Adapter ID
38	IOC bus IS

Figure 12-21 (Part 2 of 12). MOSS BER Type 01 Formats

Format: foM5a

ID: 05	
MOSS Check F0	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK: FO
31	ADDR
32-33	DUMP info
34	Unused
35-58	Scanner dump

Format: foM6

ID: 06	
MOSS Check 03 06	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK
31	IPL information
32	CCU Id
33	REQ
34	LVL1 REQ
35	System status
36-37	IPL check code
38-165	LA
166-180	Disk error
181-182	F2
183-185	X71
186-188	X72
189	IPL mode
190-192	CCU configuration
193-216	MIS (Error 06)
217	F1
218-219	RC from CDF
220-315	CA
316-317	IPLCHECK
318	Switch info
319	3746-900

Format: foM7

ID: 06	
MOSS Check 01 02	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK

Format: foM7a

ID: 06	
MOSS Check 04	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK
31	LA address

Format: foM8

IDs: 91 B3 C1 C2

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK
31-32	COMMAND
33-64	MB

Figure 12-21 (Part 3 of 12). MOSS BER Type 01 Formats

Format: foM9

ID: 06	
EXT: 05 07 MOSS Check 05	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK: 05
31	EXTENSION: 05/07
32	CCU (Identifier)
33-34	NCP abend
35	Dump status 0
36	Switch info 0 Sw state not know 1 M-P are connected 2 M-P-S are connect

Format: foM9a

ID: 06	
EXT: 05 MOSS Check 08	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK: 08
31	EXTENSION: 05
32	CCU (ID)
33-35	IAR
36-38	SAR
39-41	LAR
42-44	X70
45-47	X76
48-50	X7D
51-53	X7E
54-55	HDCK

Format: foM10

ID: 06	
MOSS Check 09	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK: 09
31	CCU
32-33	IPL-CHECK(0F1B)
34-36	X71 MSA displ.
37-39	X72 MSA displ.
40-42	IAR
43-45	WKR1
46-48	WKR2
49-51	WKR3
52-54	WKR4
55-57	WKR5
58-60	WKR6
61-63	WKR7
64-65	X7E
66-67	X7D
68-69	X76
70-71	CA XD
72-73	CA XE
74-75	X50
76-77	X51
78-79	X52
80-81	X60
82-145	LA
146	Switch information 0 Sw state not know 1 M-P are connected 2 M-P-S are connect

Format: foM10a

ID: 06	
MOSS Check 07	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK: 07

Format: foM11

ID: 06	
MOSS Check 12	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK: 12
31	REQ
32	Configuration
33	Default
34	Mode
35	From
36	To

Figure 12-21 (Part 4 of 12). MOSS BER Type 01 Formats

Format: foM12

ID: 19

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	Flag (error C)
31-32	Alert indicator
33	Req
34	FCN
35	Serv
	Panel old:
36	Req
37	FCN
38	Serv
39-86	Hexadecimal codes
87-88	CDF RC
89-90	ECB DISC
	MIOC:
91-92	CCUA
93-94	CCUB
	MB CCUA:
95	CMND
96-97	STAT
	MB CCUB
98	CMD
99-100	STAT

Format: foM13

ID: 06

MOSS Check 10 11

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS CHECK=10
31-32	Check code
33	From
34	To
35	Mode
36	Default
37-39	MB into
40-42	SWITCH
43-66	Sense from
67-90	Sense to
91	Status
92-155	LA
156-219	CA
220	Fallback cause

Format: foM14

IDs: 10 11

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30-37	OC1
38-45	OC2 common
46-53	CCUF
54-61	CCUB fields
62-107	IORB
108-115	PLIST for ID 10
108-127	PLIST for ID 11

Format: foM15

IDs: 12 13 14

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30-37	OC1
38-45	OC2
46-53	CCUF
54-61	CCUB
62-77	IORB for ID 14
62-90	IORB for ID 13
62-107	IORB for ID 12

Figure 12-21 (Part 5 of 12). MOSS BER Type 01 Formats

Format: foM16

ID: 08	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	DUMP
31	TRACE
32	CA
33	CCU
34	Unused

Format: foM18

IDs: 16 1A 1B 1C 1D	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30-37	OC1
38-45	OC2
46-53	CCUF
54-61	CCUB
62-77	IORB
82-93	PLIST

Format: foM19

ID: 06	
MOSS Check: 08 EXT: 07	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK
31	EXT
32	CCU
33-34	CP abend code

Format: foM20

IDs: 22 40	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	Status
31	Configuration
32	Default
33	Mode
34	To
35-37	Unused
38-101	LA
102-165	CA
166-167	IPL checking
168-170	MB
171-173	SWITCH
174-197	Sense from
198-221	Sense to
222	Flags

Format: foM21

ID: 20	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-check
31	ORIGI
32	Function
33	SERV
34	CCU
35	STATUS
36	REQ
37	LVL1-REQ
38	Configuration
39	CCU Default
40	3745 mode
41	Switch information

Format: foM22

ID: 85	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
29-xx	1st BER with its own length
xxx-xxx	2nd BER with its own length
xxx-xxx	3rd BER with its own length
	Note: There may be more than three BERs

Figure 12-21 (Part 6 of 12). MOSS BER Type 01 Formats

Format: foM23

ID: 21	
EXT: 01 02 03 04 05	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	Event-ext
31	Status
32	CCU ID
33	Configuration
34	CAC return code
35	CCU default
35	3745 mode

Format: foM24

IDs: 24 to 29, 37	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	CA

Format: foM25

ID: 30	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30-31	FRU GROUP

Format: foM26

ID: 31	
Byte	Meaning
1-27	Header
28-29	Type-ID
30-33	PLIST
34-37	PRB
38-41	SRB
42-45	OP
46-47	ERR
48	DISC
49	DATA
50-51	CMD

Format: foM27

ID: 32	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30-33	PLIST
34-37	PRB
39	DATA
40-41	CMND
42-43	ERR

Format: foM28

ID: 38	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30-31	ERR1
32-33	ERR2

Figure 12-21 (Part 7 of 12). MOSS BER Type 01 Formats

Format: foM29

ID: 07	
ERROR: 04 08 40 80	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	ERROR
31-32	TRA ADDR
33-34	Get CMD complete Lvl 2 err status
35-36	TIC 1 Lvl 2 error status
37-38	TIC 2
39-42	Unused
43-44	MOSS error status
45-46	Lvl 1 error status
47-48	TIC CTL register
49-51	X'76'

Format: foM29a

ID: 07	
ERROR: FE	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	ERROR= FE
31-32	TRA INPUT ADDR
33-34	TRA OUTPUT ADDR
35	TIC NBR
36-37	2K-blk INITIAL
38-39	2K-blk REQUEST
40-41	2K-blk FINAL
42	STOP CMD CNT

Format: foM29b

ID: 07	
EXT: 01 02 03 04 05	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	ERROR
31	ERROR EXT
32	TRA number
33-34	TRA address
35	TIC number
36	CCU

Format: foM30

ID: 15	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30-37	OC1
38-45	OC2
46-53	CCUF
54-61	CCUB
62-77	IORB
78-101	PLIST
102-133	BLK4T

Format: foM30a

ID: 0A	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	Error code (FF)
31	Error extension
32	ELA number
33	ELA error status
34	CCU

Figure 12-21 (Part 8 of 12). MOSS BER Type 01 Formats

Format: foM31

ID: 17

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK
31	BCLE
32	CMD
33	B STAT
34	A STAT
35-38	C STAT
39	M STAT

Format: foM32

ID: 33

EXT: 01 02 03 04 05

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK
31	Unused
36	CCU
37	Abend code
39-62	MIS
63-65	IAR
66-68	SAR
69-71	LAR
72-74	X'70'
75-77	X'76'
78-80	X'7D'
81-83	X'7E'
84-85	CCU hardcheck

Format: foM33

ID: 39

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	IORV
31	PIRV
32-233	Internal buffer
234	Status
235	REQ

Format: foM34

ID: 06

MOSS Check 13

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK
31	CCU
32-35	LOAD MODULE name
36-40	TIMED IPL DATE/TIME
41-45	REFERENCE DATE/TIME

Format: foM35

ID: 06

MOSS Check 14

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS-CHECK
31	CCU
32-35	LOAD MODULE name
36-40	TIMED IPL DATE/TIME
41-45	REFERENCE DATE/TIME
46	MOSS CANCEL ORIGIN

Figure 12-21 (Part 9 of 12). MOSS BER Type 01 Formats

Format: foM36

ID: 1E	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30-37	IOC1
38-45	IOC2
46-53	CCUF
54-61	CCUB
62-85	IORB

Format: foM37

ID: 23	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	CCU
31	PS 3746-900 error

Format: foM38

ID: 2A	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	TA
31	TD
32	CCU
33-36	SLID

Format: foM39

ID: 2B	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	TA
31	TD
32	CCU
33	Origin

Format: foM40

ID: A0	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30-31	Error code
32-34	Panel code
35-37	IML request
38	MOSS/MOSS-E model
39-42	DIAG status

Format: fo41

ID: A1	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	Reason
31-33	Panel code

Format: foM42

ID: A2	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30-32	Old panel code

Figure 12-21 (Part 10 of 12). MOSS BER Type 01 Formats

Format: foM43

ID: A3	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS check
31-34	SLID
35-38	Transaction ID
39	LAN status
40	FRB type in error
41	MOSS check cause
42-50	Previous req. summa
51-54	SSA Cmd header
55-62	Server name
63-66	Current Inst. Addr.
67-137	Received message

Format: foM45

ID: 2C	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30-31	Completion code
32-35	CPN
36	CCU ID
37-60	Reference code

Format: foM46

ID: 2D	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30-31	CCU ID
32	REASON

Format: foM47

ID: 06 MOSS Check: 18	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30-221	LSSD string first part

Format: foM44

ID: A4	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	MOSS check value
31	Reason code
32	Major request code
33	Minor request code
34	Major return code
35	Minor return code
36	Global LAN status
37	LAN manager status
38-39	Open error code
40-41	Ring status
42-43	Link status
44-47	Current Inst. Addr.
48-53	Local adap MAC addr
	DLC counters
54-55	Transmit counter
56-57	Receive counter
58	Transmit error
59	Receive error
60-61	T1 expired
62	Received command
63	Sent command
64	Primary state
65	Secondary state
66	Station VS
67	Station VR
68	Station VA
	MAC counters
69	Line error
70	Internal error
71	Burst errors
72	ARI/FCI error
73	Abort delimiter
74	Unused
75	Lost frame
76	Receive congestion
77	Frame copied error
78	Frequency error
79	Token error
80-82	Unused

Format: foM48

ID: 06 MOSS Check: 28	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30-346	LSSD string second part

Figure 12-21 (Part 11 of 12). MOSS BER Type 01 Formats

Format: foM50

ID: A3	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	IML origine
31-32	Low address
33-34	High address
35	Adapter address

Figure 12-21 (Part 12 of 12). MOSS BER Type 01 Formats

Diagnostics BER Type 03

Diagnostics BER Type 03 - Summary

Table 12-48. BER Type 03 Description

BER Error	ID Description
01	Diagnostic started
02	Diagnostic completed successfully
03	Hardware error detected by diagnostic
04	Microcode error detected in a diagnostic (ABEND type 1 and 2)
05	Microcode error detected in the monitor (ABEND type 3)

Diagnostics BER Type 03 - Detailed BER Display

Diagnostics BER Type 03 - IDs 01 and 02: Format foD1, see page 12-142

```
                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:03 ID:hh
<ERROR DESCRIPTION>                          <REFER.CODE IN CHAR.> CCCCCCCC
 GROUP NBR:hh  IFT/SECT:hhhh  ROUTINE:hh  ADT NBR:hh  LINE NBR:hh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Diagnostics BER Type 03 - ID 03: Format foD2, see page 12-142

```
                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:03 ID:03
<ERROR DESCRIPTION>                          <REFER.CODE IN CHAR.> CCCCCCCC
 ERC:hhhh  RAC:hhhh
 ERROR BIT:hhhh
 ADT NBR:hh  LINE NBR:hh  MUX NBR:hh  CCU ATT:hh
 IFT/SECT:hhhh  ROUTINE:hh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Diagnostics BER Type 03 - IDs 04 and 05: Format foD3, see page 12-142

```
                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:03 ID:hh
<ERROR DESCRIPTION>                          <REFER.CODE IN CHAR.> CCCCCCCC
 RAC:hhhh  ADT NBR:hh  CCU ATT:hh  IFT/SECT:hh  ROUTINE:hh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Note: When running the diagnostics, the BR option generates the diagnostic BERs when a machine error is encountered. To suppress the generation, the

command 'NBR' is used. The default option is BR. For more information see *Service Functions, SY33-2055*.

Diagnostic BERs Type 03 - Formats

Format: foD1

IDs: 01 and 02

Byte	Meaning
1-27	Header
28-29	Type ID
30	Group number
31-32	IFT section-routine
33	Adapter seq. number
34	Adapter line addr.

Format: foD3

IDs: 04 and 05

Byte	Meaning
1-27	Header
28-29	Type ID
30-43	Unused
44-45	RAC
46-61	Unused
62	Adapter seq. number
63-64	Unused
65	CCU attached
66-189	Unused
190	IFT
191	Section
192	Routine number

Format: foD2

IDs: 03

Byte	Meaning
1-27	Header
28-29	Type ID
30-33	Unused
34-35	Error ref. code
36-37	RAC code
38-45	Unused
46-47	Error bit
48-61	Unused
62	Adapter seq. number
63	Line address
64	MUX Id
65	CCU attached
66-189	Unused
190	IFT
191	Section
192	Routine number

Figure 12-22. Diagnostics BER Formats

Power BER Type 04

Power Subsystem BER Type 04 - Summary

BER ID	Description of the event	ALERT	ALARM
00	No reply from channel adapter power block	9D	9D
	No reply from line adapter power block	9F	9F
	No reply from line unit power block	A1	A1
	No reply from CCU power block		90
	No reply from MOSS power block	A8	A8
01	Overcurrent error on CA power block	9D	9D
	Overcurrent error on LA power block	9F	9F
	Overcurrent error on line unit power block	A1	A1
	Overcurrent error on CCU power block		90
	Overcurrent error on MOSS power block	A8	A8
02	Power supply fault on CA power block	9D	9D
	Power supply fault on LA power block	9F	9F
	Power supply fault on line unit power block	A1	A1
	Power supply fault on CCU power block		90
	Power supply fault on MOSS power block	A8	A8
04	MOSS cooling problem	A8	A8
04	Cooling problem (not MOSS)	A7	A7
05	TCM/PUC temperature greater than threshold 1	95	95
06	TCM/PUC temperature under threshold 1	98	98
07	TCM/PUC temperature greater than threshold 2	NO	99
08	MOSS control panel error	08	08
09	Power up of a power block	NO	NO
0A	Power control mode change	NO	NO
0B	Power block powered ON (automatic)	NO	NO
0C	Power block powered OFF (automatic)	See *	See *
0E	Power supply-to-power control error	A2	A2
0F	Battery failure	A5	A5
10	Internal clock down	A6	A6
11	Thermal detector failure	NO	9B
12	AC failure	A3	A3
13	Invalid AC failure	A4	A4
14	Cooling problem corrected	AD	AD
15	Remote power OFF received	NO	NO
16	PLA failure	AC	AC
17	Battery OK. Perform a POS and a MOSS IML	A9	A9
1B	Power block powered ON (manual)	NO	NO
1C	Power block powered OFF (manual)	See *	See *
28	MOSS hardware transient error (dump taken)	02	02
28	End of IML data due to a temporary AC failure	A3	A3
29	End of IML data due to an unexpected event	NO	NO
30	Microcode error BER	AB	AB
31	Set time of day	NO	NO
33	Clean or change air filters	AA	AA
34	Air filters changed	NO	NO
35	Battery changed. Perform a POS and a MOSS IML	NO	A9
36	Change battery	A5	A5

* Alert/Alarm code could be 90, 9D, 9F, A1, or A8.

Figure 12-23. Power Subsystem BER Type 04 Summary

Note: The description of the events does not necessarily match the alarm messages listed in the **Problem Determination Guide,** *SA33-0096*.

Power BER Type 04 - Detailed BER Display

Warning: The BER detail PS ID and AFD ID fields are in **hexadecimal**. Convert to decimal for use in the POS function or to follow MIP directions.

Power BER Type 04 - IDs 00 to 09, 0B to 0E, 10 to 16, and 1B to 1C: Format foP1, see page 12-149.

```
                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:04 ID:hh
<ERROR DESCRIPTION>                          <REFER.CODE IN CHAR.> CCCCCCCC
REQ:hh  RESP:hh  PS ID:hh  AFD ID:hh
PS TYPE:hh  OLD STATUS:bbbb  BUS ID:bbbbbbbb
ADAPTER1:hh  ADAPTER2:hh
RPO:hh  CCU:hh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Power BER Type 04 - ID 0F, 17, 33 to 36: Format foP5, see page 12-149.

```
                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:04 ID:17
<ERROR DESCRIPTION>                          <REFER.CODE IN CHAR.> CCCCCCCC



===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Power BER Type 04 - ID 0A: Format foP1, see page 12-149.

```
                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:04 ID:0A
<ERROR DESCRIPTION>                          <REFER.CODE IN CHAR.> CCCCCCCC
OLD       NEW
bbbbbbbb  bbbbbbbb


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Power BER Type 04 - IDs 28, 29: Format foP2, see page 12-149.

```
                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:04 ID:hh
<ERROR DESCRIPTION>                          <REFER.CODE IN CHAR.> CCCCCCCC
IML SOURCE:hh  CAUSE:hh REASON:hh
CONTROL MODE:hh  INSTAL TYPE:hh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Power BER Type 04 - ID 30: Format foP3, see page 12-149.

```
                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:04 ID:30
<ERROR DESCRIPTION>                          <REFER.CODE IN CHAR.> CCCCCCCC

IOIRV:hh PIRV:hh  REQ:hh  RESP:hh
ERR:hh  ECB:hhhh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Power BER Type 04 - ID 31: Format foP4, see page 12-149.

```
                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:04 ID:31
<ERROR DESCRIPTION>                     <REFER.CODE IN CHAR.> CCCCCCCC
 DATE:hh / hh / hh
 DAY :hh
 TIME:hh : hh : hh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Power BER Type 04 - Field Description

Table 12-49. Power BER type 04 Field Description

Field name	Meaning	Refer to
Adapter1	Affected adapter number (in hexadecimal)	-
Adapter2	Affected adapter number (in hexadecimal)	-
AFD	Air flow detector id (blower id)	page 10-64
BUS ID	Bus identifier	page 10-40
CCU	Value is 00, except in case of case of RPO: hh = 01 for CCUA, hh = 02 for CCUB	
Control Mode	See OLD and NEW	Chapter 10
DAY	Day of the week	page 12-146
ECB	Event control block	(*)
ERR	Microcode error	page 12-146
IML/IPL	Source of IML/IPL Cause of IML/IPL Reason of power OFF	page 12-146 page 12-146 page 12-146
Install-Type	MPW power logic card state	" "
IOIRV	I/O interrupt request vector	page 8-14
LAR	Lagging address registers (input X'74')	page 2-44
NEW	New panel info (01=host, 02=network, 03=local)	
OLD	Old panel info (01=host, 02=network, 03=local)	
PIRV	Program interrupt request vector	page 8-14
PS ID	Power supply ID	page 10-6
PS Type	Power supply type	page 10-6
REQ	See request description	page 12-147
RESP	PLC response to MOSS	page 12-148
RPO	Request power OFF	page 12-146

(*) For software information on BERs originated by NCP/PEP, refer to the associated product documentation.

Power BER Type 04 - Field Details

Some of the following fields may not appear on the BER detail display, but they are part of the BER and they are listed as they appear in the BER file.
See the section 'BER Formats on Disk' page 12-128

Table 12-50. BER 04 Field Details

Field Name	Field Value	Meaning
DAY	01 02 03 04 05 06 07	Sunday Monday Tuesday Wednesday Thursday Friday Saturday
IPL/IML Source	01 02 03 04 05 06 07	Host requested IPL Auto restart Remote IPL Request from panel Request from console Scheduled power ON Auto restart after emergency power OFF
IPL/IML Cause	01 02 03 04	MOSS IML General IPL Retry on MOSS PS fault MOSS check
Microcode error	01 02 03 04 05 06	Invalid response Request expected Response expected Invalid interrupt Invalid asynchronous event Invalid TCM/PUC error reporting
REASON	 01 02 03 04 05	Last power OFF reason Power OFF from host in host mode (power hold signal inactive) AC failure Remote power OFF in network mode Power OFF from panel in local mode Power OFF from the EPO switch
RPO	01 02 03	General power OFF Remote power OFF request Requested power OFF failed
Install Type	00 01 02 03	Normal state First installation Hot replacement Cold replacement
PS OLD/NEW status	bbbb (binary) 0001 0010 0011 0100 0101 1000 1001 1010	 Unused Up status Down status No reply Thermal fault OC fault PS fault Interface failure

RESP and REQ fields: **RESP** field meaning depends on the associated **REQ** field value.

A REQ value corresponds to 2 possible RESP:

- OK response
- KO response

according to the following table:

Note: The **REQUEST** code is valid only when the BER is issued after a MOSS request to the power control.

Table 12-51. BER 04 REQ/RESP Table

REQ	RESP OK	RESP KO	Meaning
01	42	C2	Start diskette
02	43	C3	Stop diskette
03	44	C4	Power ON a power block
04	45	C5	Power OFF a power block
05	N/A	N/A	MPWL reset
06	N/A	N/A	General power OFF
07	48	C8	Start disk
08	49	C9	Stop disk
09	4A	CA	Set adapter
0A	4B	CB	Reset adapter
0B	4D	N/A	Manufacturing power OFF
0C	4E	N/A	Check MPWL
0D	50	N/A	Get end of IML data
0E	51	N/A	Get stacked error record
0F	52	N/A	Create configuration table
10	53	N/A	Acknowledge configuration table
11	54	D4	Sense power block
12	55	N/A	Set time of day
13	56	D6	Get time of day
14	57	N/A	Set scheduled power ON
15	58	N/A	Get scheduled power ON
16	59	N/A	Allow scheduling
17	5A	N/A	Inhibit scheduling
18	N/A	N/A	Allow remote finger
19	N/A	N/A	Inhibit remote finger
1A	N/A	N/A	Signal logon
1B	5E	N/A	Get scheduling state
1C	N/A	N/A	MOSS IML from disk
1D	N/A	N/A	General IPL from disk
1E	N/A	N/A	Send time of day to MPWL
1F	70	F0	Display message indicator on panel
20	76	F6	Display console in use
21	7E	FE	Display hexadecimal code on panel
22	7F	FF	Display function code

If the BER is issued from an error reported to the MOSS by the power control:

- The **REQUEST** field is set to 00.
- The **RESP** field takes the meaning given in the following table:

Table 12-52. BER 04 RESP Table When REQ = 00

RESP	Meaning
00	Unused
01	Unused
02	Power block up
03	Power block down
04	No reply from power block
05	Thermal fault
06	Air flow fault
07	TCM/PUC greater than threshold 1
08	Overcurrent fault
09	PS fault
0A	TCM/PUC under threshold 1
0B	TCM/PUC greater than threshold 2
0C	Interface KO
0D	Local request
0E	Force local
0F	Battery KO
10	TCM/PUC KO
11	Power control mode change
12	Panel KO
13	AC failure
14	Invalid AC failure
15	MPWA KO
16	Remote power OFF
17	Air flow detector OK
18	Battery OK

Power BER Type 04 - Formats

Format foP1

@Ds:00-09, 0B-0E, 10-16, 1B-1C	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	REQ
31	RESP
32	PS ID
33	AFD
34	Retry indicator
35	PS type
36 bbbb bbbb	Old Status Address
37	BUS ID
38	Adapter 1
39	Adapter 2
40	RPO
41	CCU
ID: 0A only	
42	Old control
43	New control
44	Tower ID for airflow fault

Format foP2

IDs: 28 29	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	IML source
31	CAUSE
32	POWER OFF reason
33	CTRL Mode
34-173	PCT
174-180	TOD
181	Install Type
182-213	AFD status
214-217	Airflow fault on each tower

Format foP4

ID: 31	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30-32	Time (SS, MM, HH) in Hex
33	Day of week
34-36	Date (day, month, year)

Format foP3

ID: 30	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	IORV
31	PIRV
32	REQ
33	RESP
34	ERR CODE
35-37	Unused
38-41	MPNL data
42-43	ECB

Format foP5

ID: 0F, 17, 33-36	
Byte	Meaning
1-27	Header
28-29	TYPE-ID

Figure 12-24. Power BER Formats

NCP ESS BER Type 08

ESS BER Type 08 - Summary

Table 12-53 (Page 1 of 4). ESS BER Type 08 Summary

BER ID	Abend Code (NCP)	Event Description	Recovery or Action	ALERT	ALARM
14	0930	ELAyy AIO Address Exception Check IOC error LVL1 with: LVL1 summary register X7E = '0100' (IOC-1) or '0001' (IOC-2) with IOC LVL1 register X76 = '8200' (IOC-1) or '0082' (IOC-2)	NCP re-IPL	No	E1
16	0931	ELAyy AIO Storage Protect Check IOC Error LVL1 with: LVL1 Summary Register X7E = '0100' (IOC-1) or '0001' (IOC-2) with IOC LVL1 Register X76 = '4200' (IOC-1) or '0042' (IOC-2)	NCP re-IPL	No	E1
18		ELAyy IOH/IOHI to Adapter not attached IOC Error LVL1 with: LVL1 Summary Register X7E = '0100' (IOC-1) or '0001' (IOC-2) with IOC LVL1 Register X76 = '2800' (IOC-1) or '0028' (IOC-2) For adapter address in TA, the CDS shows the adapter not attached.	None	30	30
1B	0933	ELAyy Invalid Input IOH IOC Error LVL1 with: LVL1 Summary Register X7E = '0100' (IOC-1) or '0001' (IOC-2) with IOC LVL1 Register X76 = '5800' (IOC-1) or '0058' (IOC-2) LAS (line adapter status) bit 1.7 is On.	NCP re-IPL	No	E1
1C		ELAyy Portx Command Rejected by Adapter Microcode Adapter LVL1 with: LVL1 Summary Register X7E = '2000' (IOC-1) or '0200' (IOC-2) with Adapter Status Register (Error Status Type 3 non-Hardstop) or LAS = B'1000 00u0 10xx xxxz' as command reject on line interface address = b'xxxxxz' where 'x..x' reflects the relative line address and 'z' gives the interface side (Xmit or Rcv). When 'u' = 1 this indicates a command reject for command-on-command.	Port down	31	31
1E		ELAyy Invalid Output IOH to Adapter Adapter LVL1 with: LVL1 Summary Register X7E = '2000' (IOC-1) or '0200' (IOC-2) with Adapter Status Register (Error Status Type 3 non-Hardstop) or LAS = B'1000 000u 0100 0000' as Invalid Output IOH for which the related PIO terminated correctly (no IOC error LVL1) but the adapter microcode rejects the Output IOH by raising this current adapter LVL1. 'u' = '1' means adapter disconnected due to NCP command 'F2'.	ELA down	32	32
26		ELAyy Portx SCTL/DMA Storage Protect or Address Exception Adapter LVL2 with: PSA LCS (Line Control Status) = 'DC' as any DMA type error PSA HELCS (High byte of Extended LCS) = '10' as specifically SP/AE	ELA port down	37	37

Table 12-53 (Page 2 of 4). ESS BER Type 08 Summary

BER ID	Abend Code (NCP)	Event Description	Recovery or Action	ALERT	ALARM
91		ELAyy AIO Error IOC Error LVL1 with: LVL1 Summary Register X7E = '0100' (IOC-1) or '0001' (IOC-2) with IOC LVL1 Register X76 = 'uV00' (IOC-1) or '00uV' (IOC-2) with AIO CCW Register X75H or X75L = B'1nnn n000' where nnnn from 0 to 15 represents the IOC relative adapter number, adapter which was performing the AIO, AIO (Adapter Initiated Operation / Cycle Steal) failing in Time-Out (V='A') or in Bus-In parity Check (V='6') with 'u' giving the time when the operation failed (refer to page 2-37).	ELA μ code retry	No	No
91		ELAyy AIO Error (threshold) Adapter Down flag is on.	ELA down	34	34
92		ELAyy Unresolved AIO Error IOC Error LVL1 with: LVL1 Summary Register X7E = '0100' (IOC-1) or '0001' (IOC-2) with IOC LVL1 Register X76 = 'uV00' (IOC-1) or '00uV' (IOC-2) with AIO CCW Register X75H or X75L = B'1nnn n000' where nnnn from 0 to 15 represents the IOC relative adapter number, adapter which was performing the AIO, but as opposed to previous BER 08 91, V='2' only (not 'A' or '6').	ELA μ code retry	No	No
92		ELAyy Unresolved AIO Error (threshold) Adapter Down flag is On	ELA down	34	34
93		ELAyy AIO Invalid CSCW IOC Error LVL1 with: LVL1 Summary Register X7E = '0100' (IOC-1) or '0001' (IOC-2) with IOC LVL1 Register X76 = '2200' (IOC-1) or '0022' (IOC-2) AIO CCW register X75H or X75L = B'1nnn n000' where nnnn from 0 to 15 represents the IOC relative adapter number, adapter which was performing the AIO.	ELA μ code retry	No	No
93		ELAyy AIO Invalid CSCW (threshold) Adapter Down flag is On	ELA down	38	38
94		ELAyy Portx Cycle Steal Error on Set Mode Adapter LVL1 with: LVL1 Summary Register X7E = '2000' (IOC-1) or '0200' (IOC-2) Adapter Status Register (Error Status Type 3 non-Hardstop) or LAS = B'1000 0000 10xx xxxz' (almost identical to BER 08 1C as Command Reject on line interface address 'xxxxxz') but NCP looks at the SLI bit in the LNVT: if ON (Set LNVT Initial required) and if adapter command-reject status = '10xx xxxx xxxx xxxx' then NCP will generate this BER 08 94 instead of BER 08 1C.	Port down	3C	3C
95		ELAyy Adapter LVL1 Hardcheck Adapter LVL1 with: LVL1 Summary Register X7E = '2000' (IOC-1) or '0200' (IOC-2) with Adapter Status Register (Error Status Type 3 Hardstop) or LAS = B'0000 0uuu uuuu uu00' where the string 'uu..uu' reflects the hardware checkers which have been raised (u=1), as several can occur simultaneously in some cases of failure (refer to page 4-201).	ELA down	34	34
96		ELAyy Adapter Disconnected by operator Adapter LVL1 with: LVL1 Summary Register X7E = '2000' (IOC-1) or '0200' (IOC-2) with Adapter Status Register (Error Status Type 3 non-Hardstop) or LAS = B'1000 0001 0000 0000', meaning "adapter put in disconnect mode" on MOSS operator's request.	ELA Off line	3D	3D

Table 12-53 (Page 3 of 4). ESS BER Type 08 Summary

BER ID	Abend Code (NCP)	Event Description	Recovery or Action	ALERT	ALARM
97		ELAyy PIO Error IOC Error LVL1 with: LVL1 Summary Register X7E = '0100' (IOC-1) or '0001' (IOC-2) with IOC LVL1 Register X76 = 'uV00' (IOC-1) or '00uV' (IOC-2) as PIO (Program Initiated Operation) failing in Time-Out (V='8') or in Bus-In parity Check (V='4') with 'u' giving the time when the operation failed (refer to page 2-37).	NCP retry	No	No
98		ELAyy PIO Error (threshold) IOC Error LVL1 with: Identical to BER 08 97 but on last IOH/PIO retry.	ELA down	34	34
99		ELAyy Adapter LVL1 non-Hardcheck Adapter LVL1 with: LVL1 Summary Register X7E = '2000' (IOC-1) or '0200' (IOC-2) with Adapter Status Register (Error Status Type 3 non-Hardstop) or LAS = B'1iii 0uu0 0000 000v' where 'iii' (invalid interrupt level from 0 to 7) and 'u' are checkers raised by Mcode and 'v' by hardware (refer to page 4-200).	ELA down	32, 34, or 38	32, 34, or 38
9B		ELAyy LVL1 Interrupt from disconnected ELA	NCP retry	No	No
9B	093A	ELAyy LVL1 Interrupt from disconnected ELA (threshold)	NCP re-IPL	No	E3
9C		ELAyy PIO Error on Get Line ID (GLID) and PIO get error status (GES) to adapter shows LAS bit 1.0 On (TA time select).	NCP retry	No	No
9C		ELAyy PIO Error on GLID (threshold)	ELA down	34	34
9D		ELAyy Adapter Microcode detected error Adapter LVL1 with: LVL1 Summary Register X7E = '2000' (IOC-1) or '0200' (IOC-2) with Adapter Status Register (Error Status Type 3 non-Hardstop) or LAS = '8800' (Microcode Check). then NCP reads the adapter Mcode Check (TA1 = '31') which gives the CSECT and checker number. This last data overwrites the previous LAS contents which is then not seen in BER display.	ELA down	38	38
9E		ELAyy PIO Get Error Status failed IOC Error (X76 not 0) in LVL1 Identical to BER 08 97/98 but on IOH/PIO for Adapter Get Error Status either after an Adapter LVL1 or after an Adapter LVL2 leading to an IOH/PIO Get Line ID failure (IOC error LVL1).	ELA down	34	34
A1		ELAyy Portx Unexpected Interrupt LVL2 The BER is generated when Get Line ID data is invalid (not in the allowed range) or points on a line that is considered as not installed and therefore not SYSGENed in NCP, or points on a SYSGENed line but the line is not active from NCP view point.	NCP retry	No	No
A1	0936	ELAyy Portx Unexpected Interrupt LVL2 (threshold)	NCP re-IPL	No	E2
A2		ELAyy Portx Adapter Internal or Attachment Error Hardware error reported via LVL2 LCS = 'C0', 'C4', 'C6', 'C8', 'C9', 'CA', 'CE', 'D0', 'D6', 'D8', 'DA'.	Port down	3C	3C
A2		ELAyy Portx Adapter Internal or Attachment Error CP error reported via LVL2 LCS = 'D4', 'D2'.	Port down	31	31

Table 12-53 (Page 4 of 4). ESS BER Type 08 Summary

BER ID	Abend Code (NCP)	Event Description	Recovery or Action	ALERT	ALARM
A2		ELAyy Portx Adapter Internal or Attachment Error Environment error reported via LVL2 LCS = 'CB', 'DE', 'DF'.	Port down	3F	3F
A4		ELAyy Portx Time-Out on command except F5	Port down	No	No
A6		ELAyy Portx SCTL/DMA internal Error Adapter LVL2 PSA LCS (Line Control Status) = 'DC' (SCTL/DMA/SWDM error) and PSA HELCS (High byte of extended LCS = '02', '12', '22').	Port down	3C	3C
A7		ELAyy Portx DMSW/SCTL DMA Interface error Adapter LVL2 PSA LCS (Line Control Status) = 'DC' (SCTL/DMA/SWDM error) and PSA HELCS (High byte of extended LCS = '04', '14', '24', '34', '44').	Port down	3C	3C
A8		ELAyy Portx DMSW DMA reported error Adapter LVL2 PSA LCS (Line Control Status) = 'DC' (SCTL/DMA/SWDM error) and PSA HELCS (High byte of extended LCS = '06', '16').	port down	3C	3C
A9		ELAyy Portx DMSW DMA Parity Check or Time-Out Adapter LVL2 PSA LCS (Line Control Status) = 'DC' (SCTL/DMA/SWDM error) and PSA HELCS (High byte of extended LCS = '08', '18', '28').	Port down	3C	3C
AA		ELAyy Portx EAC DMA Interface Error Adapter LVL2 PSA LCS (Line Control Status) = 'DC' (SCTL/DMA/SWDM error) and PSA HELCS = '0A', '1A', '2A', '3A', '4A', '5A', '6A', '7A', '9A', 'AA', 'BA'.	Port down	3C	3C
B1		ELAyy Portx Time-Out on command F5	Port down	3E	3E
B7		ESS link error not caused by controller hardware. BER information only.		No	No

Note: In case of abend, anNCP re-IPL is performed and an Alarm/Alert is generated when IPL is completed. This alert is triggered by MOSS BER 01 ID 06, error code 05.

ESS BER Type 08 - Detailed BER Display

ESS BER Type 08 - ID 14, 16, 91, 92, 93: Format foE1, see page 12-160. Program level 1 generates one of the following BERs when an error occurs during an AIO operation on a scanner.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:08 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                             <REF. CODE IN CHAR.> CCCCCCCC

F:bbbbbbbb
X7E:hhhh  X76:hhhh  X75:hhhh  ETA:hhhh  LAS:hhhh  X76U:hhhh  SPR:hhhhhhhh
SWA:hhhh  LAR:hhhhhhhh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

ESS BER Type 08 - IDs 18, 1B, 97, 98, 9C, 9E: Format foE2, see page 12-160. Program level 1 generates one of these BERs when an error occurs during a PIO operation on a scanner.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:08 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                             <REF. CODE IN CHAR.> CCCCCCCC

F:bbbbbbbb X7E:hhhh X76:hhhh I:hhhh LAR:hhhhhhhh
LAS:hhhh X76U:hhhh ETA:hhhh SWA:hhhh IAR:hhhhhh TA:hhhhh TD:hhhh
IOB/LXB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
        hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
CCB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
    hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
AXB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhh hh
SCB:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hh
PSA:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

ESS BER Type 08 - IDs 1E, 95, 96, 99, 9B, 9D: Format foE3, see page 12-160. Program level 1 generates one of these BERs when an error is reported by a scanner on level 1.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:08 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                           <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
X7E:hhhh X76:hhhh ADNO:hh LAS:hhhh X76U:hhhh SWA:hhhh LAR:hhhhhhhh



===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

ESS BER Type 08 - ID A1: Format foE4, see page 12-161. These BERs are generated on a LVL2 unresolved interrupt.

```
                              ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:08 ID:hh<LOST:ddd CP-ABEND:hhhh>
<Error description>                          <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
TA:hh  TD:hh  NW:hhhh  IDR:hhhh  LNVT:hhhhhhhh  LCS:hh
PSA:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
CNT:hhhh

OVERRIDE FLAG WITH NEW HEXADECIMAL VALUE
===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

ESS BER Type 08 - ID B1: Format foE5, see page 12-161. These BERs are generated on a LVL2 time out.

```
                              ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:08 ID:hh<LOST:ddd CP-ABEND:hhhh>
<Error description>                          <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
TA:hh  TD:hh  NW:hhhh
PSA:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh

OVERRIDE FLAG WITH NEW HEXADECIMAL VALUE
===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

ESS BER Type 08 ID 26, A2, A3, A4, A5, A6, A7, A8, A9, AA: Format foE5, see page 12-161. Program level 2 generates one of these BERs when a scanner internal error or a transient line error is detected.

```
                               ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:08 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                          <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb TA:hh TD:hh NW:hhhh IDR:hhhh
PSA:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
IOB/LXB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
        hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
CCB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
    hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
AXB:hhhh hhhh hhhh hhhh hhhh hhhh hhhh
SAT:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hh
SCB:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hh
CSC:hhhh CNT:hhhh

===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Note: Lost and CP abend fields are displayed when applicable.

ESS BER Type 08 ID 94, 1C: Format foE6, see page 12-161. Program level 1 generates this BER when a command reject is reported by a scanner on level 1 (control program error).

```
                                ELD DETAIL
 SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:08 ID:hh<LOST:ddd CP-ABEND:hhhh>
 <ERROR DESCRIPTION>                          <REFER.CODE IN CHAR.> CCCCCCCC
 F:bbbbbbbb LNVT:hhhh PSA:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
 SCF:hh LSTAT:hh LAS:hhhh CR1:hh CR2:hh IAR:hhhhhhhh TA:hh TD:hh
 IOB/LXB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
         hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
 CCB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
     hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
 AXB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhh  hh
 SCB:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

ESS BER Type 08 - ID B7: Format foE7, see page 12-161. Program level 3 generates the following BERs when an external ESS physical link error occurs.

```
                                ELD DETAIL
 SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:08 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                                  CCCCCCC
 TA BYTE0:hh  TD BYTE1:hh  BFLAG:hhhh  TDREFLECT:hhhh
 XMTTOT:hhhh hhhh  RCVTOT:hhhh hhhh  XMTERR:hhhh hhhh  RCVERR:hhhh hhhh
 EXCSCLSN:hhhh hhhh  LATECSLN:hhhh hhhh  RCVCNGST:hhhh hhhh  CRCERR:hhhh hhhh
 FRAMERR:hhhh hhhh  RSIZERR:hhhh hhhh  XMTDEF:hhhh hhhh  ONECLSN:hhhh hhhh
 MULTCLSN:hhhh hhhh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

BFLAG BER flag:
- 40 = RCVERR reached its threshold.
- 80 = XMTERR reached its threshold.

TDREFLECT Time Domain Reflectometry is a measure of the distance from a 3745 Ethernet adapter attachment to the point on the Ethernet where there is a fault that is causing signals to be reflected. The 3745 Ethernet adapter sees this condition as a cause of an Excess Collision Error. Whenever Excess Collision Errors Occur, a value will be stored for Time Domain Reflectometry. If no Excess Collision Errors have occurred during the interval for a counter report, this value will be zero. Unlike other counter values, this value only has 10 bits of valid data.

XMTTOT The Transmit Total Counter includes frames transmitted successfully and frames lost during transmission.

RCVTOT The Receive Total Counter includes frames received successfully and receive frames that were lost.

XMTERR The Transmit Error Counter includes all transmit frames lost. This count includes EXCSCLSN and LATECLSN.

RCVERR The Receive Error Counter includes all receive frames that were lost. This count includes RCVCNGST, CRCERR, FRAMERR, and RSIZERR.

EXCSCLSN Excess Collision Errors occur when 16 attempts to transmit a frame fail because collisions are detected on the Ethernet.

LATECLSN A Late Collision Error occurs when a transmit frame is lost because of a collision that takes place after the maximum time that should be required to detect a collision. In this case, the transmitter of the other frame should have been aware of the 3745 frame when it listened for the presence of carrier before beginning its transmission.

RCVCNGST A receive Congestion Error occurs when the 3745 adapter is unable to receive a frame because its buffers are filled.

CRCERR A CRC Error occurs when a receive frame is discarded because a problem was detected with the cyclic redundancy check.

FRAMERR A Framing Error occurs when a receive frame does not end on a byte boundary.

RSIZERR A Receive Size Error occurs when a receive frame is longer than the Ethernet allowed maximum frame size of 1518 bytes.

XMTDEF The Transmit Deferred Counter includes the number of frames for which the initial transmission of the frame was deferred because carrier was sensed on the Ethernet.

ONECLSN The One Collision Counter includes the number of times that there was one collision before a frame was transmitted successfully.

MULTCLSN The Multiple Collision Counter includes the number of times that there was more than one collision before a frame was transmitted successfully.

ESS BER Type 08 - ID B7 Triggering Condition

NCP will generate this BER when either:

1. The transmit error threshold (XMTERR) or
2. The receive error threshold (RCVERR) is reached.

XMTERR hits come from:

1. Excess collision errors (EXCSCLSN) or
2. Late collision errors (LATECLSN).

RCVERR hits come from:

1. Receive congestion errors (RCVCNGST) or
2. CRC errors (CRCERR) or
3. Framing error (FRAMERR) or
4. Receive size error (RSIZERR).

ESS BER Type 08 - Field Description

Table 12-54 (Page 1 of 2). ESS BER Type 08 Field Description

Field Name	Meaning	Refer to
ADNO	ELA number (decimal) in error description field.	
LAS or L-STAT	Line adapter status refleting: • LA Error Status Type 1 (AIO error) • LA Error Status Type 2 (PIO error) • LA Error Status Type 3 (adapter LVL1)	page 4-198
ETA	TA field of IOH failure in level 1.	page 14-24
IDR	Get line ID response.	Chapter 4
F	Indicator flag (indicates a byte expansion follows)	(*)
SWA	Switch adapter error register.	page 3-23
CR1	First command sent to scanner	
CR2	Second command sent to scanner	
LAR	Lagging address register	page 2-44
SPR	LA shared pointer register X'3F' or X'6F'.	
CSC	Configuration status control flag (contains X'FFFF' for PEP, BSC/SS and BNN lines).	
CNT	Repetition count (BER flooding). Number of times the BER appeared.	
SCF	Secondary Control Field.	
I	First two bytes of instruction.	
IAR	IAR of interrupt level.	
LCS	Line communication status.	page 14-26
PORTnn	Port number (1 or 2) within the ELA (in error description line).	
LNVT	Line vector table.	page 4-101
LOST	Lost record count (LRC).	(*)
NW	Network address (NCP)	(*)
IOB/LXB	X'24' bytes of LXB (for SDLC lines) or IOB (for BSC/SS lines) control blocks. This area is padded with X'FF' for PEP.	(*)
CCB	X'40' bytes of data from the CCB control block. • If PEP, the fields are CCBL2 through CCBPOLL inclusive. • If PEP, the fields are CCBTROPT through CCBXPTR inclusive.	(*)
AXB ACB TRACE	X'E' bytes of data from the AXB control block from AXBFCTL through AXB+X'15' (ACB trace area). For PEP, this area contains the CCB extension starting at the PEP CCB + X'60'.	(*)
AXB PSA	X'11' bytes of data from the PSA trace area of the AXB control block (AXBASSCF through AXBTROFF). For PEP, this area contains the remaining portion of the CCB extension padded with X'F'.	(*)
SCB	X'19' bytes of the SCB/CUB from SCBSSCF (CUBSSCF) through SCBRTCNT (CUBRTCNT) inclusively. For BSC/SS lines and for PEP, this area is padded with X'FF's.	(*)
SAT	17 bytes of PSA trace area for NCP. For PEP, this area contains the EP CCB extension.	(*)
SCBCSCF	Configuration station control flags (NCP only).	(*)
PSA	Parameter area (16 bytes)-status area (12 bytes). The byte contents of the PSA depend on the current command (CCMD).	(*)
TA	IOH/IOHI image (TA: hh means TA data byte 0) (see CSn and PORTnn).	page 14-24
TD	IOH/IOHI image -- TD data adapter specific bytes (TD: hh means TD data byte 1).	page 14-24
X3F	CSP shared pointer register.	page 2-24

Table 12-54 (Page 2 of 2). ESS BER Type 08 Field Description

Field Name	Meaning	Refer to
X74	X'74' - LAR bytes (See CSn and PORTnn).	page 2-31
X75	X'75' - Cycle steal control word register.	page 2-31
X76	X'76' - IOC error summary register.	page 2-31
X76U	X'76' - Cause of error not found (PIO to read error register failed).	page 2-31
X79	X'79' - Interrupt level.	page 2-31
X7E	X'7E' - CCU level 1 interrupt.	page 2-31
X7F	X'7F' - Interrupt request register CCU levels 2, 3, and 4	page 2-31

Note: All values are in hexadecimal notation (X'0' to X'F'), except for:

- Flag bytes F and CS STAT, which are in bit format (8 or 16 bits, 0 or 1)
- The error description line with a CS number and LINE number, which are in decimal notation.

(*) For software information on BERs originated by NCP/PEP, refer to the associated product documentation.

ESS BER Type 08 - Formats

Format: foE1

ID: 14 16 91 92 93	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35-36	X76
37-38	X75
39-40	Unused
41-42	ETA
43-44	LAS
45-46	X76U
47-50	SPR
51	Flag
52	Unused
53-54	SWA
55-58	LAR

Format: foE2

IDs: 18 1B 97 98 9C 9E	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35-36	X76
37-38	I
39-42	LAR
43-44	LAS
45-46	X76U
47-48	ETA
49-50	Unused
51	Flag
52	Unused
53-54	SWA
55	INTLVL
56-58	IAR
59-60	TA
61-62	TD
63-66	Unused
67-102	IOB/LXB
103-166	CCB
167-198	AXB
199-215	SCB
216	Unused
217-244	PSA

Format: foE3

ID: 1E 95 96 99 9A 9B 9D	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35-36	X76
37	ADNO
38-42	Unused
43-44	LAS
45-46	X76U
47-50	Unused
51	F
52	TSS Flag
53-54	SWA
55-58	LAR
59-66	Unused
67-102	LBX
103-166	CCB
167-182	ATT
183-198	PSA Trace

Figure 12-25 (Part 1 of 2). ESS BER Formats

Format: foE4

ID: A1

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33	F
34	Unused
35-36	IDR
37-64	PSA (56 = LCS)
65	TA byte 0
66	TD byte 1
67-68	NW
69-72	LNVT
73-108	IOB/LXB
109-172	CCB
173-186	AXB trace
187-203	SAT trace
204-219	SCB
220	SCBCSCF
221-222	Count

Format: foE5

IDs: 26 A2 A3 A4 A5 A6 A7 A8 A9 AA AB B1

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33	Flag
34	Unused
35-36	IDR
37-64	PSA
65	TA byte 0
66	TD byte 1
67-68	NW
69-104	IOB/LXB
105-168	CCB
169-182	AXB (IOB)
183-199	SAT trace
200-215	SCB
216	CSC
217-218	Count (Only for A2, A4, and AB)

Format: foE6

ID: 94 1C

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33	F
34	Interrupt level 1
35-36	LNVT
37-52	PSA
53	SCF
54	LSTAT
55-56	LAS
57	CR1
58	CR2
59-62	IAR
63-64	Unused
65	TA
66	TD
67-102	LXB/IOB
103-166	CCB
167-197	AXB
198	Unused
199-215	SCB
216	Unused

Format: foE7

ID: B7

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33	TA Byte 0
34	TD Byte 1
35-36	BFLAG
37-38	TDREFLECT
39-42	XMTTOT
43-46	RCVTOT
47-50	XMTERR
51-54	RCVERR
55-58	EXCSCLSN
59-62	LATECLSN
63-66	RCVCNGST
67-70	CRCERR
71-74	FRAMERR
75-78	RSIZERR
79-82	XMTDEF
83-86	ONECLSN
87-90	MULTCLSN

Figure 12-25 (Part 2 of 2). ESS BER Formats

NCP 3746 Model 900 BER Type 9

3746 Model 900 BER Type 9 - Summary

Table 12-55 (Page 1 of 4). 3746 Model 900 BER Type 9 Summary

BER ID	Abend Code (NCP)	Event Description	Recovery or PGM Action	MOSS ALERT	ALARM
10		Cmd Reject-No prior Set vvvv vvvv stands for LNVT, ALNVT, or TLNVT X7E='2000' (IOC-1 with CBA-1) or '0200' (IOC-2 with CBA-2) CBA LVL1 with first GES = X'2802', second GES = IOH TA, third GES = IOH TD	CSS Adapter down	EC	EC
11		Cmd Reject-Set vvvv Out of Sequence vvvv stands for LNVT, ALNVT, or TLNVT X7E='2000' (IOC-1 with CBA-1) or '0200' (IOC-2 with CBA-2) CBA LVL1 with first GES = X'2902', second GES = IOH TA, third GES = IOH TD	CSS Adapter down	EC	EC
12		Cmd Reject-Set CDF/E Out of Sequence X7E='2000' (IOC-1 with CBA-1) or '0200' (IOC-2 with CBA-2) CBA LVL1 with first GES = X'2A02', second GES = IOH TA, third GES = IOH TD	CBA down	E4	E4
13		Cmd Reject-Invalid Adapter Address X7E='2000' (IOC-1 with CBA-1) or '0200' (IOC-2 with CBA-2) CBA LVL1 with first GES = X'2302', second GES = IOH TA, third GES = IOH TD	None	EB	EB
14		Cmd Reject-Invalid Line Address X7E='2000' (IOC-1 with CBA-1) or '0200' (IOC-2 with CBA-2) CBA LVL1 with first GES = X'2402', second GES = IOH TA, third GES = IOH TD	None	F1	F1
15		Cmd Reject-No prior Start Line Initial X7E='2000' (IOC-1 with CBA-1) or '0200' (IOC-2 with CBA-2) CBA LVL1 with first GES = X'2502', second GES = IOH TA, third GES = IOH TD	Line down	No but NCP alert	F2
16		Cmd Reject-Xmit Command on Command X7E='2000' (IOC-1 with CBA-1) or '0200' (IOC-2 with CBA-2) CBA LVL1 with first GES = X'2602', second GES = IOH TA, third GES = IOH TD	Line down	No but NCP alert	F2
17		Cmd Reject-Rcv command when no LVL2 X7E='2000' (IOC-1 with CBA-1) or '0200' (IOC-2 with CBA-2) CBA LVL1 with first GES = X'2702', second GES = IOH TA, third GES = IOH TD	Line down	No but NCP alert	F2

Table 12-55 (Page 2 of 4). 3746 Model 900 BER Type 9 Summary

BER ID	Abend Code (NCP)	Event Description	Recovery or PGM Action	MOSS ALERT	ALARM
18		Cmd Reject-Adapter not installed X7E='2000' (IOC-1 with CBA-1) or '0200' (IOC-2 with CBA-2) CBA LVL1 with first GES = X'2102', second GES = IOH TA, third GES = IOH TD	None	No but NCP alert	E9
19		Cmd Reject-Adapter Inoperative X7E='2000' (IOC-1 with CBA-1) or '0200' (IOC-2 with CBA-2) CBA LVL1 with first GES = X'2202', second GES = IOH TA, third GES = IOH TD	None	No but NCP alert	EA
1B	0933	PIO Error-Invalid Input IOH IOC Error LVL1 on IOH/PIO	NCP abend	No	E1
1D		DMA SP/AE during LNVT Read for a given CSS adapter X7E='2000' (IOC-1 with CBA-1) or '0200' (IOC-2 with CBA-2) CBA LVL1 with first GES = X'3503', second GES = IOH TA, third GES = SLID bytes 0-1, fourth GES = SLID bytes 2-3	CSS adapter down	ED	ED
1E		DMA SP/AE during CDF-E Write X7E='2000' (IOC-1 with CBA-1) or '0200' (IOC-2 with CBA-2) CBA LVL1 with first GES = X'3602', second GES = SLID bytes 0-1, third GES = SLID bytes 2-3	CBA down	E5	E5
30		NPSA parameter error Diagnostic code = '40' for NPSA Invalid command Diagnostic code = '41' for invalid NDPSA pointer Abnormal request reason code = 'C003' for NPSA Error-Invalid Halt cause code	Line down	No but NCP alert	F2
31		NDPSA parameter error Diagnostic Code = '10' for NDPSA invalid receive initial Diagnostic Code = '15' for Invalid NDPSA chain pointer Diagnostic Code = '16' for Invalid NDPSA buffer pointer	Line down	No but NCP alert	F2
32		NDPSA invalid command LVL2 notify with an halt code cause of '9009' in NPSA meaning invalid command or qualifier in NDPSA.	Line down	No but NCP alert	F2
33		Station NDPSA Invalid Command	Line station reset	No but NCP alert	F4
34		Line NDPSA invalid adapter LRID LVL2 notify with an halt code cause of '9002' in NPSA meaning invalid adapter LRID in NDPSA.	Line down	No but NCP alert	F2
35		LPSA invalid status LVL2 abnormal request with an halt code cause of 'A004,A005,A006' in NPSA meaning invalid LPSA status and respectively invalid reason code or diagnostic code or congestion flags.	Line down	No but NCP alert	F2
37		Invalid resource definition data LVL2 with cc = '02'	Line down	No but NCP alert	F2

Table 12-55 (Page 3 of 4). 3746 Model 900 BER Type 9 Summary

BER ID	Abend Code (NCP)	Event Description	Recovery or PGM Action	MOSS ALERT	ALARM
38		Protocol hardware/software mismatch LVL2 with cc = '03'	Line down	No but NCP alert	F0
39		Line NDPSA error Diagnostic code = '04' for No ECB in NDPSA to pint on PIU NPSA diagnostic code = '05' for invalid offset or count in buffer prefix	Line down	No but NCP alert	F2
93		DMA Hardware Error X7E='2000' (IOC-1 with CBA-1) or '0200' (IOC-2 with CBA-2) CBA LVL1 with first GES = X'3702', second GES = SLID bytes 0-1, third GES = SLID bytes 2-3	CBA down	E7	E7
94		HPPB Hardware Error X7E='2000' (IOC-1 with CBA-1) or '0200' (IOC-2 with CBA-2) CBA LVL1 with GES-1st = X'1100'	CBA down	E6	E6
95		Adapter program reset issued by NCP level 1 failed twice (IOC error). X7E='0100' (IOC-1 with CBA-1) or '0001' (IOC-2 with CBA-2)	None	No	No
96		SAP to MOSS-E connection lost X7E='2000' (IOC-1 with CBA-1) or '0200' (IOC-2 with CBA-2) CBA LVL1 with GES-1st = X'1300'	None	F7	F7
97		IOC PIO Error LVL1 entered after NCP IOH instruction due to X7E = '0100'(IOC-1/CBA-1) or '0001'(IOC-2/CBA-2) and X76 = 'x8' or 'x4'	NCP retry	No	No
98		IOC PIO Error (threshold) Identical to BER 09 97	CBA down	E6	E6
99		Adapter LVL1-Invalid Error Status X7E='2000' (IOC-1 with CBA-1) or '0200' (IOC-2 with CBA-2)	CBA down	E8	E8
9B		IOC Error on PIO Set Hi/Lo Cmd As BER 09 98(97) but on specific IOH commands	CBA down	E6	E6
9C		PIO Get Line ID failed	None.	No	No
9C		PIO Get Line ID failed or PIO GLID failed (threshold)	CBA down	E6	E6
9D		CDF-E update error When CBA LVL1 with first GES = '43xx' as adapter CDF-E update inconsistent, second GES = adapter CDF-E entry bytes 0-1, third GES = adapter CDF-E entry byte 3-4, and so on according to xx as a multiple of 2. X7E='2000' (IOC-1 with CBA-1) or '0200' (IOC-2 with CBA-2)	CSS adapter down	EE	EE
9E		IOC PIO Error on GES	CBA down	E6	E6

Table 12-55 (Page 4 of 4). 3746 Model 900 BER Type 9 Summary

BER ID	Abend Code (NCP)	Event Description	Recovery or PGM Action	MOSS ALERT	ALARM
9F		Any CBA LVL1 with NCP generation not supporting the CSS. X7E='2000' (IOC-1 with CBA-1) or '0200' (IOC-2 with CBA-2)	None	F8	F8
A1		Unexpected Interrupt LVL2	None	No	No
A1	0936	Unexpected Interrupt LVL2 (threshold)	NCP abend	E2	E2
B0		Time-out on command No answer received (time-out) on "Execute Request" but following "Halt" has been completed successfully (Halt Cause Code = '8401').	Line down	No but NCP alert	F3
B1		Line timeout on halt command. No answer received (time-out) on "Execute Request" and on following "Halt" command.	None	No	No
B1		Adapter timeout on halt command. No answer received (time-out) on "Execute Request" and on following "Halt" command.	CBA down	EE	EE
B2		Time-Out on failure recovery Time-out on CBC reporting recovery after CBC slot failure	CBA down	E6	E6

3746 Model 900 BER Type 9 Detailed BER Display

3746-900 BER Type 9 - IDs 10 and 15 to 19 These BERs are generated for transmit side errors (TD byte 1 = odd)***:*** Format foS1, see page 12-176.

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:09  ID:hh
  <ERROR DESCRIPTION>                             <REFER.CODE IN CHAR.> CCCCCCCC
X7E:hhhh LAR:hhhh hhhh INTLVL:hh IAR:hhhhhh X76:hhhh AITADNO:hh AITTYPE:hh
AITCONF:hh AITSTAT:hh AITPROT:hhhh L1BPIO76:hhhh L1BIOHTA:hhhh L1BIOHTD:hhhh
L1XGESFG:hh L1BERFLG:hh L1XSWADE:hhhh L1BPIOTA:hhhh
NPSA PARM:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
NPSA STAT:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
1ST NDPSA:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
hhhhhhhh NACBWQH:hhhh hhhh NACBLCQH:hhhh hhhh NACB1HCC:hhhh NACBFLAG:hh
NACBERPF:hh
                                                                PAGE 1 OF 2
===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:09  ID:hh
  <ERROR DESCRIPTION>                             <REFER.CODE IN CHAR.> CCCCCCCC
X-LXB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh X-CCBSTAT1:hhhh X-CCBEND1:hhhh
X-CCBBAR:hhhh X-CCBCTL:hh X-ATTECTL:hh
X-ATT:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
hhhhhhhh hhhhhhhh hhhhhhhh
GES:hhhh hhhh hhhh hhhh hhhh hhhh
LKEFMT:hh
                                                                PAGE 2 OF 2
===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

3746-900 BER Type 9 - IDs 10 and 15 to 19 These BERs are generated for receive side errors (TD byte 1 = even)*.:* Format foS2, see page 12-176.

```
                                ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:09  ID:hh
  <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
X7E:hhhh LAR:hhhh hhhh INTLVL:hh IAR:hhhhhh X76:hhhh AITADNO:hh AITTYPE:hh
AITCONF:hh AITSTAT:hh AITPROT:hhhh L1BPIO76:hhhh L1BIOHTA:hhhh L1BIOHTD:hhhh
L1XGESFG:hh L1BERFLG:hh L1XSWADE:hhhh L1BPIOTA:hhhh
LPSA PARM:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
LPSA STAT:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
1ST LDPSA:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
hhhhhhhh NACBWQH:hhhh hhhh NACBLCQH:hhhh hhhh NACB1HCC:hhhh NACBFLAG:hh
NACBERPF:hh

                                                                  PAGE 1 OF 2

===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

```
                                ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:09  ID:hh
  <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
X-LXB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh X-CCBSTAT1:hhhh X-CCBEND1:hhhh
X-CCBBAR:hhhh X-CCBCTL:hh X-ATTECTL:hh
X-ATT:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
hhhhhhhh hhhhhhhh hhhhhhhh
GES:hhhh hhhh hhhh hhhh hhhh hhhh
LKEFMT:hh

                                                                  PAGE 2 OF 2

===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

3746-900 BER Type 9 - IDs 30 to 34 and 39: These BERs are generated for TD byte 0 bits 2-3 = 00 (line interface). Format foS3, see page 12-177.

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:09  ID:hh
  <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
TA:hhhh TD:hhhh
NPSA PARM:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
NPSA STAT:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
LPSA PARM:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
LDPSA:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhh
1ST NDPSA:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhh
SLID:hhhh hhhh NACBFLAG:hh NACBERPF:hh
NACBWQH:hhhh hhhh NACBFLCQH:hhhh hhhh NACB1HCC:hhhh

                                                                PAGE 1 OF 2

===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:09  ID:hh
  <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
R-LXB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
hhhhhhhh X-CCBSTAT1:hhhh X-CCBEND1:hhhh X-CCBBAR:hhhh
X-CCBCTL:hh X-ATTECTL:hh
X-ATT:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
SSBSSCF/CUBBSCF:hhhh LKEFMT:hh
BUFFER:hhhhhhhh hhhhhhhh hhhhhhhh


                                                                PAGE 2 OF 2

===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

3746-900 BER Type 9 - IDs 30 to 32 and 39: These BERs are generated for TD byte 0 bits 2-3 = 01 (CBA/PRC interface) or 10 (trace interface). Format foS4, see page 12-177.

```
                                ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:09  ID:hh
  <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
TA:hhhh TD:hhhh
NPSA PARM:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
NPSA STAT:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
LPSA PARM:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
LDPSA:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
1ST NDPSA:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
hhhhhhhh hhhhhhhh SLID:hhhh hhhh NACBFLAG:hh NACBRTYP:hh LACBFLAG:hh R-LXBSTFLD:hh
TRACE PT1: CCTSTATE CCTSNPM CCTRTT CCTOFLAG CCTBAR CCTBKTMR LTVTSTAT
               hh      hh      hh      hh      hh      hh      hh

                                                                 PAGE 1 OF 2
===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

```
                                ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:09  ID:hh
  <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
TRACE PT2: CCTSTATE CCTSNPM CCTRTT CCTOFLAG CCTBAR CCTBKTMR LTVTSTAT
               hh      hh      hh      hh      hh      hh      hh
AITTYPE:hh









                                                                 PAGE 2 OF 2
===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

3746-900 BER Type 9 - ID 35: Format foS5, see page 12-178.

```
                                ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:09  ID:hh
  <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
TA:hhhh TD:hhhh            LPSA PARM:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
LPSA STAT:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
LDPSA:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhh
NACBFLAG:hh NACBRTYP:hh LACBFLAG:hh LXBSTFLD:hh
TRACE PT1: CCTSTATE CCTSNPM CCTRTT CCTOFLAG CCTBAR CCTBKTMR LTVTSTAT
               hh      hh      hh      hh    hhhh    hhhh      hh
TRACE PT2: CCTSTATE CCTSNPM CCTRTT CCTOFLAG CCTBAR CCTBKTMR LTVTSTAT
               hh      hh      hh      hh    hhhh    hhhh      hh
AITTYPE:hh

===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

3746-900 BER Type 9 - IDs 37 and 38: Format foS6, see page 12-178.

```
                                ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:09  ID:hh
  <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
TA:hhhh TD:hhhh
LPSA PARM:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
LPSA STAT:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
LDPSA:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhh
NACBFLAG:hh NACBRTYP:hh LACBFLAG:hh R-LXBSTFLD:hh
DATA:hhhh hhhh LKEFMT:hh AITTYPE:hh




===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

3746-900 BER Type 9 - ID A1: Format foS7, see page 12-179.

```
                                ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:09  ID:hh
  <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
NPSA PARM:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
NPSA STAT:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
CCBBAR:hhhh TA:hhhh TD:hhhh
CNT:hhh







===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

3746-900 BER Type 9 - IDs B1 and B2: Format foS8, see page 12-179.

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:09  ID:hh
  <ERROR DESCRIPTION>                             <REFER.CODE IN CHAR.> CCCCCCCC
TA:hhhh TD:hhhh
NPSA PARM:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
NPSA STAT:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
LPSA PARM:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
NACBFLAG:hh NACBERPF:hh NACBWQH:hhhhhhhh NACBLCQH:hhhhhhhh NACB1HCC:hhhh
R-LXB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
hhhhhhhh X-CCBSTAT1:hhhh X-CCBEND1:hhhh X-CCBBAR:hhhh X-CCBCTL:hh X-ATTECTL:hh
X-ATT:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh

                                                                 PAGE 1 OF 2
===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:09  ID:hh
  <ERROR DESCRIPTION>                             <REFER.CODE IN CHAR.> CCCCCCCC
AITADNO:hh AITTYPE:hh AITCONF:hh AITSTAT:hh AITPROT:hhhh LKEFMT:hh
TRACE PT1: CCTSTATE CCTSNPM CCTRTT CCTOFLAG CCTBAR CCTBKTMR LTVTSTAT
               hh      hh      hh      hh    hhhh    hhhh      hh
TRACE PT2: CCTSTATE CCTSNPM CCTRTT CCTOFLAG CCTBAR CCTBKTMR LTVTSTAT
               hh      hh      hh      hh    hhhh    hhhh      hh




                                                                 PAGE 2 OF 2
===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

3746-900 BER Type 9 - IDs 11 to 14, 1B, 93 to 99, 9B to 9F: Format foS9, see page 12-180.

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:09  ID:hh
  <ERROR DESCRIPTION>                             <REFER.CODE IN CHAR.> CCCCCCCC
X7E:hhhh LAR:hhhh hhhh INTLVL:hh IAR:hhhhhh X76:hhhh AITADNO:hh AITTYPE:hh
AITCONF:hh AITSTAT:hh AITPROT:hhhh L1BPIO76:hhhh L1BIOHTA:hhhh
L1BIOHTD:hhhh L1XGESFG:hh L1BERFLG:hh L1XSWADE:hhhh L1BPIOTA:hhhh
GES:hhhh hhhh hhhh hhhh hhhh hhhh
 CDF-E: hhhhhhhh




===>Format 5 general

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

3746-900 BER Type 9 - ID 1D: Format foS10, see page 12-180.

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:09  ID:hh
  <ERROR DESCRIPTION>                             <REFER.CODE IN CHAR.> CCCCCCCC
X7E:hhhh LAR:hhhh hhhh INTLVL:hh IAR:hhhhhh X76:hhhh AITADNO:hh AITTYPE:hh
AITCONF:hh AITSTAT:hh AITPROT:hhhh L1BPIO76:hhhh L1BIOHTA:hhhh
L1BIOHTD:hhhh L1XGESFG:hh L1BERFLG:hh L1XSWADE:hhhh L1BPIOTA:hhh
GES:hhhh hhhh hhhh hhhh hhhh hhhh
 LNVT SEG ADDRESS: hhhhhhhh




===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

3746-900 BER Type 9 - ID 1E: Format foS11, see page 12-180.

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:09  ID:hh
  <ERROR DESCRIPTION>                             <REFER.CODE IN CHAR.> CCCCCCCC
X7E:hhhh LAR:hhhh hhhh INTLVL:hh IAR:hhhhhh X76:hhhh AITADNO:hh AITTYPE:hh
AITCONF:hh AITSTAT:hh AITPROT:hhhh L1BPIO76:hhhh L1BIOHTA:hhhh
L1BIOHTD:hhhh L1XGESFG:hh L1BERFLG:hh L1XSWADE:hhhh L1BPIOTA:hhhh
GES:hhhh hhhh hhhh hhhh hhhh hhhh
 CDF-E: hhhhhhhh




===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

3746-900 BER Type 9 - Field Description

For fields not listed in the following table, use the NCP documentation for field description.

Table 12-56. 3746-900 BER type 9 Field Description

Field Name	Meaning	Refer to
AITADNO	TA data registerbyte 0 bits 3-7	page 3-64
AITPROT	Adapter protocol status	page 12-174
AITCONF	Adapter configuration	page 12-174
AITSTAT	Adapter status indicator	page 12-174
AITTYPE	Adapter type	page 12-174
CNT	Repetition counter (ber flooding). Number of times the BER appeared.	-
GES	Get error status	page 12-175
IAR	IAR of interrupt level.	page 2-24
INTLVL	Interrupt level	-
LAR	Lagging Address Register (X'74').	page 2-44
LKEFMT	Functional group	page 12-175
L1BERFLG	Box event record flags	page 12-175
L1BIOHTA/ TA	IOHI image -- TA data register (TA: hhhh means data bytes 0 and 1).	page 3-64
L1BIOHTD/ TD	IOHI image -- TD data adapter specific bytes (TD: hhhh means data bytes 0 and 1).	-
L1XGESFG	Invalid GES indicators flag byte	page 12-175
L1XSWADE	Switch adapter error register.	page 3-23
X76	X'76' - IOC error summary register.	page 2-36
X7E	X'7E' - CCU level 1 interrupt.	page 2-43

Table 12-57 (Page 1 of 2). 3746-900 BER Type 9 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
AITCONF		Adapter configuration
	1	Adapter not installed
	. 1	Adapter not operative
	. . 1	Adapter not attached to this CCU
	. . . 1	Adapter not switched to this CCU
	. . . . x . . .	Adapter not switched to this CCU x = 0 : No integrated modem in use x = 1 : Integrated modem in use
	. . . . . x . .	Unused
	. . . . . 1 .	CSS coupler is not primary
	 x	Unused
AITPROT		Adapter protocol status
Byte 0	1	Adapter slot protocol is down
	. 1	Trace protocol is down
	. . 1	Adapter slot and trace protocol are down
	. . . x x x x x	Unused
Byte 1	1	SDLC mapper is down
	. 1	ESCON mapper is down
	. . 1	TRA mapper is down
	. . . x x x x x	Unused
AITSTAT		Adapter status indicator
Byte 0		Line adapter status indicator
	1	Interrupt from the line adapter when disconnected
	. 1	IOH instruction to line adapter failed twice
	. . x	Unused
	. . . 1	Line adapter down due to line adapter LVL1 interrupt
	. . . . x . . .	Unused
	. . . . . 1 . .	Line adapter down due to exceeding incident limit
	. . . . . 1 .	Line adapter down due to MOSS command
	 x	Unused
Byte 1		Channel adapter status indicator
	1	Channel adapter active for NCP
	. 1	Channel adapter active for EP
	. . 1	Channel adapter active for programmed resource
	. . . 1	Channel adapter is 'install in progress'
	. . . . 1 . . .	Channel adapter is CACM mode disconnected
	. . . . . x . .	Unused
	. . . . . x .	Unused
	 1	Channel adapter is permmmmmmmmanently down
AITTYPE	xxxx xxxx	Adapter type X'00' = Undefined processor X'01' = CADS X'02' = BCCA X'10' = TSS X'20' = HPTSS X'30' = TRA X'50' = CBA X'51' = CBSP X'53' = ESCP X'54' = TRP

Table 12-57 (Page 2 of 2). 3746-900 BER Type 9 Field Details

Field Name	Bit Pattern or Hex Value	Meaning
GES (1st)		Get error status
	Byte 0	Byte 0 Bits 0-3 = Error category Byte 0 Bits 4-7 = Error type
	Byte 1	Byte 1 Bits 0-7 = Total number of associated GESs after this one.
LKEFMT	x	x = 0 : Link definition x = 1 : Station definition
	. x	x = 0 : Physical definition x = 1 : Logical definition
	. . 0 0	Unused
	. . . . x x x x	Protocal type definition xxxx = 0000 : None xxxx = 0010 : ESCON xxxx = 0011 : TRA
L1BERFLG		Box event record flags
	x	x = 0 : Control program is EP x = 1 : Control program is NCP or PEP
	. 1	Adapter down
	. . 1	Control program put adapter down
	. . . 1	Redrive has been disabled (NCP only) or error on invalid ESC (EP only)
	. . . . 1 . . .	MOSS CACM timeout detected (3745 only)
	. . . . . 1 . .	Error on get error status
	. . . . . 1 .	CA is being disabled
	 1	IOH or IOHI on level 1 failed twice
L1XGESFG		Invalid GES indicators flag byte
	1	Invalid GES error category
	. 1	Invalid GES error type
	. . 1	Invalid GES count
	. . . 1	Invalid GES TA/TD
	. . . . x x x x	Unused

3746 Model 900 BER Type 09 - Formats

Format foS1

IDs: 10 and 15 to 19

Bytes	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35-38	LAR
39	INTLVL
40-42	IAR
43-44	X76
45	AITADNO
46	AITTYPE
47	AITCONF
48	AITSTAT
49-50	AITPROT
51-52	L1BPIO76
53-54	L1BIOHTA
55-56	L1BIOHTD
57	L1XGESFG
58	L1BERFLG
59-60	L1XSWADE
61-62	L1BPOHTA
63-94	NPSA
95-126	NDPSA
127-130	NACBWQH
131-134	NACBLCQH
135-136	NACB1HCC
137	NACBFLAG
138	NACBERPF
139-174	X-LXB
175-176	X-CCBSTAT1
177-178	X-CCBEND1
179-180	X-CCBBAR
181	X-CCBCTL
182	X-ATTECTL
183-214	X-ATT
215-226	GESs
227	LKEFNT

Format foS2

IDs: 10 and 15 to 19

Bytes	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35-38	LAR
39	INTLVL
40-42	IAR
43-44	X76
45	AITADNO
46	AITTYPE
47	AITCONF
48	AITSTAT
49-50	AITPROT
51-52	L1BPIO76
53-54	L1BIOHTA
55-56	L1BIOHTD
57	L1XGESFG
58	L1BERFLG
59-60	L1XSWADE
61-62	L1BPOHTA
63-94	LPSA
95-126	NDPSA
127-130	NACBWQH
131-134	NACBLCQH
135-136	NACB1HCC
137	NACBFLAG
138	NACBERPF
139-174	X-LXB
175-176	X-CCBSTAT1
177-178	X-CCBEND1
179-180	X-CCBBAR
181	X-CCBCTL
182	X-ATTECTL
183-214	X-ATT
215-226	GESs
227	LKEFNT

Figure 12-26 (Part 1 of 5). 3746 Model 900 BER Formats

Format foS3

IDs: 30 to 34 and 39	
Bytes	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	TA
35-36	TD
37-52	NPSA PARM
53-68	NPSA STAT
69-84	LPSA PARM
85-110	LDPSA
111-116	Unused
117-142	NDPSA
143-148	Unused
149-152	SLID
153	NACBFLAG
154	NACBERPF
155-158	NACBWQH
159-162	NACBLCQH
163-164	NACB1HCC
165-200	R-LXB
201-202	X-CCBSTAT1
203-204	X-CCBEND1
205-206	X-CCBBAR
207	X-CCBCTL
208	X-ATTECTL
209-240	X-ATT
241-242	SSBSSCF/CUBBSCF
243	LKEFNT
244-255	BUFFER

Format foS4

ID : 30 to 32 and 39	
Bytes	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	TA
35-36	TD
37-52	NPSA PARM
53-68	NPSA STAT
69-84	LPSA PARM
85-110	LDPSA
111-116	Unused
117-142	NDPSA
143-148	Unused
149-152	SLID
153	NACBFLAG
154	NACBRTYP
155	LACBFLAG
156	R-LXBSTFLD
157	PT1 CCTSTATE
158	PT1 CCTSNPM
159	PT1 CCTRTT
160	PT1 CCTOFLAG
161-162	PT1 CCTBAR
163-164	PT1 CCTBKTMR
165	PT1 LTVTSTAT
166	Unused
167	PT2 CCTSTATE
168	PT2 CCTSNPM
169	PT2 CCTRTT
170	PT2 CCTOFLAG
171-172	PT2 CCTBAR
173-174	PT2 CCTBKTMR
175	PT2 LTVTSTAT
176	AITTYPE

Figure 12-26 (Part 2 of 5). 3746 Model 900 BER Formats

Format foS5

ID : 35	
Bytes	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	TA
35-36	TD
37-52	LPSA PARM
53-68	LPSA STAT
69-100	LDPSA
101	NACBFLAG
102	NACBRTYP
103	LACBFLAG
104	R-LXBSTFLD
105	PT1 CCTSTATE
106	PT1 CCTSNPM
107	PT1 CCTRTT
108	PT1 CCTOFLAG
109-110	PT1 CCTBAR
111-112	PT1 CCTBKTMR
113	PT1 LTVTSTAT
114	Unused
115	PT2 CCTSTATE
116	PT2 CCTSNPM
117	PT2 CCTRTT
118	PT2 CCTOFLAG
119-120	PT2 CCTBAR
121-122	PT2 CCTBKTMR
123	PT2 LTVTSTAT
124	AITTYPE

Format foS6

IDs: 37 and 38	
Bytes	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	TA
35-36	TD
37-52	LPSA PARM
53-68	LPSA STAT
69-100	LDPSA
101	NACBFLAG
102	NACBRTYP
103	LACBFLAG
104	R-LXBSTFLD
105-108	DATA
109	LKEFNT
110	AITTYPE
111-112	Repetit. BER count

Figure 12-26 (Part 3 of 5). 3746 Model 900 BER Formats

Format foS7

ID : A1	
Bytes	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-48	NPSA PARM
49-64	NPSA STAT
65-66	CCBBAR
67-68	TA
69-70	TD
71-72	Count

Format foS8

IDs: B1 and B2	
Bytes	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	TA
35-36	TD
37-52	NPSA PARM
53-68	NPSA STAT
69-84	LPSA PARM
85	NACBFLAG
86	NACBERPF
87-90	NACBWQH
91-94	NACBLCQH
95-96	NACB1HCC
97-132	R-LXB
133-134	X-CCBSTAT1
135-136	X-CCBEND1
137-138	X-CCBBAR
139	X-CCBCTL
140	X-ATTECTL
141-172	X-ATT
173	AITADNO
174	AITTYPE
175	AITCONF
176	AITSTAT
177-178	AITPROT
179	LKEFMT
180	Unused
181	PT1 CCTSTATE
182	PT1 CCTSNPM
183	PT1 CCTRTT
184	PT1 CCTOFLAG
185-186	PT1 CCTBAR
187-188	PT1 CCTBKTMR
189	PT1 LTVTSTAT
190	Unused
191	PT2 CCTSTATE
192	PT2 CCTSNPM
193	PT2 CCTRTT
194	PT2 CCTOFLAG
195-196	PT2 CCTBAR
197-198	PT2 CCTBKTMR
199	PT2 LTVTSTAT

Figure 12-26 (Part 4 of 5). 3746 Model 900 BER Formats

Format foS09

IDs: 11-14, 1B, 93-99, 9B-9F	
Bytes	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35-38	LAR
39	INTLVL
40-42	IAR
43-44	X76
45	AITADNO
46	AITTYPE
47	AITCONF
48	AITSTAT
49-50	AITPROT
51-52	L1BPIO76
53-54	L1BIOHTA
55-56	L1BIOHTD
57	L1XGESFG
58	L1BERFLG
59-60	L1XSWADE
61-62	L1BPOHTA
63-66	CDF-E (ID 12 only)
67-78	GESs

Format foS10

IDs: 1D	
Bytes	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35-38	LAR
39	INTLVL
40-42	IAR
43-44	X76
45	AITADNO
46	AITTYPE
47	AITCONF
48	AITSTAT
49-50	AITPROT
51-52	L1BPIO76
53-54	L1BIOHTA
55-56	L1BIOHTD
57	L1XGESFG
58	L1BERFLG
59-60	L1XSWADE
61-62	L1BPOHTA
63-74	GESs
75-78	LNVT SEG ADDRESS

Format foS11

ID : 1E	
Bytes	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35-38	LAR
39	INTLVL
40-42	IAR
43-44	X76
45	AITADNO
46	AITTYPE
47	AITCONF
48	AITSTAT
49-50	AITPROT
51-52	L1BPIO76
53-54	L1BIOHTA
55-56	L1BIOHTD
57	L1XGESFG
58	L1BERFLG
59-60	L1XSWADE
61-62	L1BPOHTA
63-74	GESs
75-78	CDF-E

Figure 12-26 (Part 5 of 5). 3746 Model 900 BER Formats

NCP CA BER Type 10

CA BER Type 10 - Summary

Table 12-58 (Page 1 of 5). CA BER Type 10 Summary

BER ID	ABEND Code (NCP)	Event Description	Recovery or PGM Action	ALERT	ALARM
10	0915	• CADS: Invalid ESC address used (EP or NEO are the CA owner) – Mismatch between ESC addresses range defined in NCP/PEP sysgen and in MOSS CDF for involved CA. – Program error (for example, possible overwrite of control blocks where ESC values are kept) if found in normal operations • BCCA: ESC addresses not allowed on this type of CA.	NCP re-IPL	NO	NO
14	0910	Address exception (AIO) (X'76' bit 0.0 or 1.0 ON)	NCP re-IPL	NO	NO
16	0911	Storage protect (AIO) (X'76' bit 0.1 or 1.1 ON)	NCP re-IPL	NO	NO
18	0912	Invalid CA selection in Control Program (attempt to select a non-installed CA). Control Program issuing an output X'07' with **either** bit 0.2 or 0.3 set **and** bits 0.4, 0.6 indicating select bits for a CA that is not installed.	NCP re-IPL	NO	NO
1B	0913	Invalid IOH/IOHI input to CA (for example input to register which cannot be read) X'7E' bit 0.5 ON	NCP re-IPL	NO	NO
1C	0914	Output sequence issued in error to CA X'0D' bit 1.0 ON	NCP re-IPL	NO	NO
1E	0913	Invalid IOH/IOHI output to CA output X'0D', X'0E', or X'0F'	NCP re-IPL	NO	NO
1F	0913	Invalid IOH/IOHI output to CA (Hardware detected) X'7E' bit 0.5 ON	NCP re-IPL	NO	NO
34	091F	Level 3 IPL configuration check • Stacked status cleared by initial select for the 1st time, or transfer of final status but not on the IPLing CA. built for the non-IPLing CA • PRI built for the IPLing CA	NCP re-IPL	NO	NO
35	0	ESC address (from host) not within range (PEP on level 3 interrupt) Mismatch between ESC addresses range defined in NCP/PEP sysgen		NO	NO
80	0	Autoselection error: IOH IN X'0F' failed (X'09' and X'0A' contain 'FEFE')	Retry cmd in X'0F'		
80	0920	Autoselection error (limit threshold) • X'76' bit 0.4 ON for IOC1 time out, or • X'76' bit 1.4 ON for IOC2 time out • X'76' bits 0.0 to 0.3 (or 1.0 to 1.3) contain '0010'.	NCP re-IPL	NO	NO
80	0	fit=5.Autoselection error (limit threshold) • X'76' bit 0.4 ON for IOC1 time out, or • X'76' bit 1.4 ON for IOC2 time out • X'76' bits 0.0 to 0.3 (or 1.0 to 1.3) contain '0101'.	CA down	50	50

Table 12-58 (Page 2 of 5). CA BER Type 10 Summary

BER ID	ABEND Code (NCP)	Event Description	Recovery or PGM Action	ALERT	ALARM
80	0920	Autoselection error (limit threshold) • X'76' bit 0.4 ON for IOC1 time out, or • X'76' bit 1.4 ON for IOC2 time out • X'76' bits 0.0 to 0.3 (or 1.0 to 1.3) contain '0101'.	NCP re-IPL	NO	NO
81	0	Failure to read X'08', or more than one CA in error from the X'08'. CA dropped from the autoselection chain bit 0 in CA X'08' byte 0	CA down	50	50
81	0	• CA dropped from the Autoselection chain in CA X'08' byte 0, CAs bit = 0 • Non-contiguous CAs in the autoselection chain All CAs on the IOC bus are removed from the chain.		NO	NO
82	0	CA cannot be selected in level 1, not possible to issue IN CA X'08	CA down	50	50
82		CA cannot be selected in level 1 (last CA, no INN traffic)	NCP re-IPL	NO	40
83		Autoselection error, 1 CA identified		NO	NO
84		Autoselection error, several errors		NO	NO
85	917 919 91A	CA not accessible (not attached, not initialized) Unresolved AIO Unresolved adapter error PIO error on a CA		NO	NO
86	917 919 91A	CA not operative Unresolved AIO Unresolved adapter error PIO error on a CA		NO	NO
87	917 919 91A	Interrupt from a disable CA Unresolved AIO Unresolved adapter error PIO error on a CA		NO	NO
88	917 919 91A	Unexpected level 1 in concurrent maintenance AIO threshold reached Unresolved interrupt PIO threshold reached		NO	NO
89	917 919 91A	Unexpected level 1 from CA CACM disconnect or with CA install in progress AIO threshold reached Unresolved interrupt PIO threshold reached		NO	NO
90	0	CADS: Invalid ESC address (PEP or NEO are not the CA owner). ESC addresses not active on the CA. BCCA: ESC addresses not allowed on this type of CA.	NCP retry	NO	NO
90	0	Invalid ESC address (limit threshold)	CA down	50	50
90		Invalid ESC address (last CA, no INN) all CAs have been disabled	NCP re-IPL	NO	NO

Table 12-58 (Page 3 of 5). CA BER Type 10 Summary

BER ID	ABEND Code (NCP)	Event Description	Recovery or PGM Action	ALERT	ALARM
91	0	AIO error • X'75' bit 0.0 and 1.0 OFF • X'76' bit 0.4 ON for IOC1 time out, or • X'76' bit 1.4 ON for IOC2 time out • X'76' bit 0.5 or 1.5 for IOC1/IOC2 bus IN parity error • X'76' bit 0.6 or 1.6 in both cases (AIO) • X'76' bits 0.0, 0.1, 0.2, 0.3 or X'76' bits 1.0, 1.1, 1.2, 1.3 contain the IOC status at the time of error	NCP retry	NO	NO
91	0	AIO error (limit threshold)	CA down	50	50
91		AIO error (last CA, no INN), all CAs have been disabled	NCP re-IPL	NO	NO
92	0922	Level 1 from CA during recovery (interrupt from a CA which is already being disabled by error recovery procedures as a result of level 1 checks). Indicates the probable failure of the disable sequence	NCP re-IPL	NO	40
93	0	Driver/receiver check X'0D' bit 1.6 or 1.7 ON	NCP retry	NO	NO
93	0	Driver/receiver check (limit threshold)	CA down	50	50
93		Driver/receiver check (last CA, no INN) All CAs have been disabled	NCP re-IPL	NO	NO
94	0	Level 1 from a CA not generated active X'7E' bit 0.5 or 1.5 ON	NCP retry	NO	NO
94	0921	Lvl 1 from a CA not generated active (limit threshold)	NCP re-IPL	NO	NO
96	0	Channel bus IN check (X'0D' bit 1.3 or 1.5 ON)	NCP retry	NO	NO
96	0	Channel bus IN check (limit threshold)	CA down	50	50
96		Channel bus IN check (last CA, no INN), all CAs have been disabled	NCP re-IPL	NO	40
97	0	PIO error (Input or output IOH failed) • X'76' bit 0.4 ON for IOC1 time out, or X'76' bit 1.4 ON for IOC2 time out • X'76' bit 0.5 or 1.5 for IOC1/IOC2 bus IN parity error X'76' bit 0.6 or 1.6 in both cases	NCP retry	NO	NO
97	0	PIO error (limit threshold)	CA down	50	50
97	091A	PIO error (last CA, no INN), all CAs have been disabled	NCP re-IPL	NO	40
98	0	Internal adapter error: • X'7E' bit 0.5 or 1.5 ON • X'0E' bits to indicate CAs Control program checks the level 3 instruction that failed. • If it is a valid IOH/IOHI, retry the instruction in the interrupted level • If it is not a valid IOH/IOHI, attempt to disable the CA	NCP retry	NO	NO

Table 12-58 (Page 4 of 5). CA BER Type 10 Summary

BER ID	ABEND Code (NCP)	Event Description	Recovery or PGM Action	ALERT	ALARM
98	09F0	Internal adapter error : • Final status transfer. Not enough information available to recover when a data/status interrupt is pending during level 1 processing	NCP re-IPL	NO	NO
98	09F1	Internal Adapter error : • Status byte cleared (X'00' bit 0.6) Not enough information available to recover when an initial selection interrupt is pending during level 1 processing.	NCP re-IPL	NO	NO
98	0	Internal adapter error (limit threshold)	CA down	50	50
98		Internal adapter error (last CA, no INN), all CAs have been disabled	NCP re-IPL	NO	NO
99	0	Ground fault, X'0D' bit 1.4 ON	NCP retry	NO	NO
99	0	Ground fault (limit threshold)	CA down	50	50
9A	0920	IOH failed in level 1, abort AIO recovery. Control program cannot get the registers needed to determine the error	NCP re-IPL	NO	NO
9B	0920	IOH failed in level 1, abort PIO recovery: • IOH required for the recovery failed twice in level 1, or • Output IOH X'07' failed twice in level 1	NCP re-IPL	NO	40
9B	0	IN CA X'08' failed in level 1	NCP retry	NO	NO
9B	0	IN CA X'08' failed in level 1 (limit threshold)		NO	NO
9C	0920	IOH failed in level 1, abort ADP recovery	NCP re-IPL	NO	NO
9D	0	CA microcode detected error • X'0D' bit 0.1 ON • Origin found in X'60'	CA down	51	51
9E	0	Unresolved error on CA level 1: • CA register X'0D' did not specify any adapter error bit • See "Specific Mechanism", page 12-14	NCP retry	NO	NO
9E	0	Unresolved error on CA level 1 (limit threshold)	CA down	50	50
9E		Unresolved error on CA level 1 (last CA, no INN). All CAs have been disabled	NCP re-IPL	NO	NO
9F	0925	ESC interrupt (PEP/NEO are not CA owner) • X'0F' bits 0.2 or 0.3 ON • ESC address in X'3' byte 0	NCP re-IPL	NO	NO
B1	0	Unresolved CA level 3 • Initial select interrupt (X'0F' bit 0.2), but no bit ON in X'00'. • See "Specific Mechanism", page 12-14	NCP retry	NO	NO
B1	091C	Unresolved CA level 3 initial select interrupt (limit threshold)	NCP re-IPL	NO	NO
B2	0	Unresolved CA level 3 • Data/status interrupt (X'0F' bit 0.3), but no bit ON in X'02', and it is not a system reset (no bit in X'00').	NCP retry	NO	NO

Table 12-58 (Page 5 of 5). CA BER Type 10 Summary

BER ID	ABEND Code (NCP)	Event Description	Recovery or PGM Action	ALERT	ALARM
B2	091D	Unresolved CA level 3 data/status interrupt (limit threshold)	NCP re-IPL	NO	NO
B3	0	Unresolved CA level 3 interrupt (level 3 but no initial select nor data status)	NCP retry	NO	NO
B3	091E	Unresolved CA level 3 interrupt (limit threshold) (addresses are within the ESC address range, but not in the PEP GEN)	NCP re-IPL	NO	NO
B5	0927	NCP cannot disable CA after an error detected on the CA. NCP exhausted disable count	NCP re-IPL	NO	NO
B6	0	Inappropriate command (neither NOP nor TIO) on stacked initial status: PEP only (X'00' bit 0.5)	NCP retry	NO	NO
B6	0926	Inappropriate command (neither NOP nor TIO) on stacked initial status (limit threshold)	NCP re-IPL	NO	NO
B7	091E	CA level 3 interrupt from an undefined CA • CA installed and attached but not defined in NCP • CA installed and attached but the box is defined as link-attached	NCP re-IPL	NO	NO
B8	091E	CA level 3 interrupt from a CA that is neither installed nor attached to that CCU	NCP re-IPL	NO	NO
B9	0	Channel media device level error	NCP retry	NO	NO
BA	091E	CA level 3 interrupt but the CA is not operational	NCP re-IPL	NO	NO
BB		CA level 3 from a CA that is CACM disconnect (MOSS cancel CACM and reset CA)		NO	NO
BC		CA level 3 from a CA with install in progress (MOSS cancel CACM and reset CA)		NO	NO
BD	091E	CA level 3 from a CA ERP inoperative	NCP re-IPL	NO	NO
BE	091E	CA level 3 from a disabled CA	NCP re-IPL	NO	NO
BF	0	Unresolved adapter level 1 interrupt (CA reg X'0E' did not specify a CA with the level 1 interrupt)	NCP retry	NO	NO
BF	0919	Unresolved adapter level 1 interrupt (limit threshold)	NCP re-IPL	NO	NO

Note: In case of abend, NCP re-IPL is performed and the Alarm/Alert is generated when IPL is completed. Alert is triggered by MOSS BER ID 06, error code 05.

CA BER Type 10 - Detailed BER Display

CA BER Type 10 - IDs 18, 1C, 1E, 80, 97, 9B: Format foC1, see page 12-193. Program level 1 generates one of the following BERs when an error occurs during a PIO operation on a channel.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:10 ID:hh <LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                          <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb  CAVT:bbbbbbbb  X75:hhhh
X7E:hhhh  X76:hhhh  I:hhhh  LAR:hhhhhhhh  X76U:hhhh  ETA:hhhh   ADNO:hh
SWA:hhhh  IAR:hhhhhh  TA:hhhh  TD:hhhh  X8:hhhh  X9:hhhh    XA:hhhh
X50:hhhh  X51:hhhh  X52:hhhh
CAB:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
    hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
CAC:hhhh
 X0:hhhh X1:hhhh X2:hhhh X3:hhhh X4:hhhh X5:hhhh X6:hhhh X7:hhhh
 XB:hhhh XC:hhhh XD:hhhh XE:hhhh XF:hhhh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

CA BER Type 10 - IDs 14, 16, 91, 9A: Format foC2, see page 12-193. Program level 1 generates one of the following BERs when an error occurs during an AIO operation with a channel.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:10 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                          <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
X7E:hhhh  X76:hhhh  X75:hhhh  ETA:hhhh  X76U:hhhh  FPR:hhhhhhhh SWA:hhhh
X50:hhhh  X51:hhhh  X52:hhhh
CAB:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
    hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
CAC:hhhh
 X0:hhhh  X1:hhhh  X2:hhhh  X3:hhhh  X4:hhhh  X5:hhhh  X6:hhhh  X7: hhhh
 XB:hhhh  XC:hhhh  XD:hhhh  XE:hhhh  XF:hhhh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

CA BER Type 10 IDs 10, 1B, 1F, 87, 90, 92, 93, 94, 96, 98, 99, 9C, 9D, 9E, 9F

Format foC3, see page 12-194. Program level 1 generates one of these BERs when a CA reports an error on its level 1.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:10 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                          <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
X7E:hhhh  X76:hhhh  ADNO:hh  LAR:hhhhhhhh  X76U:hhhh  TA:hhhh  SWA  :hhhh
X60:hhhh  X50:hhhh  X51:hhhh  X52:hhhh
CAB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
    hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh CAC:hhhh
 X0:hhhh  X1:hhhh  X2:hhhh  X3:hhhh  X4:hhhh  X5:hhhh  X6:hhhh  X7: hhhh
 XB:hhhh  XC:hhhh  XD:hhhh  XE:hhhh  XF:hhhh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

CA BER Type 10 - IDs 34, 35, B1, B2, B5, B6, BD, BE: Format foC4, see page 12-194. Program level 3 generates one of the following BERs when a CA request at level 3 remains unresolved.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:10 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                            <REFER.CODE IN CHAR.> CCCCCCCC
CAVT:bbbbbbbb
X77:hhhh  X7F:hhhh  XO:hhhh  X1:hhhh  X2:hhhh  X3:hhhh X4:hhhh X5:hhhh
X6:hhhh  X7:hhhh  XB:hhhh  XC:hhhh  XF:hhhh
CAB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
    hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
CAC:hhhh TA:hh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

When the registers are set to ‘FF’, the information they contain is not valid.

CA BER Type 10 - IDs 81, 82, 83, 84: Format foC5, see page 12-194. Program level 3 generates one of the following BERs when a CA request at level 3 remains unresolved.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:10 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                            <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb  CAVT:bbbbbbbb  STAT:hhhh
X7E:hhhh  X76:hhhh  I:hhhh  LAR:hhhhhhhhh  X75:hhhh  X76U:hhhh  ETA:hhhhhhhh
ADNO:hh
SWA:hhhh IAR:hhhhhh  TA:hhhh TD:hhhh X8:hhhh XE:hhhh  XF:hhhh
FPR:hhhhhhhh
CAB:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
    hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

CA BER Type 10 - IDs 85, 86, 88, 89, BF: Format foC8, see page 12-195. Program level 3 generates one of the following BERs when a CA request at level 3 remains unresolved.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:10 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                           <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
X7E:hhhh  X76:hhhh  ADNO:hh  LAR:hhhhhhhh  X76U:hhhh  TA:hhhh  SWA  :hhhh
XD:hhhh  XE:hhhh  XF:hhhh
CAVT:bbbbbbbb  CCU-INPUT-X57:hhhh  CCU-OUTPUT-X57:hhhh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

CA BER Type 10 - IDs B3, B7, B8, BA, BB, BC, BF: Format foC6, see page 12-194. Program level 3 generates one of the following BERs when a CA request at level 3 remains unresolved.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:10 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                            <REFER.CODE IN CHAR.> CCCCCCCC
CAVT:bbbbbbbb
X77:hhhh  X7F:hhhh
TA:hhhh  STATUS:hhhh  CCU=INPUT-X57:hhhh  CCU-OUTPUT-X57:hhhh  XF:hhhh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

CA BER Type 10 - ID B9: Format foC7, see page 12-195. Program level 3 generates the following BER for a CA condition.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:10 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                            <REFER.CODE IN CHAR.> CCCCCCCC
CAVT:bbbbbbbb
X77:hhhh  X7F:hhhh  TA:hh  STATUS:hhhh  X0:hhhh  X2:hhhh  XF:hhhh  X6:hhhh
CMD:hh  CABSENSE:hh  SENSE 1:hh  SENSE 2:hh
ABORT REASON:hh  DATA REASON:hh  CMD REJ REASON:hh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

CA BER Type 10 - Field Description

Table 12-59. CA BER type 10 Field Description

Field Name	Meaning	Refer to
ABORT REASON	CAB abort reason	page 12-192
ADNO	• field ADNO for PIO operation • field XE for CA error reported at level 1 • field X75 for AIO operation • field XF for CA error reported at level 3. CA address (1 to 16) as used by NCP/PEP in its control blocks (not to be confused with ESC or NSC address.	
CAB	X'30' bytes of fields from the CAB, from CABCND up to and including CABXR6F. For PEP the fields CASEL through TERMADR are included from the PEP CHCB (X'10' bytes). The remaining space is padded with X'FF' for PEP.	(*)
CABSENSE	CA sense byte	page 12-191
CAC	Channel adapter contact control flags.	(*)
CAVT	CAVT flag	(*)
CCU INPUT X57	X'57' - Input CA command LS reg (same for output).	page 12-117
CMD	Current channel command	page 12-191
CMD REJ REASON	Command reject raison code	page 12-192
DATA REASON	Data check raison code	page 12-192
ETA	TA field of IOH failure in level 1.	(*)
F	Indicator flag byte (indicates a byte expansion follows)	(*)
I	First two bytes of instruction.	
IAR	IAR of interrupt level.	page 2-24
LAR	Lagging Address Register (X'74').	page 2-44
SENSE 1	Extended sense byte 1	page 12-191
SENSE 2	Extended sense byte 2	Unused
STAT	CA Reg X'9' Autoselection chain status.	page 7-25
STATUS	CER channel adapter state.	page 12-191
SWA	Switch adapter error register.	page 3-23
TA	IOHI image -- TA data registers X'50', X'70'. (TA: hhhh means data bytes 0 and 1).	page 3-61
TD	IOHI image -- TD data adapter specific bytes (TD: hhhh means data bytes 0 and 1).	page 3-61
X0-XF	Channel Adapter Registers	page 7-16
X3M and X6M	CA cycle steal fixed pointer register.	page 2-24
X50	X'50' - Adapter bus control module check register	page 7-40
X51	X'51' - Channel A control module check register	page 7-40
X52	X'52' - Channel B control module check register	page 7-40
X60	X'60' - Microcode-detected error code register	page 7-41
X7E	X'7E' - CCU level 1 interrupt.	page 2-43
X7F	X'7F' - Interrupt request reg - CCU level 2, 3, and 4.	page 2-44
X74	X'74' - Cycle steal control word register.	page 2-33
X75	X'75' - LAR bytes (see CAn).	page 2-34
X76	X'76' - IOC error summary register.	page 2-36
X76U	X'76' - Cause of error not found (PIO to read error register failed).	page 2-36
X77	X'77' - Interrupt request reg - adapter levels 2 and 3.	page 2-38
X79	X'79' - Utility.	page 2-39

(*) For software information on BERs originated by NCP/PEP, refer to the associated product documentation.

CA BER Type 10 - Field Details

Table 12-60 (Page 1 of 2). MOSS BER Type 10 ID B9 Field Details

Field Name	Bit pattern or Hex value	Meaning
CMD		Current channel command
	01	Write
	02	Read
	03	No op
	04	Sense
	05	Write IPL control
	09	Write break
	31	Write start 0
	32	Read start 0
	51	Write start 1
	52	Read start 1
	61	Write XID control
	62	Read XID control
	72	Read configuration data
	93	Restart reset
	A3	Discontact control
	C3	Contact control
	E4	Sense ID
STATUS		CER channel adapter state
	8000	Attention
	4000	Status modifier
	2000	Control unit end
	1000	Busy
	0800	Channel end
	0400	Device end
	0200	Unit check
	0100	Unit exception
CABSENSE		CA sense byte
	1	Command reject
	. 1	Intervention required
	. . 1	Bus out check
	. . . 1	Equipment check
	. . . . 1 . . .	Data check
	. . . . . 1 . .	Overrun
	. . . . . 1 .	Not initialized
	 1	Program abort
SENSE 1		Extended sense byte 1
	1	Dump complete
	. 1	Imprecise data check
	. . 1	Resetting event
	. . . 1	Device characteristics change

Table 12-60 (Page 2 of 2). MOSS BER Type 10 ID B9 Field Details

Field Name	Bit pattern or Hex value	Meaning
ABORT REASON		CAB abort reason codes
	01	Initialized state. Not defined as CA line
	02	Initialized state. EP only line
	03	Initialized and concacted state CA line
	04	Initialized and concacted state CA line
	10	FID4 concacted state
	11	FID2 concacted state
	12	Contact pending state
	13	Contact pending state
	30	Discontacted or ANS in progress
	31	Write start received during XID exchange
	32	XID proc failed to complete within ATO limit
	33	Read start received during XID exchange
	34	Read XID received out of sequence
	35	Unexpected contact channel Cmd received
	36	Contact channel Cmd received out of sequence
	37	Discontact channel Cmd received
	38	PRI received and ANS invoked
	39	XID received on channel link
	3A	Station on channel link in contact/discontact state
	40	Inbound transfer while ANS in progress
	41	Bus out check W/ANS in progress
	42	Equipment check W/ANS in progress
	43	Inbound transfer data streaming timeout
	44	Inbound transfer W/ANS in progress
	45	Channel stop or HIO received during read Cmd
	46	Inbound transfer data streaming timeout
	47	XID NEG. failed, ANS invoqued
	50	XID3 received W/length error
	51	XID3 received W/CV22 appened
	60	PIU received while not FID4 contacted
	61	PIU received while not FID2 contacted
DATA REASON		Data check reason code
	01	Unrecognizable XID Type
	02	Received XID2 length incorrect
	03	PIU can not be routed to INN path control
	04	PIU can not be routed to BNN path control
	05	Transfer count exceeded
	06	LH validation failed
	07	Set blocking delay LH length invalid
	08	Invalid LH function code
	0A	Input data buffer was empty
	0B	Channel stop occurred
CMD REJ REASON		Command reject reason code
	01	Channel Cmd Decoder did not recognize the Cmd code as valid
	02	MOSS failed to acknowledge write IPL Cmd in time to avoid equipemnt check
	03	Incorrect XID channel Cmd sequence unexpected read XID
	04	RCD command received over an invalid type of CA

CA BER Type 10 - Formats

Format f0C1

IDs: 18, 1C, 1E, 80, 97, 9B	
Bytes	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35-36	X76
37-38	I
39-42	LAR
43-44	X75
45-46	X76U
47-48	ETA
49	Unused
50	Adno
51	Flag
52	CAVT
53-54	SWA error register
55	Unused
56-58	IAR int level
59-60	TA
61-62	TD
63-68	Unused
63-64	X8 ◄┐ for
65-66	X9 ◄┘ ID 80/9B
67-68	XA ◄
69-70	X50 (*)
71-72	X51 (*)
73-74	X52 (*)
75-122	CAB (*)
123-124	(CAC)
125-150	CA Regs X'0'-X'F'

Format foC2

IDs 14, 16, 91, 9A	
Bytes	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35-36	X76
37-38	X75
39-40	Unused
41-42	ETA
43-44	Unused
45-46	X76U
47-50	FPR
51	Flag
52	Unused
53-54	SWA
55-68	Unused
69-70	X50 (*)
71-72	X51 (*)
73-74	X52 (*)
75-122	CAB (*)
123-124	CAC (*)
125-150	CA regs X'0'-X'F' (*)

(*) means that if contents are FEFEFE...FE, data is invalid.

Figure 12-27 (Part 1 of 3). CA BER Formats

Format foC3

IDs:10 1B 1F 87 90 92 93 94 96 98 99 9C 9D 9E 9F

Bytes	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35-36	X76
37	ADNO
38	Unused
39-42	LAR
43-44	Unused
45-46	X76U
47-48	TA
49-50	Unused
51	Flag
52	Unused
53-54	SWA
55-68	Unused
67-68	X60 ID=9D/1F
69-70	X50 (*)
71-72	X51 (*)
73-74	X52 (*)
75-76	N/A
77-124	CAB (*)
125-126	CAC
127-152	CA Regs X'0'-X'F'

Format foC4

IDs: 34 35 B1 B2 B5 B6 BD BE

Bytes	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X77
35-36	X7F
37-38	X0
39-40	X1
41-42	X2
43-44	X3
45-46	X4
47-48	X5
49-50	X6
51-52	X7
53-54	XB
55-56	XC
57-58	XF
59-106	CAB/CHCB
107-108	CAC
109	TA
110	Unused (F for B5)
111	Flag

(*) means that if contents are FEFEFE...FE, data is invalid.

Figure 12-27 (Part 2 of 3). CA BER Formats

Format f0C5

IDs: 81 to 84	
Bytes	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35-36	X76
37-38	I 0 for IDs 81/82
39-42	LAR
43-44	X75 0 for IDs 83/84
45-46	X76U
47-48	ETA
49	Unused
50	ADNO
51	Flag
52	CAVT
53-54	SWA
56-58	IAR 0 for IDs 81/82
59-60	TA
61-62	TD
Only for IDs 81,83 (0 for 82,84)	
63-64	X'08'
65-66	STAT
67-68	X'0E'
69-70	X'0F'
71-74	FPR
75-122	CAB

Format foC6

IDs: B3 B7 B8 BA BB BC	
Bytes	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X77
35-36	X7F
37-38	STATUS
39-40	CCU-INPUT X57
41-42	CCU-OUTPUT X57
43	TA
44	CAVT
45-46	X0F

Format foC7

IDs: B9	
Bytes	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X77
35-36	X7F
37-38	STATUS
39-40	X00
41-42	X02
43	TA
44	CAVT
45-46	X0F
47-48	X06
49	Command
50	CABSENSE
51	SENSE1
52	SENSE2
53	Abort reason
54	Data check reason
55	CMD reject reason
56	Equip check reason

Format foC8

IDs: 85 86 88 89 BF	
Bytes	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35-36	X76
37	ADNO
38	CAVT
39-42	LAR
43-44	TA
45-46	76U
47	F
48	Unused
49-50	SWA
51-52	CCU-INPUT X57
53-54	CCU-OUTPUT X57
55-60	CA Reg XD to XF

Figure 12-27 (Part 3 of 3). CA BER Formats

NCP TSS/HPTSS BER Type 11

TSS/HPTSS BER Type 11 - Summary

Table 12-61 (Page 1 of 5). TSS/HPTSS BER Type 11 Summary

BER ID	ABEND Code (NCP)	Event Description	Recovery or PGM Action	ALERT	ALARM
14	0930	LSS/HSSyy AIO Address Exception Check IOC error LVL1 with: LVL1 summary register X7E = '0100' (IOC-1) or '0001' (IOC-2) with IOC LVL1 register X76 = '8200' (IOC-1) or '0082' (IOC-2)	NCP re-IPL	NO	NO
16	0931	LSS/HSSyy AIO Storage Protect Check IOC Error LVL1 with: LVL1 Summary Register X7E = '0100' (IOC-1) or '0001' (IOC-2) with IOC LVL1 Register X76 = '4200' (IOC-1) or '0042' (IOC-2)	NCP re-IPL	NO	NO
18	0	LSS/HSSyy IOH/IOHI to Adapter not attached IOC Error LVL1 with: LVL1 Summary Register X7E = '0100' (IOC-1) or '0001' (IOC-2) with IOC LVL1 Register X76 = '2800' (IOC-1) or '0028' (IOC-2) For adapter address in TA, the CDS shows the adapter not attached.		NO	NO
1B	0933	LSS/HSSyy Invalid Input IOH IOC Error LVL1 with: LVL1 Summary Register X7E = '0100' (IOC-1) or '0001' (IOC-2) with IOC LVL1 Register X76 = '5800' (IOC-1) or '0058' (IOC-2) LAS (line adapter status) bit 1.7 is On.	NCP re-IPL	NO	NO
1C	0	Line command reject Error status type 3 of CSP, bit 1.0 = 1 See details on Figure 12-8 on page 12-12	Line down	43	43
1E	0	LSS/HSSyy Invalid Output IOH to Adapter Adapter LVL1 with: LVL1 Summary Register X7E = '2000' (IOC-1) or '0200' (IOC-2) with Adapter Status Register (Error Status Type 3 non-Hardstop) or LAS = B'1000 000u 0100 0000' as Invalid Output IOH for which the related PIO terminated correctly (no IOC error LVL1) but the adapter microcode rejects the Output IOH by raising this current adapter LVL1. 'u' = '1' means adapter disconnected due to NCP command 'F2'.	LSS/HSS down	60	60

Table 12-61 (Page 2 of 5). TSS/HPTSS BER Type 11 Summary

BER ID	ABEND Code (NCP)	Event Description	Recovery or PGM Action	ALERT	ALARM
26		HSSyy Portx SCTL/DMA Storage Protect or Address Exception Adapter LVL2 with: PSA LCS (Line Control Status) = 'DC' as any DMA type error PSA HELCS (High byte of Extended LCS) = '10' as specifically SP/AE	Line down HSS down	73	73
91	0	LSS/HSSyy AIO Error IOC Error LVL1 with: LVL1 Summary Register X7E = '0100' (IOC-1) or '0001' (IOC-2) with IOC LVL1 Register X76 = 'uV00' (IOC-1) or '00uV' (IOC-2) with AIO CCW Register X75H or X75L = B'1nnn n000' where nnnn from 0 to 15 represents the IOC relative adapter number, adapter which was performing the AIO, AIO (Adapter Initiated Operation / Cycle Steal) failing in Time-Out (V='A') or in Bus-In parity Check (V='6') with 'u' giving the time when the operation failed (refer to page 2-37).	TSS/HPTSS µcode retry	63	63
92	0	LSS/HSSyy Unresolved AIO Error IOC Error LVL1 with: LVL1 Summary Register X7E = '0100' (IOC-1) or '0001' (IOC-2) with IOC LVL1 Register X76 = 'uV00' (IOC-1) or '00uV' (IOC-2) with AIO CCW Register X75H or X75L = B'1nnn n000' where nnnn from 0 to 15 represents the IOC relative adapter number, adapter which was performing the AIO, but as opposed to previous BER 11 91, V='2' only (not 'A' or '6').	TSS/HPTSS µcode retry	NO	NO
92	0	Scanner AIO error unresolved (limit threshold)	LSS/HSS down	63	63
93	0	LSS/HSSyy AIO Invalid CSCW IOC Error LVL1 with: LVL1 Summary Register X7E = '0100' (IOC-1) or '0001' (IOC-2) with IOC LVL1 Register X76 = '2200' (IOC-1) or '0022' (IOC-2) AIO CCW register X75H or X75L = B'1nnn n000' where nnnn from 0 to 15 represents the IOC relative adapter number, adapter which was performing the AIO.	TSS/HPTSS µcode retry	NO	NO
93	0	Scanner AIO invalid CSCW (limit threshold)	LSS/HSS down	63	63

Table 12-61 (Page 3 of 5). TSS/HPTSS BER Type 11 Summary

BER ID	ABEND Code (NCP)	Event Description	Recovery or PGM Action	ALERT	ALARM
94		LSS/HSSyy Portx Cycle Steal Error on Set Mode Adapter LVL1 with: LVL1 Summary Register X7E = '2000' (IOC-1) or '0200' (IOC-2) Adapter Status Register (Error Status Type 3 non-Hardstop) or LAS = B'1000 0000 10xx xxxz' (almost identical to BER 11 1C as Command Reject on line interface address 'xxxxxz') but NCP looks at the SLI bit in the LNVT: if ON (Set LNVT Initial required) and if adapter command-reject status = '10xx xxxx xxxx xxxx' then NCP will generate this BER 11 94 instead of BER 11 1C.		43	43
95	0	LSS/HSSyy Adapter LVL1 Hardcheck Adapter LVL1 with: LVL1 Summary Register X7E = '2000' (IOC-1) or '0200' (IOC-2) with Adapter Status Register (Error Status Type 3 Hardstop) or LAS = B'0000 0uuu uuuu uu00' where the string 'uu..uu' reflects the hardware checkers which have been raised (u=1), as several can occur simultaneously in some cases of failure (refer to page 4-201).	LSS/HSS down	63	63
96	0	LSS/HSSyy Adapter Disconnected by operator Adapter LVL1 with: LVL1 Summary Register X7E = '2000' (IOC-1) or '0200' (IOC-2) with Adapter Status Register (Error Status Type 3 non-Hardstop) or LAS = B'1000 0001 0000 0000', meaning "adapter put in disconnect mode" on MOSS operator's request.	Scanner OFF line	B8	B8
96	0	HPTSS disconnected on manual request (following request from MOSS) • X'7E' bit 0.2 or 0.6 ON • Error status type 3, bit 0.7 ON • Ext register X'01' bit 5 ON	Scanner OFF line	BA	BA
97	0	LSS/HSSyy PIO Error IOC Error LVL1 with: LVL1 Summary Register X7E = '0100' (IOC-1) or '0001' (IOC-2) with IOC LVL1 Register X76 = 'uV00' (IOC-1) or '00uV' (IOC-2) as PIO (Program Initiated Operation) failing in Time-Out (V='8') or in Bus-In parity Check (V='4') with 'u' giving the time when the operation failed (refer to page 2-37).	NCP retry	NO	NO
97	0	Scanner PIO error-output IOH/IOHI before threshold. BER field line adapter address = error status type 1 of CSP. See page 4-198.	LSS/HSS down	63	63
98	0	Scanner PIO error-output IOH/IOHI (limit threshold). BER field line adapter address = error status type 1 of CSP. See page 4-198.	LSS/HSS down	63	63

Table 12-61 (Page 4 of 5). TSS/HPTSS BER Type 11 Summary

BER ID	ABEND Code (NCP)	Event Description	Recovery or PGM Action	ALERT	ALARM
99	0	LSS/HSSyy Adapter LVL1 non-Hardcheck Adapter LVL1 with: LVL1 Summary Register X7E = '2000' (IOC-1) or '0200' (IOC-2) with Adapter Status Register (Error Status Type 3 non-Hardstop) or LAS = B'1iii 0uu0 0000 000v' where 'iii' (invalid interrupt level from 0 to 7) and 'u' are checkers raised by Mcode and 'v' by hardware (refer to page 4-200).	LSS/HSS down	63	63
9A	0	Scanner adapter error unresolved • First get error status failed but retry was successful. • Error status has value at time of failure.	NCP retry	NO	NO
9B	0	Interrupt from disconnected scanner Level 1 interrupt presented to NCP/PEP while the scanner is disconnected (X'01' bit 5 ON). X'7E' bit 0.2 or 0.6 ON		NO	NO
9B	093A	Interrupt from disconnected scanner (limit threshold)	NCP re-IPL	NO	NO
9C	0	Adapter PIO error on broadcast "get line ID" IOH command Adapter was the answering one at failure time.	None	NO	NO
9C	0	Adapter PIO error on broadcast "get line ID" IOH command Adapter was the answering one at failure time. (threshold)	Adapter down	63	63
9D	0	Scanner microcode error. CSP error status M has cause of error. BER field line adapter status = Status M is an error code (for PE only).	LSS/HSS down	63	63
9E	0	Get error status command failed (IOC error) during NCP LVL1 process on Line Adapter LVL1 or on PIO Get Line ID error.		NO	NO
A1	0	Unresolved level 2 interrupt. If spurious retry count (the interrupt occurred on a non-defined line)		NO	NO
A1	0936	Unresolved level 2 interrupt (limit threshold) See Specific Mechanism, page 12-14	NCP re-IPL	NO	NO
A2	0	Internal FESL error reported via level 2 • LCS = C0, C2, C4, C6, C8, D0, D2, D4, D6, D8	Line down	43	43
A2	0	Internal FESH error reported via level 2 • LCS = C0, C2, C4, C6, C8, D0, D2, D4, or D8	Line down	43	43
A2	0	Internal FESH error reported via level 2 • LCS = CE. Local clock failure.	Line down	43	43
A3	0	Internal MUX error reported via level 2 • LCS = CA	Line down	43	43
A3	0	Internal MUX/LIC error reported via level 2 • LCS = CC.	Line down	43	43
A3	0	Internal LIC error reported via level 2 • LIC failing or not plugged. • LCS = CE.	Line down	43	43

Table 12-61 (Page 5 of 5). TSS/HPTSS BER Type 11 Summary

BER ID	ABEND Code (NCP)	Event Description	Recovery or PGM Action	ALERT	ALARM
A3	0	Internal LIC error reported via level 2 • Line cannot be accessed by configuration. • LCS = DE.	Line down	43	43
A4	0	Time out on any command, except F5. F5 command sent to the scanner, back up timer in NCP/PEP level 3 expired before receiving level 2 from scanner to process it. See Specific mechanism, Figure 12-9 on page 12-12	Line down	NO	NO
A4	0	Transient FESL/MUX error reported at level 2, ELCS bit 7 ON	TSS μcode retry	NO	NO
A5	0	Transient LIC error reported at level 2, ELCS bit 7 OFF	TSS μcode retry	NO	NO
A6	0	SCTL/DMA internal error, if twin SBY or BU LCS = 'DC' • ELCS bits 4,5,6 = 001	Line down	73	73
A6	0	SCTL/DMA internal error, if single or dual • LCS = 'DC' • ELCS bits 4,5,6 = 001	Line down	73	73
A7	0	Switch/SCTL/DMA interface (main bus) error • LCS = 'DC' • ELCS bits 4,5,6 = 010	Line down	73	73
A8	0	Switch/DMA reported error • LCS = 'DC' • ELCS bits 4,5,6 = 011	Line down	73	73
A9	0	Switch/DMA parity check or DMA time out • LCS = 'DC' • ELCS bits 4,5,6 = 100	Line down	73	73
AA	0	FESH/DMA interface error • LCS = 'DC' • ELCS bits 4,5,6 = 101	Line down	73	73
AB		Internal LIC error level 2 (LIC5 and LIC6)	Line down	43	43
B1	0	Scanner command time out on F5. Command F5 sent to the scanner, back up timer in NCP/PEP level 3 expired before receiving level 2 from scanner to process it. See Specific mechanism, Figure 12-9 on page 12-12	Line down	43	43

Note: In case of abend, NCP re-IPL is performed and an Alarm/Alert is generated when IPL is completed. Alert is triggered by MOSS BER 01 ID 06, error code 05.

TSS/HPTSS BER Type 11 - Detailed BER Display

TSS/HPTSS BER Type 11 - ID 14, 16, 91, 92, 93: Format foT1, see page 12-206. Program level 1 generates one of the following BERs when an error occurs during an AIO operation on a scanner.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:11 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                             <REF. CODE IN CHAR.> CCCCCCCC

F:bbbbbbbb
X7E:hhhh  X76:hhhh  X75:hhhh  ETA:hhhh  LAS:hhhh  X76U:hhhh  SPR:hhhhhhhh
SWA:hhhh  LAR:hhhhhhhh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

TSS/HPTSS BER Type 11 - IDs 18, 1B, 97, 98, 9C, 9E: Format foT2, see page 12-206. Program level 1 generates one of these BERs when an error occurs during a PIO operation on a scanner.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:11 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                             <REF. CODE IN CHAR.> CCCCCCCC

F:bbbbbbbb X7E:hhhh X76:hhhh I:hhhh LAR:hhhhhhhh
LAS:hhhh X76U:hhhh ETA:hhhh SWA:hhhh IAR:hhhhhh TA:hhhhh TD:hhhh
IOB/LXB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
        hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
CCB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
    hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
AXB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhh hh
SCB:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hh
PSA:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

TSS/HPTSS BER Type 11 - IDs 1E, 95, 96, 99, 9A, 9B, 9D: Format foT3, see page 12-206. Program level 1 generates one of these BERs when an error is reported by a scanner on level 1.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:11 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                            <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
X7E:hhhh X76:hhhh ADNO:hh LAS:hhhh X76U:hhhh SWA:hhhh LAR:hhhhhhhh









===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

TSS/HPTSS BER Type 11 - ID A1: Format foT4, see page 12-207. These BERs are generated on a LVL2 unresolved interrupt.

```
                              ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:11 ID:hh<LOST:ddd CP-ABEND:hhhh>
<Error description>                            <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
TA:hh  TD:hh  NW:hhhh  IDR:hhhh  LNVT:hhhhhhhh  LCS:hh
PSA:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
CNT:hhhh

OVERRIDE FLAG WITH NEW HEXADECIMAL VALUE
===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

TSS/HPTSS BER Type 11 - ID B1: Format foT5, see page 12-207. These BERs are generated on a LVL2 time out.

```
                              ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:11 ID:hh<LOST:ddd CP-ABEND:hhhh>
<Error description>                            <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
TA:hh  TD:hh  NW:hhhh
PSA:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh

OVERRIDE FLAG WITH NEW HEXADECIMAL VALUE
===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

TSS/HPTSS BER Type 11 ID 26, A2, A3, A4, A5, A6, A7, A8, A9, AA, AB: Format foT5, see page 12-207. Program level 2 generates one of these BERs when a scanner internal error or a transient line error is detected.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:11 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb TA:hh TD:hh NW:hhhh IDR:hhhh
PSA:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
IOB/LXB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
        hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
CCB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
    hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
AXB:hhhh hhhh hhhh hhhh hhhh hhhh hhhh
SAT:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hh
SCB:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hh
CSC:hhhh CNT:hhhh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Note: Lost and CP abend fields are displayed when applicable.

TSS/HPTSS BER Type 11 ID 94, 1C: Format foT6, see page 12-207. Program level 1 generates this BER when a command reject is reported by a scanner on level 1 (control program error).

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:11 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb LNVT:hhhh PSA:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
SCF:hh LSTAT:hh LAS:hhhh CR1:hh CR2:hh IAR:hhhhhhhh TA:hh TD:hh
IOB/LXB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
        hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
CCB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
    hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
AXB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhh  hh
SCB:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

TSS/HPTSS BER Type 11 - Field Description

Table 12-62 (Page 1 of 2). TSS/HPTSS BER Type 11 Field Description

Field Name	Meaning	Refer to
ADNO	CS number (decimal) in error description field. This CS number is derived from: • field TA for PIO operation – for CS error reported at level 2 – for CA error reported at level 3. • field X75 for AIO operation. • field CSPA for CS error reported at level 1. If no n is specified (blank CS), problem isolation by program was not possible.	
LAS or L-STAT	LA adapter status • LA Error Status Type 1: CSP error status 1 • LA Error Status Type 2: CSP error status 2 • LA Error Status Type 3/H: CSP error status 3	page 4-198
CSPA	CSP address used by NCP/PEP (see CSn and LINEnn).	page 4-18
ETA	TA field of IOH failure in level 1.	page 4-103
IDR	Get line ID response.	Chapter 4
F	Indicator flag (indicates a byte expansion follows)	(*)
SWA	Switch adapter error register.	page 3-23
CR1	First command sent to scanner	
CR2	Second command sent to scanner	
LAR	Lagging address register	page 2-44
SPR	LA shared pointer register X'3F' or X'6F'.	
CSC	Configuration status control flag (contains X'FFFF' for PEP, BSC/SS and BNN lines).	
CNT	Repetition count (BER flooding). Number of times the BER appeared.	
SCF	Secondary Control Field.	
I	First two bytes of instruction.	
IAR	IAR of interrupt level.	
LCS	Line communication status.	page 6-35
LINEnn	Line number (0 to 31) within the CS (in error description line).	
LNVT	Line vector table.	page 4-101
LOST	Lost record count (LRC).	(*)
NW	Network address (NCP) or CA number and ESC (PEP).	(*)
IOB/LXB	X'24' bytes of LXB (for SDLC lines) or IOB (for BSC/SS lines) control blocks. This area is padded with X'FF' for PEP.	(*)
CCB	X'40' bytes of data from the CCB control block. • If PEP, the fields are CCBL2 through CCBPOLL inclusive. • If PEP, the fields are CCBTROPT through CCBXPTR inclusive.	(*)
AXB ACB TRACE	X'E' bytes of data from the AXB control block from AXBFCTL through AXB+X'15' (ACB trace area). For PEP, this area contains the CCB extension starting at the PEP CCB + X'60'.	(*)
AXB PSA	X'11' bytes of data from the PSA trace area of the AXB control block (AXBASSCF through AXBTROFF). For PEP, this area contains the remaining portion of the CCB extension padded with X'F'.	(*)

Table 12-62 (Page 2 of 2). TSS/HPTSS BER Type 11 Field Description

Field Name	Meaning	Refer to
SCB	X'19' bytes of the SCB/CUB from SCBSSCF (CUBSSCF) through SCBRTCNT (CUBRTCNT) inclusively. For BSC/SS lines and for PEP, this area is padded with X'FF's.	(*)
SAT	17 bytes of PSA trace area for NCP.For PEP, this area contains the EP CCB extension.	(*)
SCBCSCF	Configuration station control flags (NCP only).	(*)
PSA	Parameter area (16 bytes)-status area (12 bytes). The byte contents of the PSA depend on the current command (CCMD).	(*)
TA	IOH/IOHI image (TA: hh means TA data byte 0) (see CSn and LINEnn).	page 4-103
TD	IOH/IOHI image -- TD data adapter specific bytes (TD: hh means TD data byte 1).	page 4-103
X3F	CSP shared pointer register.	page 2-24
X74	X'74' - LAR bytes (See CSn and LINEnn).	page 2-31
X75	X'75' - Cycle steal control word register.	page 2-31
X76	X'76' - IOC error summary register.	page 2-31
X76U	X'76' - Cause of error not found (PIO to read error register failed).	page 2-31
X79	X'79' - Interrupt level.	page 2-31
X7E	X'7E' - CCU level 1 interrupt.	page 2-31
X7F	X'7F' - Interrupt request register CCU levels 2, 3, and 4	page 2-31

Note: All values are in hexadecimal notation (X'0' to X'F'), except for:

- Flag bytes F and CS STAT, which are in bit format (8 or 16 bits, 0 or 1)
- The error description line with a CS number and LINE number, which are in decimal notation.

(*) For software information on BERs originated by NCP/PEP, refer to the associated product documentation.

TSS/HPTSS BER Type 11 - Formats

Format: foT1

ID: 14 16 91 92 93	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35-36	X76
37-38	X75
39-40	Unused
41-42	ETA
43-44	LAS
45-46	X76U
47-50	SPR
51	Flag
52	Unused
53-54	SWA
55-58	LAR

Format: foT2

IDs: 18 1B 97 98 9C 9E	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35-36	X76
37-38	I
39-42	LAR
43-44	LAS
45-46	X76U
47-48	ETA
49-50	Unused
51	Flag
52	Unused
53-54	SWA
55	INTLVL
56-58	IAR
59-60	TA
61-62	TD
63-66	Unused
67-102	IOB/LXB
103-166	CCB
167-198	AXB
199-215	SCB
216	Unused
217-244	PSA

Figure 12-28 (Part 1 of 2). TSS/HPTSS BER Formats

Format: foT3

ID: 1E 95 96 99 9A 9B 9D

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35-36	X76
37	ADNO
38-42	Unused
43-44	LAS
45-46	X76U
47-50	Unused
51	F
52	TSS Flag
53-54	SWA
55-58	LAR
59-66	Unused
67-102	LBX
103-166	CCB
167-182	ATT
183-198	PSA Trace

Format: foT4

ID: A1

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33	F
34	Unused
35-36	IDR
37-64	PSA (56 = LCS)
65	TA byte 0
66	TD byte 1
67-68	NW
69-72	LNVT
73-108	IOB/LXB
109-172	CCB
173-186	AXB trace
187-203	SAT trace
204-219	SCB
220	SCBCSCF
221-222	Count

Format: foT5

IDs: 26 A2 A3 A4 A5 A6 A7 A8 A9 AA AB B1

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33	Flag
34	Unused
35-36	IDR
37-64	PSA
65	TA byte 0
66	TD byte 1
67-68	NW
69-104	IOB/LXB
105-168	CCB
169-182	AXB (IOB)
183-199	SAT trace
200-215	SCB
216	CSC
217-218	Count (Only for A2, A4, and AB)

Format: foT6

ID: 94 1C

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33	F
34	Interrupt level 1
35-36	LNVT
37-52	PSA
53	SCF
54	LSTAT
55-56	LAS
57	CR1
58	CR2
59-62	IAR
63-64	Unused
65	TA
66	TD
67-102	LXB/IOB
103-166	CCB
167-197	AXB
198	Unused
199-215	SCB
216	Unused

Figure 12-28 (Part 2 of 2). TSS/HPTSS BER Formats

NCP/PEP BER, Type 12

NCP/PEP BER Type 12 Summary

The following BERs are software errors detected by the CCU hardware. Software errors detected by software checking mechanisms (logical errors) lead to Control Program abends.

Table 12-63. NCP/PEP BER Type 12 Summary

BER ID	ABEND Code (NCP)	Event Description	Recovery or PGM Action	ALERT	ALARM
11	000A	IN/OUT or IOH/IOHI on level 5. IAR not 0, retry not possible.	NCP re-IPL	NO	NO
12	001B	Invalid operation code • X'7E' bit 0.4 ON	NCP re-IPL	NO	NO
13	0950	Address exception - I fetch • X'7E' bit 1.1 ON	NCP re-IPL	NO	NO
14	0951	Address exception - I execution • X'7E' bit 1.3 ON	NCP re-IPL	NO	NO
15	0952	Storage protect - I fetch • IAR not 0 • X'7E' bit 1.2 ON	NCP re-IPL	NO	NO
16	0953	Storage protect - I execution • X'7E' bit 1.4 ON	NCP re-IPL	NO	NO
17	0954	Level 5 branch to storage location 0. IAR = 0.	NCP re-IPL	NO	NO
18	0955	User (non NCP code) branch to storage location 0. IAR = 0.	NCP re-IPL	NO	NO
19	000E	Logic error (interrupt reason lost). Program check in level 1.	NCP re-IPL	NO	NO
21	0	Level 2 PCI. The level 2 PCI should be OFF because level 1 has reset it (X'77' bit 0.7). If it is ON (hot level 2 PCI), or if spurious retry count from a PCI level 2 interrupt.		NO	NO
21	0956	Level 2 PCI (limit threshold)	NCP re-IPL	NO	NO

Note: In case of abend, NCP re-IPL is performed and the alarm/alert is generated when IPL is completed. Alert is triggered by MOSS BER ID 06, error code 05.

NCP/PEP BER Type 12 - Detailed BER Display

NCP/PEP BER Type 12 - IDs 11 through 19: Format foN1, see page 12-210. Program level 1 generates one of these BERs when an NCP/PEP program exception occurs.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:hh ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC

X7E:hhhh  X74:hhhhhh  X79:hh  IAR:hhhhhh  I:hhhh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

NCP/PEP BER Type 12 - ID 21: Format foN2, see page 12-210. Program level 1 generates one of these BERs when a program-controlled interrupt request at level 2 remains unresolved.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:hh ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC

X7F:hhhh  IAR3:hhhhhhhh  IAR4:hhhhhhhh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

NCP/PEP BER Type 12 - Field Description

Table 12-64. NCP/PEP BER Type 12 Field Description

Field Name	Meaning	Refer to
I	First two bytes of instruction.	-
IAR	IAR of interrupt level.	page 2-24
IAR3	IAR contents of level 3.	page 2-24
IAR4	IAR contents of level 4.	page 2-24
X74	X'74' - Lagging address register.	page 2-31
X79	X'79' - Byte 1 interrupted levels.	page 2-31
X7F	X'7F' - Interrupt request reg - CCU lvls 2, 3, and 4.	page 2-31

Note: All values are in hexadecimal notation (X'0' to X'F').

NCP/PEP BER Type 12 - Formats

Format: foN1

IDs: 11 to 19

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35	Unused
36-38	X74
39	X79, byte 1
40-42	IAR
43-44	I

Format: foN2

ID: 21

Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7F
35-38	IAR3
39-42	IAR4

Figure 12-29. NCP/PEP BER Formats

NCP CCU BER Type 13

CCU BER Type 13 - Summary

Table 12-65 (Page 1 of 2). CCU BER Type 13 Summary

BER ID	ABEND Code (NCP)	Event Description	Recovery or PGM Action	ALERT	ALARM
32	0	Level 3 interrupt configuration check • Invalid level 3 interrupt (for example, CA interrupt on a link-attached single box • or no CA on CCU are switched or installed on a twin box).		NO	NO
32	0978	Level 3 interrupt configuration check (limit threshold)	NCP re-IPL	NO	NO
91	0	Unresolved Lvl 1 interrupt, no bit in CA register X'E'.		NO	NO
91	0970	Unresolved level 1 interrupt (limit threshold)	NCP re-IPL	NO	NO
92	0971	Unresolved interrupted level when requested Interrupt level not 2, 3, 4, 5 as per contents of X'79' bits 1.0, 1.1, 1.2, 1.3.	NCP re-IPL	NO	NO
93	0972	Unexpected CCU hardcheck (CCU should have stopped) • Not possible to reset X'77', bit 0.1, or • MOSS has not reset this bit after IPL.	NCP re-IPL	NO	NO
94	0973	Unexpected IPL request • Not possible to reset X'77' bit 0.0, or • MOSS has not reset this bit after IPL.	NCP re-IPL	NO	NO
95	0971	Invalid level 1 interrupted IAR (IN X'79')	NCP re-IPL	NO	NO
B1	0	Unresolved level 3 interrupt. NCP reading out X'77' does not find bit 1.0 ON (CA level 3) and X'7F' bits 0.2, 0.6, 1.5 and 1.6 ON (level 3 raised by MOSS diag, user, timer or PCI).		NO	NO
B1	0974	Unresolved level 3 interrupt (limit threshold	NCP re-IPL	NO	NO
C1	0	Unresolved level 4 interrupt. NCP reading out X'7F' does not find bits 0.3, 0.4, 0.7 and 1.7 ON (level 4 interrupt raised by MOSS request SVC, MOSS response SVC, PCI or SVC).		NO	NO
C1	0975	Unresolved level 4 interrupt (limit threshold)	NCP re-IPL	NO	NO
C2	0	Unresolved level 4 PCI interrupt • Level 4 PCI (X'7F' bit 0.7) and not wait state, but no bytes are set in level 4 control block of NCP. • Mask used to set interrupt does not indicate release, slowdown, dispatcher request • SVC interrupt, or mask indicates wait state plus MOSS offline, outmail box, CRP request for MOSS transfer, or MOSS request.		NO	NO
C2	0976	Unresolved level 4 PCI interrupt (limit threshold)	NCP re-IPL	NO	NO
C3	0	Hot/spurious level 4 PCI. Level 4 PCI latch (X'7F' bit 0.7) does not go OFF, after a reset by output X'77' bit 1.6		NO	NO
C3	0977	Hot/spurious level 4 PCI (limit threshold)	NCP re-IPL	NO	NO

Table 12-65 (Page 2 of 2). CCU BER Type 13 Summary

BER ID	ABEND Code (NCP)	Event Description	Recovery or PGM Action	ALERT	ALARM
C4	0979	Unresolved level 4 SVC interrupt. Level 4 SVC interrupt (X'7F' bit 1.7) but CCU is in wait state. Abend if hot SVC interrupt (X'7F' bit 1.7 still ON after reset latch by Out X'77' bit 1.7).	NCP re-IPL	NO	NO
C5	0	Continuous/unresolved MOSS level 4 request. (X'7F' bit 0.3 still ON after reset latch by Out X'77' bit 0.4).		NO	NO
C5	097A	Continuous/unresolved MOSS level 4 request (limit threshold)	NCP re-IPL	NO	NO
C6	0	Continuous/unresolved MOSS level 4 status (X'7F' bit 0.4 still on after reset latch by Out X'77' bit 0.5).		NO	NO
C6	097B	Continuous/unresolved MOSS level 4 status (limit threshold)	NCP re-IPL	NO	NO

Note: In case of abend, NCP re-IPL is performed and the Alarm/Alert is generated when IPL is completed. Alert is triggered by MOSS BER ID 06, error code 05.

CCU BER Type 13 - Detailed BER Display

CCU BER Type 13 - IDs 32, B1: Format foU1, see page 12-214. BER generated by program level 3.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:13 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC

X77:hhhh  X7F:hhhh  X0:hhhh X1:hhhh  X2:hhhh  X3:hhhh  X4:hhhh  X5:hhhh
 X6:hhhh   X7:hhhh  XB:hhhh XC:hhhh  XF:hhhh
 XD:hhhh   XE:hhhh  X0:hhhh X1:hhhh  X2:hhhh
 X3:hhhh   X4:hhhh  X5:hhhh X6:hhhh  X7:hhhh
 XB:hhhh   XC:hhhh  XD:hhhh XE:hhhh  XF:hhhh
 TA:hhhh   CCU-INPUT-X57:hhhh CCU-OUTPUT-X57:hhhh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

Note: Two sets of registers: the first for IOC1, the second for IOC2.

CCU BER Type 13 - IDs 91, 92, 93, 94, and 95: Format foU2, see page 12-214. This ID indicates an unresolved level 1 interrupt.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:13 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                            <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
X7E:hhhh  X74:hhhhhh  X79:hh  IAR:hhhhhh  X7D:hhhh
CCU-INPUT-X57:hhhh    CCU-OUTPUT-X57:hhhh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

CCU BER Type 13 - IDs C1 to C6: Format foU3, see page 12-214. This ID indicates an unresolved level 4 interrupt.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:13 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                            <REFER.CODE IN CHAR.> CCCCCCCC

X77:hhhh  X7F:hhhh  RCB:hhhh hhhh hhhh hhhh
MTF: = 224 bytes for ID C6 only



===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

CCU BER TYPE 13 - Field Description

Table 12-66 (Page 1 of 2). CCU BER Type 13 Field Description

Field Name	Meaning	Refer to
IAR	IAR of interrupt level.	page 2-24
MTF	Mail box trace facility.	
RCB	Level 4 router control block.	page 7-16
X0	X'0' - Channel adapter initial selection register.	page 7-16
X1	X'1' - CA CSCW and subchannel address.	page 7-16
X2	X'2' - Data status register.	page 7-16
X3	X'3' - CA ESC subchannel.	page 7-16
X4	X'4' - CA IOH bytes 1 and 2.	page 7-16
X5	X'5' - CA IOH bytes 3 and 4.	page 7-16
X6	X'6' - CA NSC status register.	page 7-16
X7	X'7' - CA enabled indications.	page 7-16
XB	X'B' - CA ESC TIO address and status.	page 7-16
XC	X'C' - CA AIO operations register.	page 7-16
XD	X'D' - CA error register.	page 7-16
XE	X'E' - CA level 1 interrupt requests.	page 7-16
XF	X'F' - CA level 3 interrupt request and CA number.	page 7-16
X74	X'74' - Cycle steal control word register.	page 2-31
X77	X'77' - Interrupt request reg - adapter lvls 2 and 3.	page 2-31
X79	X'79' - Interrupted level.	page 2-31
X7D	X'7D' - CCU hardcheck register.	page 2-31
X7E	X'7E' - CCU level 1 interrupt.	page 2-31
X7F	X'7F' - Interrupt request reg - CCU lvls 2, 3, and 4.	page 2-31
TA	Tag address	page 7-14
TD	Tag data	page 7-14
CCU INPUT X57	X'57' - Input CA command LS reg	page 12-117

Table 12-66 (Page 2 of 2). CCU BER Type 13 Field Description		
Field Name	**Meaning**	**Refer to**
CCU OUTPUT X57	X'57' - Output CA command LS reg	page 12-117

CCU BER Type 13 - Formats

Format foU1

IDs: 32 B1	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X'77'
35-36	X'7F'
37-62	IOC1 registers X'00'-X'0F'
63-88	IOC2 registers X'00'-X'0F'
89-90	TA
91-92	CCU input X57
93-94	CCU output X57
95	BER Flag

Format foU2

IDs: 91 to 95	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X'7E'
35	Unused
36-38	X74
39	X79
40-42	IAR
43-44	X'7D' CCU hardcheck register
45-46	CCU-input X57
47-48	CCU-output X57
49	BER flag

Format foU3

IDs: C1 to C6	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	CP ABEND
33-34	X'77'
35-36	X'7F'
37-44	RCB
45-46	NTF trace ident.*
47-76	mailbox or status*
77-78	NTF trace ident.*
79-108	mailbox or status*
109-110	NTF trace ident.*
111-140	mailbox or status*
141-142	NTF trace ident.*
143-172	mailbox or status*
173-174	NTF trace ident.*
175-204	mailbox or status*
205-206	NTF trace ident.*
207-236	mailbox or status*
237-238	NTF trace ident.*
239-268	mailbox or status*

* = Only for ID C6

Figure 12-30. CCU BER Formats

NCP IOC BER Type 14

IOC BER Type 14 - Summary

Table 12-67. IOC BER Type 14 Summary

BER ID	ABEND Code (NCP)	Event Description	Recovery or PGM Action	ALERT	ALARM
17		PIO error. IOH or IOHI used by the control program when an invalid TA value of zero.	None	NO	NO
91	0	Unresolved adapter level 1		NO	NO
91	0990	Unresolved adapter level 1 (limit threshold)	NCP re-IPL	NO	NO
92	0	Unresolved AIO level 1. Attempt to cycle steal by undefined LA or CA. X'76' = 1A, 2A, 36, or B6 X'75' = Meaningless		NO	NO
92	0991	Unresolved AIO level 1 (limit threshold)	NCP re-IPL	NO	NO
93	0	Unresolved PIO level 1. PIO error detected by the IOC that was found unresolved (no time out or parity error, in X'76' bits 0.4 and 0.5 or X'76' bits 1.4 and 1.5).		NO	NO
93	0992	Unresolved PIO level 1 (limit threshold)	NCP re-IPL	NO	NO
96	0	Read switch error register failed • X'76' bit 0.4 for IOC1 time out, or • X'76' bit 1.4 for IOC2 time out • X'76' bit 0.5 or 1.5 for bus IN parity error X'76' bits 0.0, 0.1, 0.2, 0.3 or X'76' bits 1.0, 1.1, 1.2, 1.3 contain the IOC internal error status at time of error			
9A	0990	IOC-X Unresolved Adapter LVL1 (threshold) No adapter identified as raising interrupt level 1	NCP abend	NO	E3
9C		IOC-X Unresolved Adapter LVL2 No adapter identified as raising interrupt level 2	None	NO	NO
9C	0937	IOC-X Unresolved Adapter LVL2 (threshold) No adapter identified as raising interrupt level 2	NCP abend	No	E3

Note: In case of abend, NCP re-IPL is performed and the alarm/alert is generated when IPL is completed. Alert is triggered by MOSS BER ID 06, Error code 05.

IOC BER Type 14 - Detailed BER Display

3746-900 BER Type 14 - ID 17: Format fol1, see page 12-217.

```
                              ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:09  ID:hh
  <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
X7E:hhhh LAR:hhhh hhhh INTLVL:hh IAR:hhhhhh X76:hhhh L1BIOHTA:hhhh
L1BIOHTD:hhhh L1XSWADE:hhhh L1BERFLG:hh

===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

All IDs (91, 92, 93, 96): See format fol2, on page 12-217. Program level 1 generates one of these BERs when an error occurs on the IOC bus.

```
                                ELD DETAIL
 SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:10 ID:hh<LOST:ddd CP-ABEND:hhhh>
 <ERROR DESCRIPTION>                              <REFER.CODE IN CHAR.> CCCCCCCC
 F:bbbbbbbb
 X7E:hhhh  X76:hhhh  X75:hhhh X74:hhhhhhhh X76U:hhhh
 SWA:hhhh
 CCU-INPUT-X57:hhhh  CCU-OUTPUT-X57:hhhh


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

3746-900 BER Type 14 - IDs 9A and 9C: Format fol3, see page 12-217.

```
                                ELD DETAIL
SEL# hhh   FLAG hh DATE:dd/dd TIME:dd:dd  TYPE:09  ID:hh
  <ERROR DESCRIPTION>                               <REFER.CODE IN CHAR.> CCCCCCCC
X7E:hhhh LAR:hhhh hhhh INTLVL:hh IAR:hhhhhh X76:hhhh L1BIOHTA:hhhh
L1BIOHTD:hhhh L1BPIO76:hhhh L1XSWADE:hhhh L1BPIOTA:hhhh L1BERFLG:hh

===>

F1:END  F2:MENU2  F3:ALARM  F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

IOC BER Type 14 - Field Description

Table 12-68. IOC BER Type 14 Field Description

Field Name	Meaning	Refer to
IAR	IAR of interrupt level.	page 2-24
INTLVL	Interrupt level	-
LAR	Lagging Address Register (X'74').	page 2-44
L1BERFLG	Box event record flags	page 12-175
L1BIOHTA/ L1BPIOTA	IOHI image -- TA data register (TA: hhhh means data bytes 0 and 1).	page 3-64
L1BIOHTD	IOHI image -- TD data adapter specific bytes (TD: hhhh means data bytes 0 and 1).	-
L1XSWADE	Switch adapter error register.	page 3-23
L1BPIOH76	X'76' - IOC error summary register.	page 2-36
CAB	CAB error register.	(*)
F	Indicator flag byte (byte extention)	(*)
X74	X'74' - Lagging Address Register (LAR) bytes.	page 2-31
X75	X'75' - Cycle steal control word register.	page 2-31
X76	X'76' - IOC error summary register.	page 2-31
X76U	X'76' - Cause of error not found (PIO to read error register failed). See page 12-16	page 2-31
X7E	X'7E' - CCU level 1 interrupt.	page 2-31
SWA	Switch adapter error register.	page 3-23
CCU INPUT-X57	CCU input command LS register (same for OUTPUT)	page 12-117

Note: All values are in hexadecimal format (X'0' to X'F'), except for the flag indicator F, which is in bit format (8 bits, 0 or 1). (*) For software information on BERs originated by NCP/PEP, refer to the associated product documentation.

IOC BER Type 14 - Format

Format: foI1

ID: 17	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	Lost
31-32	Abend
33-34	X7E
35-38	LAR
39	INTVL
40-42	IAR
43-44	X76
45-46	L1BIOHTA
47-48	L1BIOHTD
49-50	Unused
51-52	L1XSWADE
53-54	Unused
55-56	L1BERFLG

Format: foI2

IDs: 91 92 93 96	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	Lost
31-32	Abend
33-34	X7E
35-36	X76
37-38	X75
39-42	X74
43-44	Unused
45-46	X76U
47-48	CCU input X57
49-50	CCU output X57
51	Flag
52	Unused
53-54	SWA

Format: foI3

IDs: 9A 9C	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	Lost
31-32	Abend
33-34	X7E
35-38	LAR
39	INTVL
40-42	IAR
43-44	X76
45-46	L1BIOHTA
47-48	L1BIOHTD
49-50	L1BPIO76
51-52	L1XSWADE
53-54	L1BPIOTA
55-56	L1BERFLG

Figure 12-31. IOC BER Format

NCP TRSS BER Type 15

TRSS BER Type 15 - Summary

Table 12-69 (Page 1 of 3). TRSS BER Type 15 Summary

BER ID	ABEND Code (NCP)	Event Description	Recovery or PGM Action	ALARM/ ALERT
14	0B01	Address exception (AIO) X'76' bit 0.0 or 1.0 ON	NCP re-IPL	NO
16	0B02	Storage protect (AIO) X'76' bit 0.1 or 1.1 ON	NCP re-IPL	NO
18	0	IOH/IOHI to TRM not installed X'7E' bit 0.5 or 1.5 ON IOC bus check in error status type 1 of TRM bit 0.1 and 0.5 on (X'02 bits 0.1 and 0.5)		89
91	0	TRM AIO error • X'75' bit 0.0 or 1.5 ON • X'76' bit 0.4 ON for IOC1 time out or • X'76' bit 1.4 ON for IOC2 time out • X'76' bit 0.5 or 1.5 ON for IOC bus in parity error X'76' bit 0.6 or 1.6 ON in both cases (AIO) • X'76' bits 0.0, 0.1, 0.2, 0.3 or • X'76' bits 1.0, 1.1, 1.2, 1.3 contain the IOC internal status at time of error.	TIC retry	NO
91	0	TRM AIO error (threshold)	TRM down	82
92	0	TRM AIO error unresolved	TIC retry	NO
92	0	TRM AIO error unresolved (limit threshold)	TRM down	82
93	0	TRM AIO invalid CSCW • X'75' bit 0.0 or 1.0 ON • X'76' bits 0.2 and 0.6 or 1.2 and 1.6 ON	TIC retry	NO
93	0	TRM AIO invalid CSCW (limit threshold)	TRM down	82
96	0	TRM disconnect state (following request from MOSS) • X'7E' bit 0.2 or 0.6 ON • Error status, bit 0.7 ON • Ext register X'01' bit 5 ON	TRM OFF line	B9
97	0	TRM PIO error-output IOH/IOHI • X'75' bit 0.0 or 1.0 ON • X'76' bit 0.4 ON for IOC1 time out or • X'76' bit 1.4 ON for IOC2 time out • X'76' bit 0.5 or 1.5 for IOC bus in parity error X'76' bit 0.6 or 1.6 OFF in both cases Origin given in error status type 1 of TRM	NCP retry	NO
97	0	TRM PIO error-output IOH/IOHI (limit threshold)	TRM down	NO
98	0	TRM PIO error-output IOH/IOHI (over threshold)	TRM down	82
99	0	TRA adapter error (IOH bit 1.7 ON)	TRM down	82
9A	0	TRM adapter error unresolved • First get error status failed but retry was successful • Error status has value at time of failure		NO

Table 12-69 (Page 2 of 3). TRSS BER Type 15 Summary

BER ID	ABEND Code (NCP)	Event Description	Recovery or PGM Action	ALARM/ ALERT
9A	0	TRM adapter error unresolved (limit threshold) Error status filled by X'FFFF'	TRM down	82
9B	0	Interrupt from disconnected TRM • Level 1 interrupt presented to NCP/PEP while the TRM is disconnected (X'01' bit 5 ON) • X'7E' bit 0.2 or 0.6 ON		NO
9B	0	Interrupt from disconnected TRM (limit threshold)	TRM down	NO
9B	XXXX	Interrupt from disconnected TRM	NCP re-IPL	NO
9C	0	Adapter PIO error on broadcast "get line ID" IOH command Adapter was the answering one at failure time.	NO	NO
9C	0	Adapter PIO error on broadcast "get line ID" IOH command Adapter was the answering one at failure time. (threshold)	83	83
9E	0	Get error status command failed (IOC error) during NCP LVL1 process on Line Adapter LVL1 or on PIO Get Line ID error.	NCP re-IPL	83
A3	0	Invalid level 2 interrupt	TIC down	80
A4	0	DMA or interrupt vector error due to TIC interrupt level 2 • TRM status bit 0 ON • TRM status bits 4, 5 not '000'	TIC retry	NO
A4	0	DMA or interrupt vector error due to TIC (limit threshold)	TIC down	80
A5	0	DMA or interrupt vector error due to TRM Interrupt level 2 • TRM status bit 0 ON • TRM status bit 6 ON	TIC retry	NO
A5	0	DMA or interrupt vector error due to TRM (limit threshold)	TRM down	83
A7	0	PIO-MMIO error interrupt level 2 • TRM status bit 0 ON • TRM status bits 1, 2, 3 neither '000' nor '001'	TIC retry	NO
A7	0	PIO-MMIO error (limit threshold)	TIC down	80
A8	0	PIO-MMIO error (last TIC) • TRM status bit 0 ON • TRM status bits 1, 2, 3 = '001'	TRM retry	NO
A8	0	PIO-MMIO error (last TIC) • TRM status bit 0 ON • TRM status bits 1, 2, 3 = '001'	TRM down	83
AC	0	TIC adapter check interrupt level 2 • TRM status bit 0 OFF • TRM status bit 3 ON	TIC down	80
AF	0	TIC down at open time • Interrupt level 2 • SSB open completion bit 6 ON	TIC down	85
B2	0	TIC/TRM check at initialization time	TIC retry	NO

Table 12-69 (Page 3 of 3). TRSS BER Type 15 Summary

BER ID	ABEND Code (NCP)	Event Description	Recovery or PGM Action	ALARM/ ALERT
B2	0	TIC/TRM check at initialization time (limit threshold)	TIC down	(2)
B3	0	Back-up time out. No completion interrupt level 2 received during the back-up timer with : • TIC control register bits 0, 1, 3 OFF • IR/BR register bit interrupt request OFF	TIC down	87
B4	0	Component out of use • 'Interrupt occurred' flag OFF when the timer elapses and no interrupt received • 'Write interrupt register' with SCB	TIC down	8B
B5	0	Back-up time out (last TIC). No completion interrupt level 2 received during the back-up timer with : • TIC control register bits 0, 1, 3 OFF, and • IR/BR register bit interrupt request ON, or • TIC control register bits 0, 1, 3 not all OFF	TRM down	81
B6	0	Incomplete frame time out No interrupt level 2 received during the incomplete frame timer	TIC down	8C
B7	0	Token ring link error not caused by controller hardware.	TIC down	8E

Notes:

1. In case of abend, NCP re-IPL is performed and the alarm/alert is generated when IPL is completed. Alert is triggered by MOSS BER ID 06, error code 05.
2. BER ID B2 may generate diferent alerts according to the value of the interrupt register (see alerts 8D, 84, 80).

TRSS BER Type 15 - Detailed BER Display

TRSS BER Type 15 - IDs 14, 16, 91, 92, 93: Format foR1, see page 12-225. Program level 1 generates one of these BERs when an error occurs during an AIO operation on a TRA.

```
                                ELD DETAIL
 SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:15 ID:hh<LOST:ddd CP-ABEND:hhhh>
 TRMnn TICn <ERROR DESCRIPTION>                  <REFER.CODE IN CHAR.> CCCCCCCC
 F:bbbbbbbb
 X7E:hhhh  X76U:hhhh  ETA:hhhh  X3F:hhhhhhhh  X75:hhhh

 X76     TRM STATUS1    SWA ERROR REG
hhhh bbbbbbbb bbbbbbbb bbbbbbbb bbbbbbbb


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

TRSS BER Type 15 - IDs 18, 97, 98, 9C: Format foR2, see page 12-225. Program level 1 generates one of the following BERs when an error occurs during a PIO operation on a TRA.

```
                                ELD DETAIL
 SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:15 ID:hh<LOST:ddd CP-ABEND:hhhh>
 TRMnn TICn <ERROR DESCRIPTION>                  <REFER.CODE IN CHAR.> CCCCCCCC
 F:bbbbbbbb
 X7E:hhhh  X76U:hhhh  ETA:hhhh  X74:hhhhhhhh
 X79:hh  IAR:hhhhhh  I:hhhh  TA:hhhh  TD:hhhh

 X76     TRM STATUS1    SWA ERROR REG
hhhh bbbbbbbb bbbbbbbb bbbbbbbb bbbbbbbb


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

TRSS BER Type 15 - ID 96, 99, 9A, 9B: Format foR3, see page 12-225. Program level 1 generates one of the following BER when a TRM is disconnected by the MOSS, or when an error is reported by a TRM on level 1.

```
                                ELD DETAIL
 SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:15 ID:hh<LOST:ddd CP-ABEND:hhhh>
 TRMnn TICn <ERROR DESCRIPTION>                 <REFER.CODE IN CHAR.> CCCCCCCC
 F:bbbbbbbb
 X7E:hhhh  X76U:hhhh  TRMA:cc
 X76    TRM STATUS1        SWA ERROR REG
hhhh bbbbbbbb bbbbbbbb    bbbbbbbb bbbbbbbb


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

TRSS BER Type 15 - IDs A3, A4, A5, A7, A8: Format foR4, see page 12-225. Program level 2 generates one of the following BERs when an error occurs (internal TRM/TIC error).

```
                                ELD DETAIL
 SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:15 ID:hh<LOST:ddd CP-ABEND:hhhh>
TRMnn TICn <ERROR DESCRIPTION>                   <REF. CODE IN CHAR.> CCCCCCCC
 F:bbbbbbbb
 TA:hhhh TICA:hh
 TRM STATUS2
 bbbbbbbb bbbbbbbb


 ===>

  F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

TRSS BER Type 15 - ID AC: Format foR5, see page 12-226. Program level 2 generates the following BER when a TIC adapter check occurs on a TIC.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:15 ID:hh<LOST:ddd CP-ABEND:hhhh>
TRMnn TICn  <ERROR DESCRIPTION>                   <REF. CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
TA:hhhh TICA:hh
TRM STATUS2
bbbbbbbb bbbbbbbb
TIC ADAPTER CHECK STATUS:
bbbbbbbb bbbbbbbb hhhh hhhh hhhh


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

TRSS BER Type 15 - ID AF: Format foR6, see page 12-226. Program level 2 generates the following BER when a TIC check occurs at open time.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:15 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                               <REF. CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
TA:hhhh TICA:hh
TRM STATUS2
bbbbbbbb bbbbbbbb
SSB
hhhh bbbbbbbb bbbbbbbb


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

TRSS BER Type 15 - ID B2: Format foR7, see page 12-226. Program level 3 generates the following BER when a TIC/TRM check occurs on a command sent to a TRM.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:15 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                               <REF. CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
TA:hhhh             TICA:hh
TRM IIR             TIC CTL REGISTER
bbbbbbbb bbbbbbbb   bbbbbbbb bbbbbbbb


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

TRSS BER Type 15 - IDs B3, B4, B5, B6: Format foR8, see page 12-226. Program level 3 generates one of the following BERs when a time out occurs on a command sent to a TRM.

```
                                ELD DETAIL
SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:15 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                              <REF. CODECIN CHAR.> CCCCCCCC
F:bbbbbbbb
TA:hhhh             TICA:hh
TRM IR/BR           TIC CTL REGISTER
bbbbbbbb bbbbbbbb   bbbbbbbb bbbbbbbb


===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

TRSS BER Type 15 - ID B7: Format foR9, see page 12-226. Program level 3 generates the following BER when an external token ring physical link error occurs.

```
                                ELD DETAIL
 SEL#:hhhh   FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:15 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                                   CCCCCCC
 F:bbbbbbbb
 ALERT:hh         TICA:hh
 PLM STATUS:hh

 Q3: bbbbbbbb bbbbbbbb bbbbbbbb bbbbbbbb

 ===>

 F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

TRSS BER Type 15 - Field Description

Table 12-70 (Page 1 of 2). TRSS BER Type 15 Field Description

Field Name	Meaning	Refer to
TICA	TIC internal address 00-01 (within the TRM)	
TRM STAT2	TRA level 2 error status	page 5-50
TRMnn	TRM number (decimal in error description field). This TRM number is derived from: • field TA for PIO operation – for CS error reported at level 2 – for CA error reported at level 3 • field X75 for AIO operation • field TRM status level 1 for TRM adapter error reported at level 1 If no nn is specified (blank), problem isolation by program was not possible.	
TICn	TIC number 1-2 within the TRM	
TIC adapter check status	Four halfwords giving the reason of a TIC microcode abend	page 5-53
TRM STAT1	TRA level 1 error status	page 5-49
TRM IR/BR	Interrupt request/bus request flags	page 5-33
TIC CTL REG	TIC control register	page 5-32
TRM IIR	TIC interrupt register (initialize)	page 5-56
TA/TD		page 5-37 and page 5-30
ETA	TA field of IOH failure in level 1.	See TA on page 5-39

Table 12-70 (Page 2 of 2). TRSS BER Type 15 Field Description

Field Name	Meaning	Refer to
F	Indicator flag, indicates a byte expansion follows	
TRMA	TRM adapter position (1, 2, 5, or 6	page 3-74
I	First two bytes of instruction.	
IAR	IAR of interrupt level.	page 2-25
X3F	CSP shared pointer register	page 2-26
X74	X'74' - LAR bytes	page 2-33
X75	X'75' - Cycle steal control word register	page 2-34
X76	X'76' - IOC error summary register	page 2-36
X76U	X'76' - Cause of error not found (PIO to read error register failed)	page 2-37
X77	X'77' - Interrupt request reg - adapter level 2 and 3	page 2-38
X79	X'79' - Interrupt level	page 2-39
X7E	X'7E' - CCU level 1 interrupt	page 2-43
X7F	X'7F' - Interrupt request reg - CCU level 2, 3, and 4	page 2-44
SSB	System status block	(*)
SWA	SWA error register	page 3-23
ALERT	NTRI alert number (external error code for alarm 8E)	Alarm 8E in the PD Guide
PLM STATUS	Physical link status at time of error	page 12-224
Q3	Qualifier 3 of the alert	(*)

Note: All values are in hexadecimal format (X'0' to X'F'), except for:

1. The TIC ADPT CHECK STAT, SSB, TRM IR/BR, TIC CTL register, TRM IIR, TRM status 1, TRM status 2, which are in **bit format** (8 or 16 bits, 0 or 1)
2. The error description line with a TRM number and TIC number, which are in **decimal**.

(*) For software information on BERs originated by NCP/PEP, refer to the associated product documentation.

Physical Link (PLM) Status Definition

PLM Status (Hexa)	Meaning
00	Inactive: Physical link is not activated
01	Activating: TIC initialization in progress
02	Activating: TIC initialization complete
03	Activating: Open in progress
05	Active: Physical link is activated
06	Deactivating: Close in progress
07	Deactivating: Closed
08	Active or deactiving: Requested statistics from TIC
09	Active: Ring beaconing in progress
0A	Deactivating: Deactivation from host in progress

TRSS BER Type 15 - Formats

Format: foR1

IDs: 14 16 91 92 93	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35-36	X76
37-38	X75
39-40	Unused
41-42	ETA
43-44	TRM STATUS1
45-46	X76U
47-50	X3F
51	F
52	Unused
53-54	SWA
55-72	Unused

Format: foR2

IDs: 18 97 98 9C	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35-36	X76
37-38	I
39-42	X74
43-44	TRM STATUS1
45-46	X76U
47-48	ETA
49-50	Unused
51	F
52	Unused
53-54	SWA
55	X79
56-58	IAR
59-60	TA
61-62	TD

Format: foR3

IDs: 96 99 9A 9B	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33-34	X7E
35-36	X76
37	TRM address
38-42	Unused
43-44	TRM STATUS1
45-46	X76U
47-50	Unused
51	F
52	Unused
53-54	SWA error reg
55-74	Unused
75-76	ETA

Format: foR4

IDs: A3 to A8	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33	F
34	TICA
35-36	TA data
37-38	TRM STATUS2

Figure 12-32 (Part 1 of 2). TRSS BER Formats

Format: foR5

ID: AC	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33	F
34	TICA
35-36	TA data
37-38	TRM STATUS2
39-46	Adapter check status

Format: foR6

ID: AF	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33	F
34	TICA
35-36	TA data
37-38	TRM STATUS2
39-42	SSB open completion

Format: foR7

IDs: B3 to B6	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33	F
34	TICA
35-36	TA data
37-38	TRM IR/BR register
39-40	TIC control register

Format: foR8

ID: B2	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33	F
34	TICA
35-36	TA data
37-38	TIC init interrupt register
39-40	TIC control register

Format: foR9

ID: B7	
Byte	Meaning
1-27	Header
28-29	TYPE-ID
30	LOST
31-32	Abend
33	F
34	TICA
35-36	TA data
37	NTRI Alert number
38	PLM status
39-42	Alert Q3 field

Figure 12-32 (Part 2 of 2). TRSS BER Formats

Chapter 13. Traces, Dumps and File Transfer

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Traces

This section gives a general overview of the communication functions which can be traced in the 3745 and its environment.
This general overview will help the CE select the type of trace applicable to a specific problem.

Depending on type of trace chosen, the user is invited to start, stop, and display either from the MOSS console, (Refer to *3745 Service Functions Manual*, SY33-2055 for more information), or from the host console (refer to the appropriate software publication).

Trace Summary

	Line Trace	**External SIT (Internal SIT see note 2)**	**Checkpoint Trace**	**TIC Internal Trace**	**Internal CA Trace**
Goal	Check telecommunication line functions	Check scanner functions in correlation with NCP/PEP line trace	Problem isolation between the scanner microcode and scanner hardware	Problem isolation between NCP and TRM/TIC	Trace interface between CA and CCU, CA and channel
Method	Trace data and control information in CCU	Trace data and control information for each IOH	Internal traces of key entry points for each IOH	Trace data for each frame	Trace CA hardware and M-code registers
Limitations	1 line at a time for EP, 8 lines at a time for NCP 1 line for HPTSS, ESS	Max 4 interfaces up to 9600 bps. Max 2 interfaces up to 256 kbps (see note 1) Max 1 interface for HPTSS Max 2 interfaces for ESS	Max 4 interfaces up to 9600 bps. Max 2 interfaces up to 256 kbps (see note 1) Max 1 interface for HPTSS Max 2 interfaces for ESS	1 line at a time	Any or all CA at a time
Customer Impact	In line mode (performance impact)	In line mode (performance impact)	In line mode (performance impact)	In line mode (performance impact)	In line mode (performance impact)
Output	Host	Host/RSF/MOSS	Host/RSF/MOSS	Host	MOSS/RSF
Hard Copy	Yes (ACF/TAP)	Yes (ACF/TAP)	Yes (SIT imbedded)	Yes (ACF/TAP)	Yes (Host)
Documentation Support	Access method for operation. ACF/TAP for output	Access method for operation. ACF/TAP for output	MIR, Service Functions	Access method for operation ACF/TAP for output	MIR, Service Functions
Contents	RECTRD RU IOH Data Parameter A Status A Data	IOH, TCC, CCU Parm/Status FESL Status Data	CSP Address ICB Control ICB Status	RECTRD RU TIC internal elements	Trace data for each CA interrupt (CCU or channel)

Notes:

1. At 256 kbps, control information is fully traced, but data is traced only for 40 bytes.
2. Refer to page 13-24 where the differences between internal and external SIT are explained.
3. For more information on ACF/TAP refer to *NCP, SSP, EP Diagnosis Guide*.

Communication Functions Which Can Be Traced

The following table summarizes the available traces for 3745 communication functions in which the 3745 might be involved.

Trace Type	Called By	Output Returned Via	Users
ACB/AXB	Contin-ously	NCP dump or by NetView	Customer or CE
Applications	Host	Host	Customer
Branch	MOSS (note 2)	MOSS console	Customer or CE
CA internal	Host/ MOSS	ACF/TAP	Customer or CE
Checkpoint	Host and MOSS	ACF/TAP, MOSS console	Customer or CE
External SIT	Host	ACF/TAP	Customer or CE
Internal SIT	MOSS	MOSS console	Customer or CE
NetView session monitor	Host	NetView session monitor	customer or CE
PEP line	Host/ MOSS (note 1)	DYNADUMP	Customer or CE
NCP line	Host	ACF/TAP	Customer or CE
NCP TG	Host	ACF/TAP	Customer or CE
NCP generalized PIU	Host	ACF/TAP	Customer or CE
NCP session	Host	NetView session	Customer or CE
NCP CA	MOSS (note 1)	NCP dump	Customer or CE
NCP address	MOSS (note 1)	NCP dump	Customer or CE
NCP dispatcher	Continously	NCP dump	Customer or CE
TIC	Host	MOSS console, ACF/TAP	CE
VTAM/TCAM			
—Buffer	Host	ACF/TAP	Customer or CE
—I/O	Host	ACF/TAP	Customer or CE
—PIU	Host	ACF/TAP	Customer or CE
—Internal	Host	VTAM/TCAM dump	Customer or CE

Notes:

1. Called via host or control program procedures.
2. Called via CCU services.

Traces in an ACF/VTAM Environment

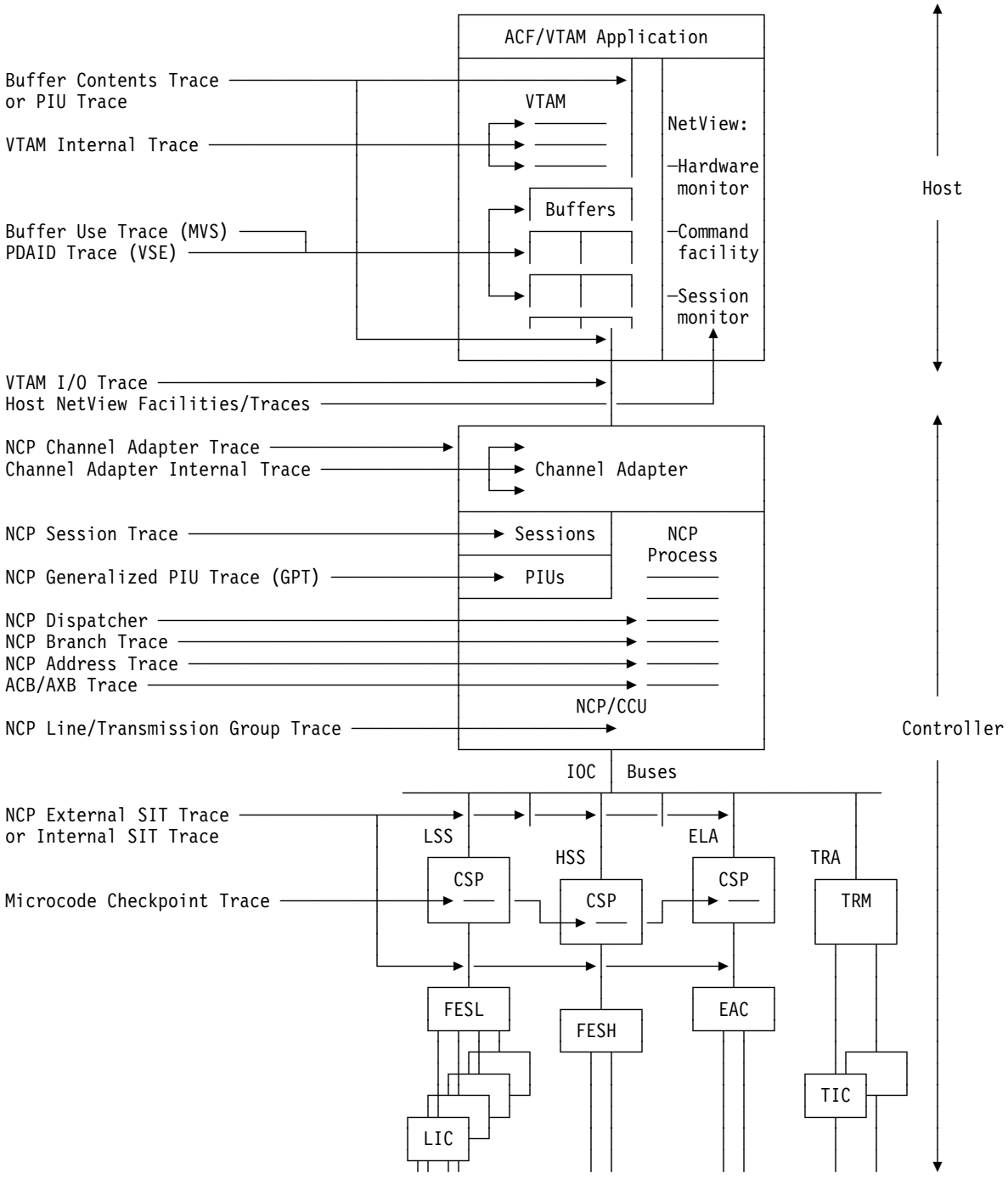


Figure 13-1. Host Traces in an ACF/VTAM Environment

Buffer Contents Trace

The buffer contents trace shows what is passing back and forth at two points within ACF/VTAM. One of the points is just inside the ACF/VTAM code near the application program interface (API); the other point is internal to the ACF/VTAM code.

The user data portion (RU) of the buffer contents trace records written from these two points, should be identical for the same PIU, since ACF/VTAM does not modify the user data it handles.

The MVS VTAM buffer contents trace records up to 212 bytes of data (224 bytes for VSE) from VTAM buffers during the transmission of an inbound or outbound message to a locally-attached device or NCP. The buffer contents trace includes the transmission header (TH), and the request/response header (RH). VTAM adds 32 bytes of header information to the MVS and VSE trace data records. GTF adds up to 12 bytes of header information to MVS/VTAM trace data records.

Because the buffer contents trace shows the contents of the PIU, this trace is sometimes called the PIU trace.

VTAM Internal Trace

The VTAM internal trace can be used to trace various types of internal activity within ACF/VTAM. This trace can be helpful if you suspect that ACF/VTAM is malfunctioning.

Buffer Use Trace

The MVS ACF/VTAM buffer use trace contains information about the 11 user-defined ACF/VTAM buffer pools. This trace helps tune an ACF/VTAM system for the optimum number of buffer pools.

The VSE PDAID trace can be used to trace a number of internal functions, but its main use, so far as ACF/VTAM is concerned, is to provide statistics on ACF/VTAM buffer use. Although the PDAID trace is functionally different from the MVS buffer use trace, it provides similar information on buffer-pool use.

VTAM I/O Trace

The I/O trace shows what is passing back and forth between ACF/VTAM and NCP.

The MVS VTAM I/O trace (RNIO) and VSE I/O trace (part of PDAIDs) records up to 20 bytes of data during the transmission of an inbound or outbound message to the NCP. This data includes the transmission header (TH), request/response header (RH), and a variable portion of the request/response unit (RU).

GTF adds up to 36 bytes of header information to the RNIO trace.

VSE/VTAM adds a 32-byte header to the I/O trace.

The RNIO or I/O trace is similar to a short buffer trace in contents, if user data is being transmitted and received. However, certain control sequences that do not appear in VTAM buffer traces may appear in RNIO or I/O traces.

The RNIO or I/O trace is used to check if the SNA sequences between VTAM and NCP are correct.

The RNIO or I/O trace is abbreviated, to save trace file space. It is preferable thus to use it instead of the VTAM buffer trace.

There are some internal VTAM PIUs/RU that will appear in the actual trace, and which may not have been originated by the NCP.

Host Traces (Environment-Independent)

Host NetView Session Monitor Trace

The NetView Session Monitor Trace executes on operating systems and access methods supported by the NetView command facility, Release 2, and the NetView Hardware Monitor Release 2E.

NetView command facility, Release 2, and NetView Hardware Monitor, Release 2E, are prerequisite for NLDM.

The NetView Session Monitor is an IBM licensed program for the continuous collection of session-related data. It has functions for monitoring session activity and completing problem determination of errors which, typically, manifest themselves as a 'hung' terminal session.

The NetView Session Monitor Trace establishes session awareness in a NetView command facility application.

The control and data flows between the NetView Session Monitor and the access methods provide the session knowledge to accommodate network enhancements in the areas of connectivity, configuration, performance, accounting, and problem determination.

The NetView Session Monitor is structured to facilitate the addition of network functions that relate to sessions. It provides an interactive session trace capability that captures access method PIUs and selected NCP control information about a session.

The capturing of session data by the NetView Session Monitor allows for continuous capture if desired by the user. The user must be able to turn data capture ON/OFF by session type and/or session name.

To provide efficient data capture, the NetView Session Monitor maintains active session wrap areas in virtual storage. The size of the wrap areas is specified by the user.

The NetView Session Monitor collects session information from two sources:

- The access method (VTAM),
- And the boundary (NCP).

The functions provided by the NetView Session Monitor are oriented to the CE and the system programmer. These functions correlate and format internal session-related data and require SNA level expertise for full understanding. The NetView Session Monitor provides information on:

- Activation and deactivation of session trace
- Session name lists
- Most recent sessions
- Session connectivity
- Bind
- Access method PIU trace data
- NCP control status data
- Hexadecimal display of access method PIUs.

NCP Channel Adapter Trace

The channel adapter trace is an optional debugging aid that stores certain fields from the channel control block into a trace table.
A maximum of 256 trace entries can be specified at SYSGEN time.

The channel adapter trace can be activated or deactivated from the operator console using the CCU functions (refer to *Advanced Operations Guide*, SA33-0097 for more information).

The NCP CA trace automatically starts the internal CA trace (see the topic “Internal Channel Adapter Trace” on page 13-30 for more information).

The trace table can be examined in a storage dump or by using the CCU display facilities at the MOSS console. For details on the trace information, refer to the appropriate software publications.

Any combination of up to six channels can be traced.

NCP Session Trace

The NCP continuously captures the last and next to last sequence/reference numbers sent to and from a boundary node resource.

When the session ends, and if session trace is enabled for the resource, the sequence/reference number, plus additional information from the control status data of the NCP are sent unsolicited to the communication network management interface (CNMI) of the access method.

The logical data manager (NLDM) formats and displays this information.

The NCP session trace is totally independent of any other NCP trace facilities, including the generalized PIU trace function.

Session trace can be activated and deactivated via a NMVT from any host which is the owner of the NCP.

The PIU sequence/reference number capturing for support of the session trace function will operate continuously after the NCP is loaded and initialized.

Storage to save sequence/reference numbers is allocated for each resource when the NCP is generated.

The NCP provides the session trace NetView Session Monitor function to continuously capture PIU sequence numbers flowing to or from each SNA boundary node resource (LUs and PUs), for each SSCP-NCP session.

For pre-SNA boundary node resources, unique reference numbers and the FID0 PIUs are captured continuously.

Both numbers for each resource are sent to the NetView Session Monitor application using a solicited/unsolicited NMVT.

Unsolicited NMVTs are sent at session termination, (LU-LU, SSCP-PU), but not for SSCP-NCP PU sessions), for SNA resources and only when an abnormal or error condition is detected for pre-SNA resources.

Solicited NMVTs are sent to the NetView Session Monitor when an NMVT request is received for a specific resource.

The trace can be activated for the following resources:

- NCP physical services (PU)
- SDLC type 1, 2, 2.1 physical units (PUs)
- SDLC logical units (LUs)
- Start-stop devices (DVBs).

Any type of resource not included in the above list is not eligible for trace activation. The following are examples of non-eligible resources:

- All user-written program resources
- SDLC links
- Start-stop links
- BSC links
- SDLC type 4 stations.

NCP Generalized PIU Trace (GPT)

The generalized PIU trace (GPT) facility allows the network operator to trace a selected network-addressable resource for the NCP. This trace is activated/deactivated by the network operator.

The NCP traces all header and limited data of the PIU sent between the boundary function and the virtual routing function of the NCP.

The NCP sends the trace records to the SNA access method to be logged and later, to be formatted by ACF/TAP.

Tracing the Outbound PIUs

Each PIU is traced in its FID4 format immediately before the NCP delivers the PIU to the connection point manager (CPM) of the resource.

The presence of the PIU in the trace data guarantees that the PIU was successfully received by the NCP, passed all explicit and virtual routing requirements, and was destined for a known boundary node resource.

It does not guarantee that the PIU was actually sent over a data link control function.

Tracing the Inbound PIUs

Each PIU is traced in its FID4 format after the boundary node has delivered the PIU to the virtual routing component.

'Inbound' here means 'to the virtual route function', not necessarily from the resource being traced.

For example, an activate physical request to a PU type 1 resource is turned around by the NCP boundary node and is not actually delivered to the device. This 'activate physical request' is traced in the outbound flow, and the response is traced in the inbound flow.

Limitations: The following table gives the number of bytes traced, including the FID4 header, versus the resource type.

Resource Type	Number of Bytes Traced
SNA boundary node PU	40 (TH + RH + 11 bytes of RU)
BSC 3270 display	40 (TH + RH + 11 bytes of RU)
BSC 3270 controller	44 (TH + RH + 15 bytes of RU)
NCP PU	44 (TH + RH + 15 bytes of RU)
User-programmed PU	40 (TH + RH + 15 bytes of RU)
User-programmed LU	40 (TH + RH + 11 bytes of RU)
	40 (TH + RH + 11 bytes of RU)

The maximum number of resources that can be traced simultaneously is limited by buffer and cycle utilization considerations.

The NCP always accepts a request to activate GPT (assuming validity checks are passed) even when the performance is degraded.

The NCP does not terminate the GPT when the NCP slows down (buffer depletion).

NCP Branch Trace

The mechanism of the NCP branch trace facility allows the CCU to record, in a predefined buffer, the non-sequential operations occurring in the flow of the CCU control program. When a branch occurs in the CCU, the 'come from' and 'go to' addresses are stored in the buffer as well as the corresponding 'come from' and 'go to' program level.

This trace is more specifically oriented toward software activities. However, it can be used by the CE for problem determination or isolation activities.

The branch trace buffer can be displayed at the MOSS console or dumped to the host.

The branch trace is started from the operator console (refer to *Advanced Operations Guide*, SA33-0097 for more information).

NCP Address Trace

The address trace is a service aid that records the contents of selected areas of controller storage and selected external registers at each successive interrupt.

Certain types of interrupt, or all interrupts, can be recorded. The network control program records the trace data in a trace table in control storage.

When the desired data has been recorded, the contents of the trace table can be displayed at the console.

For details on the trace information, refer to the appropriate software publication.

The contents of controller storage can be transferred to the host processor via the dump program, and the contents of the trace table examined in the listing of the dump.

The address trace facility allows the user to select any combination of up to four external registers, general registers, and storage halfwords whose contents are to be recorded each time data is loaded from or stored into a specified storage address at a specified program level.

The address trace is activated or deactivated from the MOSS operator console for the user-specified storage address or external register, using the control program procedures (refer to *Advanced Operations Guide*, SA33-0097 for more information).

NCP Line Trace

The NCP line trace captures the information at the boundary between the CCU and the CSP. The NCP parameter and status information (PSA), as well as line data are placed into line trace buffers by the NCP. This information is then transferred to the host where ACF/TAP retrieves and prints it (for details on the trace information, refer to the appropriate software publication).

The VTAM operators parameter default is X'FF', meaning 'trace all data'. But for an ESS interface, if the default X'FF' is taken, 42 bytes are traced.

Note: For starting or ending the trace, refer to the appropriate software publication.

EP Line Trace

The line trace facility of the PEP, is a service aid that permits detailed analysis of the operation of any telecommunication line controlled by the program. This facility records the operating parameters of a line each time a level 2 or level 3 interrupt occurs for that line. The program accumulates this information in a trace table within controller storage. The line trace records can be examined in a storage dump, or by using the CCU display facilities at the operator console.

The line trace facility does not interfere with the normal operation of the telecommunication line. Performance may be diminished somewhat because of the additional processing needed each time a character service interrupt occurs for the line or lines being traced. The amount of decrease in performance depends on how heavily the communication controller is currently loaded. Including the line trace facility has no effect on performance, except when a line is being traced.

The line trace is started or stopped by the host's DYNADUMP utility or by the MOSS/CCU data exchange procedure (CCU services). The 'option' statement of DYNADUMP allows the CE to request a PEP line trace (with or without data), or a scanner interface trace (with or without data), or both.

A maximum of 16 SIT traces can run concurrently. There is no limit to the number of EP line traces that can be run. In a PEP system, EP can run 16 SIT traces in addition to the eight traces that can run in the NCP.

Transmission Group Trace

The line trace with the transmission group (TG) option, provides the facility to trace all SNA-dependent information, such as: SNA headers, requests, and responses, as they enter and leave an NCP over a cross-domain link.

The facility includes the transportation of the traced data to an SSCP (VTAM), and the formatting and printing of the traced data at the host by ACF/TAP.

In the NCP, this facility is a special case of the existing line trace facility, and as such, the TG trace is tightly coupled to a cross-domain link.

Activation and deactivation are requested by referencing one and only one of the links in the TG to be traced.

Both the TG PIU trace for all links in the TG, and the line trace for the referenced link in the TG, are activated. Additional links in the TG may be line-traced in the present mode of activation.

The TG trace continues as long as the line trace on the referenced line continues, and as long as the line is not removed from the TG.

NCP Token-Ring Function Traces

The NCP token-ring function provides the user with three traces:

- Line trace,
- IOH trace and,
- TIC trace.

The trace function records activity on a designated physical link. The information is then transferred to the host, where ACF/TAP retrieves and prints it (for details on the trace information, refer to the appropriate software publication).

The printout is used to isolate a problem into the NCP or TRM/TIC area.

An token-ring link is a high-speed line, and only one line may be traced at a time. The trace function is supported only for physical links.

Line and IOH Trace

The traced IOHs are the ones dedicated to a TIC and to the TRM that control this TIC.

The IOHs are traced into an IOH trace area and then reported to the host by the line trace process.

The IOH trace is activated/deactivated with the line trace.

TIC Internal Trace

The TIC internal trace data is transferred to the NCP as MAC frames.
To start or stop the TIC internal trace, the NCP sends a new SCB command.

The line trace and IOH trace run together, and are activated/deactivated from the host or by the NCP normal services in case of a slowdown.

Activation of Traces

Three types of trace can be activated in the NCP: line trace, scanner trace, and internal trace (including TG).

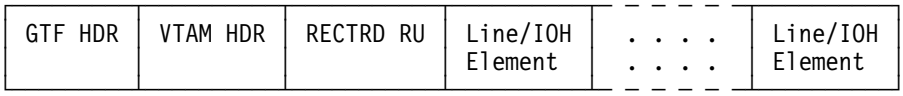
The line trace and IOH trace are activated at the same time, that is, started with the same ACTTRACE RU.

The NCP token-ring function has to activate two traces: line and IOH trace, and TIC internal trace which are mapped as follows:

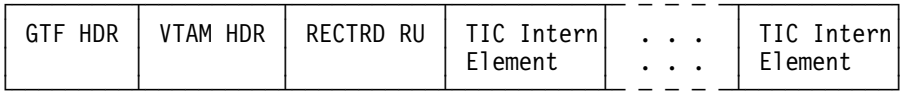
- Line and IOH traces are activated by ACTTRACE RU with type=LINE.
- TIC internal is activated by ACTTRACE RU with type=SIT.
- A negative return code is answered for the ACTTRACE of the TG.

ACF/TAP Editing and RU Formats

The data of the different traces is transferred to the host using RECTRD PIUs. ACF/TAP receives the LINE and IOH trace records in the following format:



ACF/TAP receives the TIC internal records in the following format:

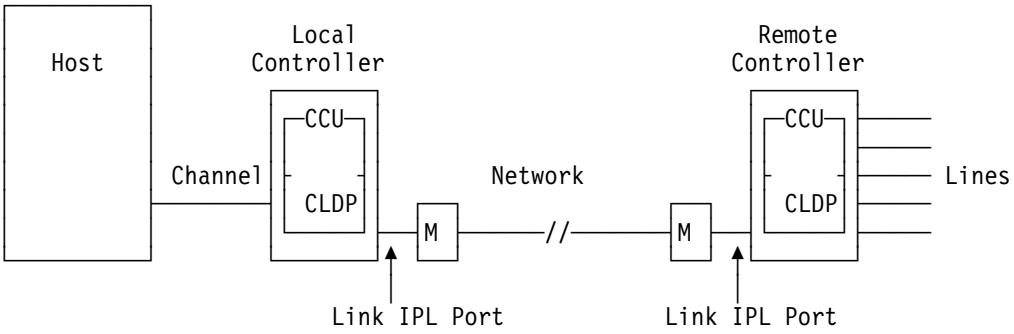


Each record has a GTF header, followed by a VTAM header, a RECTRD RU, a number of TIC internal traces, line and IOH elements. The NCP token-ring function is only concerned about the RECTRD RU header, the line/IOH elements, and the TIC internal trace elements.

For more info on ACF/TAP refer to *NCP, SSP, EP Diagnosis Guide*.

Link IPL Port Trace (LIPT)

The link IPL port trace (LIPT) facility allows to record in the scanner, the activity between the CLDP and any line used as link IPL port. The customer may start the trace on the local or remote controller, or both. The traces are stopped automatically when the control program is loaded.



- On the ***local controller*** the trace records, in the scanner, all activities between the CLDP and the line used as link IPL port. The trace is active until a channel request is received by the CLDP.
- On the ***remote controller*** the trace records, in the scanner, all activities between the CLDP and the line used as link IPL port. The trace is active until the NCP load is completed.

The LIPT is initiated on request at the MOSS console whenever a problem is encountered during the load or the dump sequence, or when more information needs to be gathered to do further problem determination and isolate a problem in the following areas:

- The hardware on the link (FESL, FESH, MUX, LIC, or MODEM)
- The microcode
- The control program
- The network
- The link IPL port definition
- The NCP generation

To activate the LIPT, refer to the paragraph "Defining a Link IPL Port" in the chapter "Link IPL Port (LKP)" of the *Advanced Operator Guide*, SA33-0097.

The LSS and HSS dumps provide the trace data for investigation.

Link IPL Port Trace (LIPT) Functional Description

The LIPT can be activated on any of the eight possible link IPL ports defined in the LKP function, on the local and/or remote controller:

- When activated at the MOSS, the trace request is sent and recorded into the CLDP during IPL phase 2.
- After the scanner IML is complete, the CLDP forwards the trace request to the scanner containing the line which has to be traced.
- The scanner then initializes the trace and uses a full-size buffer with wrap option to trace the activity on the link IPL port.

- The trace process in the scanner stays active in the local controller until a channel request is received by the CLDP, and stays active on the remote controller until the NCP load is completed.

On the MOSS side, the trace request is reset as soon as the request is passed to the CLDP. This prevent the user to leave the trace active indefinitely.

External Scanner Interface Trace

The external scanner interface trace (formerly called NCP SIT) objectives are:

- Problem determination between 3745 hardware and NCP/PEP software
- Problem isolation in the transmission subsystem and IOC areas (CSP and its microcode, FESL, DMUX, LIC, IOC bus).

This trace gets, for each line interface, data and parameter information from both sides of the CSP:

- Between FESL and CSP, the values traced are the transferred data, and the FESL status.
- Between CSP and CCU, the IOH, parameters, and status of each scanner command are traced.

The same applies for HPTSS. But only one SIT can be activated on one scanner (one line trace for each controller).

The amount of data that you can trace for each 3745 using HSS lines is limited to 40 bytes.

For ESS, two SITs can be active on each adapter (one for each line). The amount of data that can be traced for ESS is limited to 252 bytes.

The NCP/PEP line trace provides a correlation between both traces when they are run concurrently.

Information Traced

The trace information data is:

- IOH, parameter and status to and from the control program
- Data from the FESL/FESH/EAC.

The trace information is transferred from the CSP to the CCU by cycle steal. It is stored in the host in the same data set as the NCP/PEP line trace for later retrieval, formatting, and printing using ACF/TAP or DYNADUMP (PEP).

In addition to the NCP/PEP record types, new trace record types have been defined for the SIT.

A new parameter added to the access method line trace command in the host starts the scanner interface trace alone or together with the NCP line trace. Additionally, it is possible to specify in a parameter of this command the number of data bytes to be traced for each message.

Note: To start or end the trace, refer to the appropriate software publication.

NCP V5 has two types of trace for isolating telecommunication line problems:

- Scanner interface trace (SIT), and
- Line trace.

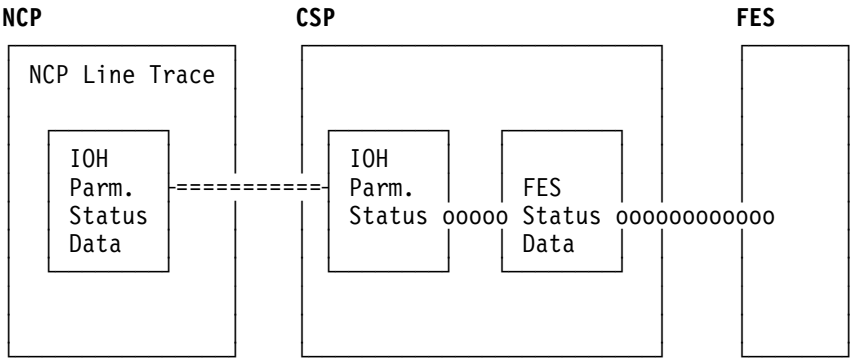
A maximum of eight traces can be active at one time (these can be any combination of SIT and line trace). Both traces are started from the host.

This requires an additional indicator on the activate and deactivate trace RUs to specify SIT.

The amount of data to be traced by line trace and SIT per I/O operation, may be specified by the SSCP in the ACTRACE PIU.

The line trace is a trace of the control program/CSP boundary as seen by the control program.

The scanner interface trace is a trace of the control program /CSP/FESL boundaries as seen by the CSP.



Legend: ==== Line interface traced by line trace
oooo Line interface traced by SIT

Information Traced for ESS

The data starting with the destination address is traced. The ending CRC bytes are not traced.

Information Traced in SDLC (Normal Mode)

During reception, the non-flag characters, the CRC characters, and the first ending flag are available in the data bursts.

The leading flags before the first non-flag character are deleted by the FESL.

During transmission, all the flags, the non-flag characters, and the pads are in the traced burst. The CRC characters are built by the FESL and are not available in the burst.

Information Traced in BSC (Normal Mode)

During reception, the following characters are not available in the burst because they are deleted by the FESL:

- The phase SYN characters and all the following SYNs up to a non-SYN character
- All the SYN characters when in control mode or in normal text
- All the DLE-SYN characters and the first DLE of a DLE-DLE sequence when in transparent text mode
- The BCC characters.

Note: The error intermediate block (EIB), if requested, is built by the FESL and inserted in the burst after an ITB character.

During transmission, all the SYN and control characters, the data, and the pads are available in the traced burst. The following are not traced because built by the FES:

- The SYN-SYN or DLE-SYN sequence generated every second
- The continuous SYN or DLE-SYN sequences generated when underrun occurs.
- The BCC characters.

Information Traced in BSC (Character Mode)

During reception, all the received characters are available in the parameter-status (PSA) except the phase SYN-SYN sequence.

During transmission, all the transmitted characters are available in the PSA except the SYN-SYN or DLE-SYN sequence generated when an underrun occurs.

Tracing in PEP Environment

The host DYNADUMP facility procedure or the MOSS/CCU data exchange procedure is used to start and stop the SIT trace in a PEP environment.

The DYNADUMP formats the trace records so that they are accepted as input to ACF/TAP.

For more info on ACF/TAP refer to *NCP, SSP, EP Diagnosis Guide*.

The 'option' statement of the DYNADUMP allows the CE to request a SIT trace (with or without data), a PEP line trace (with or without data), or both.

Correlating Line Trace and SIT

When it is necessary to run the line trace and the SIT concurrently, the trace correlation count (TCC) in the parameter zone of the NCP parameter status area (PSA), can be used to correlate the line trace entry for an IOH operation with the SIT entry for that operation.

The TCC is used in the parameter zone of the PSA when line trace is in progress for a telecommunication line. Each time the NCP-to-CSP (IOH command) or CSP-to-NCP transfer completes, the NCP line trace captures the parameter zone, then increments the TCC by 1. The trace reader can then use the TCCs to match line trace entries with the corresponding SIT entries.

Trace Limitations

Due to TSS resources and NCP/PEP constraints, there are limitations on the maximum number of lines submitted to the SIT depending on the line speed.
For SDLC lines the limitations are as follows:

- Up to 9600 bps, 4 interfaces per scanner
- Above 9600 bps, 2 interfaces per scanner
- Up to 16 interfaces for the 3745 (eight concurrent traces).

This limit, imposed by the NCP, is shared between the NCP line trace and the SIT.

For HPTSS and for ESS lines, a maximum of two traces (one line trace and one SIT trace) may be started.

The following table shows the scanner performance possibilities when the SIT is running. The additional checkpoint trace does not modify the results.
The values are indicative and do not stand as specifications for the performances.

Protocol	Line Speeds (bps)	Maximum Number of Lines		
		No Trace Activity	Trace Activity	
			Lines Being Traced	Other Lines
SDLC Duplex	2400	32	2	30
	4800	32	2	27
	9600	16	2	11
	19 200	8	1	5
	19 200	8	2	3
	57 600	2	1	0
	64 000	2	1	0
	256 000	1	1*	0
SDLC Half–Duplex	2400	32	2	30
	4800	32	2	30
	9600	32	2	27
	19 200	16	2	11
	57 600	4	1	2
	64 000	4	1	1
	256 000	1	1*	0
Start–Stop	2400	16	2	12
	4800	8	2	4
	9600	4	1	2
	19 200	2	1	0

* In the case of high–speed lines, the traced data is limited to 40 bytes per SDLC frame.

High-Speed Trace Limitations for NCP/SIT

The following tables show the maximum number of lines which can be active during a trace, based on the following assumptions:

- Duplex lines
- 50% utilization
- 40-byte trace records
- 70% maximum CCU and I/O bus utilization
- Speed: 256 kbps for each line (one line per scanner)
- Using NCP V5.

2000-Byte Blocks (PIUs): The table is indicative only.

	No Trace	Line Trace	SIT	Line Trace/ SIT
No trace	7	NA	NA	NA
One line traced	NA	7	7	7
All lines traced	NA	6	6	5

500-Byte Blocks (PIUs): The table is indicative only.

	No Trace	Line Trace	SIT	Line Trace/ SIT
No trace	4	NA	NA	NA
One line traced	NA	3	3	3
All lines traced	NA	2	3	2

Note: Performance analysis shows that one 256-kbps duplex line or two half-duplex lines may be traced with full data on the NCP line trace. This condition may require other lines to be deactivated in the controller.

SIT Record Units

The trace information is stored in the CCU buffer areas. Every IOH or IOHI instruction processed for the interface being traced, causes a trace record unit (TRU) to be stored.

Each TRU contains the IOH/IOHI, the parameter area of the PSA, the data (if any) as exchanged between the scanner and the line interface, and the status area of the PSA, in that order.

If checkpoint trace has not been deactivated from the MOSS, checkpoint data, comprising the interface control block (ICB) control and status information, is also stored.

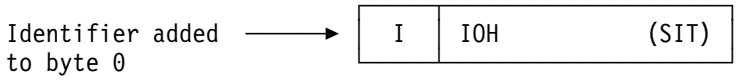
The scanner moves the trace data into the current buffer (or buffer chain) until it is completely filled. TRU recording may be continued by providing a new buffer (or buffer chain) via a second trace command.

Trace Record Unit (TRU) Formats

To find the actual format of an edited SIT, or the description of the PSA field, refer to the "TSS", "HPTSS", and "ESS" Chapters. For details on the control status data information, refer to the appropriate software publication. A summarized TRU field format description is given in the following sections.

IOH/IOHI Field

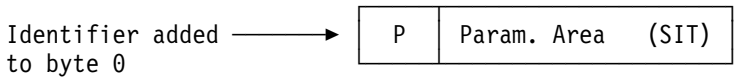
Byte 0 contains the character 'I' identifying an IOH/IOHI field.



Bytes 1 and 2 contain the byte count (always 5).
Byte 3 contains an X'00' pad.
Bytes 4 and 5 contain the first halfword of the IOH/IOHI instruction.
Bytes 6 and 7 contain the second halfword of the IOH/IOHI instruction.

Parameter Field

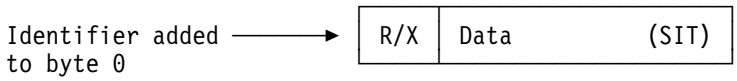
Byte 0 contains the character 'P' identifying a parameter field.



Bytes 1 and 2 contain the data count (equal to 16 for a normal command or 6 for a 3745 emulation command).
Byte 3 contains an X'00' pad.
Bytes 4 through 19 (normal mode) or 4 through 9 (emulation mode) contain the parameter area of the PSA.

Data Field

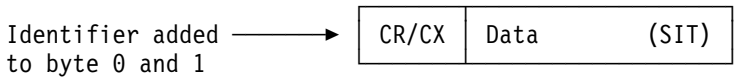
Byte 0 contains the character 'R' for received data, or 'X' for transmitted data.



Bytes 1 and 2 contain the data count (depends on the length of the data burst).
Byte 3 contains an X'00' pad.
Bytes 4 through 'n' contain the data burst. The data burst is a maximum of 8 bytes long, rounded to the next even (halfword) count. The true burst count may be found in the FESL status. The remaining bytes contain the scanner status.

Control Word Field (HPTSS and ESS only)

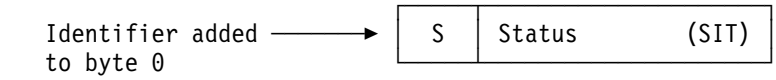
Byte 0 contains the character 'CR' for received control word, or 'CX' for transmit control word.



Byte 2 contains the data count.
Byte 3 contains an X'00' pad.
Bytes 4 through 'n' contain the control word.

Status Field

Byte 0 contains the character 'S' identifying a status field.



Bytes 1 and 2 contain the data count (equal to 12 for a normal command or 6 for an emulation command).
Byte 3 contains an X'00' pad.
Bytes 4 through 15 (normal mode) or 4 through 9 (emulation mode) contain the status area of the PSA.

Checkpoint Data Field

Byte 0 contains the character 'C' identifying a checkpoint data field.

Bytes 1 and 2 contain the byte count (always 5).
Byte 3 contains an X'00' pad byte.
Bytes 4 and 5 contain the scanner microcode checkpoint entry address.
Byte 6 contains the ICB status byte.
Byte 7 contains the ICB control byte.

Overrun Field

Byte 0 contains one of the characters 'I', 'P', 'R', 'X', 'S', or 'C' identifying the type of TRU that the scanner was trying to store when the overrun occurred.
Bytes 1 and 2 contain the byte count (always 0).
Byte 3 contains an X'00' pad.

Notes:

1. The first 4 bytes of every field contain a 1-byte field identifier, a 2-byte count of the data contained in each field, and a pad character to round out the header field to 4 bytes.
2. The data count field specified in the trace PSA TPSA is reinitialized each time there is a turnaround on the line, or that a new SDLC frame is transmitted or received.

Internal Scanner Interface Trace

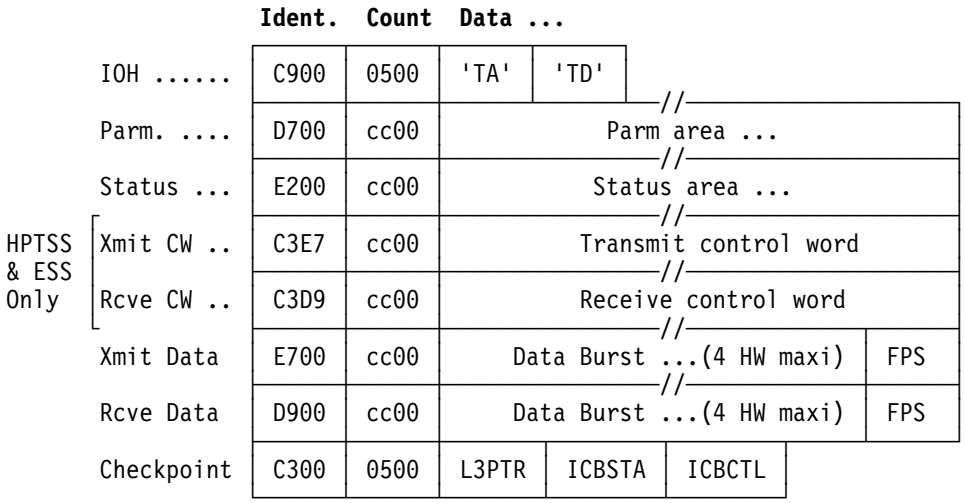
The internal scanner interface trace (internal SIT) is a line trace recorded by the scanner microcode in a 'wrap around' scanner buffer (8 kilobytes). The internal SIT is activated by a SIT function from MOSS on one line, and may be run in conjunction with the NCP SIT (called now 'external SIT'), which is started, on another line by the host operator via NCP/PEP.

The information traced is the same as for the external SIT (IOH, parameter, status, data, checkpoint trace).

There is no interface with the NCP for internal SIT.

For TSS, if more than 4 SITs (for HPTSS more than 1 SIT and for ESS more than 2 SITs) are started on a scanner (internal + external), a status of 'limit exceeded' (X'D2') is returned to the NCP.

If the NCP tries to start a SIT on a line that has internal SIT running at this time, a status of 'SIT already active for this line' (X'D4') is returned to the NCP.
The format is:



Note: 'cc'= byte count in trace record unit (depends on the command).

Differences of Internal SIT Versus External SIT

Items	Internal SIT (commands activated by MOSS operator)	External SIT (commands activated by MOSS operator)
Buffers	Scanner in wrap mode	Scanner+NCP/PEP buffers
– High-speed lines – Medium-speed lines – ESS lines – Others	1 line in 8 kilobytes 2 lines in 4 kilobytes 2 lines in 4 kilobytes 4 lines in 2 kilobytes	1 line in 8 kilobytes 2 lines in 4 kilobytes 2 lines in 4 kilobytes 4 lines in 2 kilobytes
Maximum number of lines traced	Per CSP: 4 SITs Per NCP: 8 SITs	Per CSP: 4 SITs Per NCP: 8 SITs
CSP status display	– TSS functions – New customer function	No status
Display SIT records and formatting	– TSS display function – CSP dump – SIT display function	ACF/TAP (host)

Note: The maximum of SITs, external and internal, may be eight per NCP.

Restrictions

- The maximum buffer size is 8KB (1KB = 1024 bytes).
- A maximum of four traces per scanner can be started according to the line speed:
  - High-speed line (from 230 kbps for TSS and 1.5 Mbps for HPTSS: Only one trace in a buffer of 8KB.
  - Medium-speed half-duplex line (between 56 kbps and 65 kbps): Two traces maximum in two buffers of 4KB each.
  - Medium-speed duplex line (between 56 kbps and 65 kbps): One trace maximum in a buffer of 8KB.
  - Low-speed line: Four traces in four buffers of 2KB each.
- If an external SIT is running for a given line, an internal SIT cannot be started on this line, and conversely, an external SIT cannot be started when an internal SIT is already running on.

Internal SIT Functions

The internal SIT functions for TSS, HPTSS, or ESS are executable and can be displayed from the MOSS console. (refer to *Service Functions Manual*, SY33-2055, for more information). The different functions are listed in the following section.

- Start
- Cancel
- Freeze
- Resume
- Buffering in scanner in a wrap around mode
- Transferring to the disk or to the RSF
- Display the CSP status on the MOSS screen (It gives the status of the lines which are internally/externally traced, and the number of active lines)
- Investigate the SIT buffer by:

- TSS functions display
- Scanner dump.

Start Internal SIT

This command is used to start the internal trace (issued for any line). The CSP has a limit of 4 concurrent traces per CSP.

If the limit is exceeded, the MOSS trace command will be rejected. (To start and stop the trace, refer to *Service Functions Manual*, SY33-2055, for more information.)

The MOSS trace command on a given interface is used to start the internal trace.

With the 'start trace', the MOSS provides the following parameters:

- Interface address=any interface, odd or even, of the line to be traced.
- Data count=number of bytes of data to be traced for this interface. The data include CSP/FESL control information, but the count designates a number of data characters only.

The CSP will round the data count to the next burst boundary.

Data count = 00 No data to be traced
FF All data to be traced
XX XX bytes of data to be traced.

For HPTSS:

Data count = 00 No data to be traced
FF 40 bytes of data to be traced
XX Up to 40 bytes of data to be traced.

For ESS:

Data count = 00 No data to be traced
FF 42 bytes of data to be traced
XX Up to 252 bytes of data to be traced.

For internal SIT, in case of high-speed lines (256 kbps), the data count should be limited to 40 bytes (X'28'). This to prevent overrun records to be generated in the trace buffer, due to trace data lost.

Only one trace at a time (external or internal) is supported on one line. If a second trace is issued on the same line, the command is rejected. See the following table:

Action	Ext.SIT Already Active	Int.SIT Already Active	No SIT Already Active	Result
Ext.SIT req.	X			SIT rejected (LCS=D4)
Ext.SIT req.		X		SIT rejected (LCS=D2)
Ext.SIT req.			X	SIT started
Int.SIT req.	X			MOSS reject request
Int.SIT req.		X		MOSS warning
Int.SIT req.			X	Internal SIT started

Note: If the command is rejected, MOSS will automatically request a CSP status.

Trace Termination

Disabling the line does not terminate the trace. Error conditions do not terminate the trace either.

The trace is normally ended through the cancel trace command.

For the performances, the restrictions are the same as for the external SIT.

Freeze SIT Buffer Command

The 'freeze' command is used to stop tracing the two interfaces of a line (the SIT buffer is frozen).

The command is rejected by MOSS if an external SIT was active for the specified interface. A warning is generated by MOSS if no SIT was active for this interface. See the following table table.

Action	Ext.SIT Already Active	Int.SIT Already Active	No SIT Already Active	Result
Freeze buffer	X			MOSS reject request
Freeze buffer		X		Internal SIT stopped
Freeze buffer			X	MOSS warning

Resume SIT Buffer Command

The 'resume buffer' command is used to continue the data recording on both interfaces of a line. The command is rejected by MOSS if an external SIT was active for the specified interface. A warning is generated by MOSS if no SIT was active for this interface. See the following table.

Action	Ext.SIT Already Active	Int.SIT Already Active	No SIT Already Active	Result
Resume	X			MOSS reject request
Resume		X		Internal SIT reacti-vated
Resume			X	MOSS warning

Cancel Internal Trace Command

The 'cancel SIT command' is used to stop and erase the data recording on both interfaces of a line (free SIT buffer).

The command is rejected by MOSS if an external SIT was active for the specified interface. A warning is generated by MOSS if no SIT was active for this interface. See the following table.

Action	Ext.SIT Already Active	Int.SIT Already Active	No SIT Already Active	Result
Cancel SIT	X			MOSS reject request
Cancel SIT		X		Internal SIT cancelled
Cancel SIT			X	MOSS warning

CSP Status Display

The 'CSP status display' command gives information to MOSS concerning the number of internal or external SITs, and a list of active line numbers.
This function is accessible through the SIT functions or the customer menu.

Display SIT Buffer

The 'display SIT command' is used to display all the data recorded from both interfaces of a line.

The command is rejected by MOSS if an external SIT was active for the specified interface. A warning is generated by MOSS if no SIT was active for this interface. See the following table.

Action	Ext.SIT Already Active	Int.SIT Already Active	NO SIT Already Active	Result
Display SIT	X			MOSS reject request
Display SIT		X		Internal SIT cancelled
Display SIT			X	MOSS warning

SIT Information Added to F4/F5 Line Dump Data

While F4/F5 command occurs on one traced line, the trace is stopped (SIT buffer is frozen) and the last 100 bytes of SIT information are added to the F4/F5 line dump data. Thus, the last events that occur on a line in error are recorded.

Scanner Microcode Checkpoint Trace

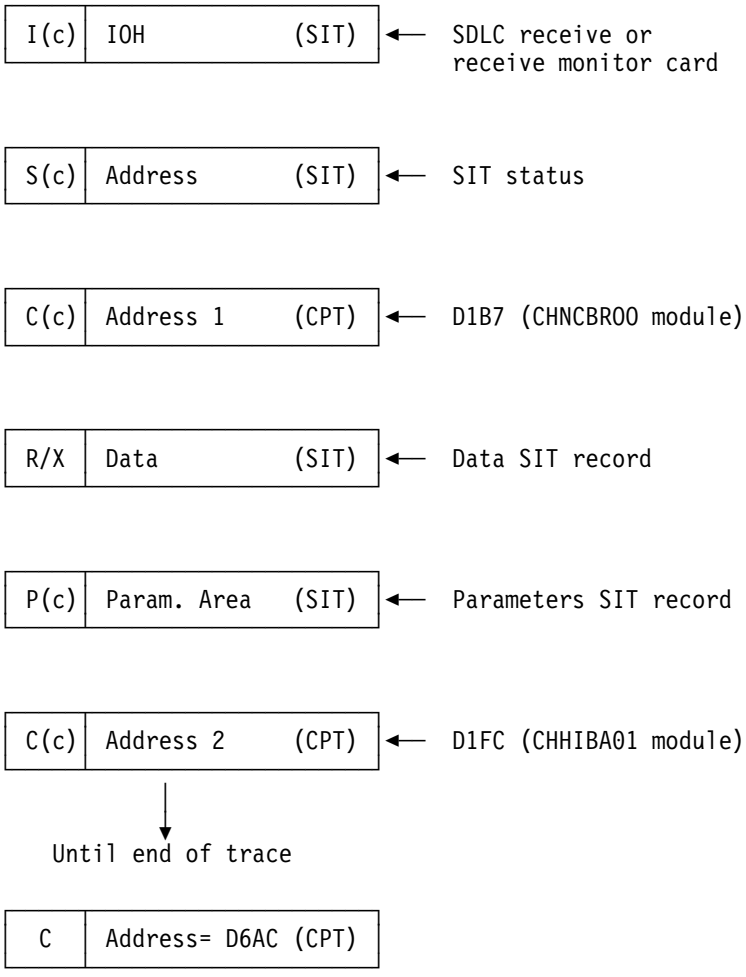
The entry point addresses are used only by the PE, they change with the scanner microcode level.

To start and stop the trace, refer to *Service Functions Manual*, SY33-2055, for the procedure.

Microcode Checkpoint Trace Records

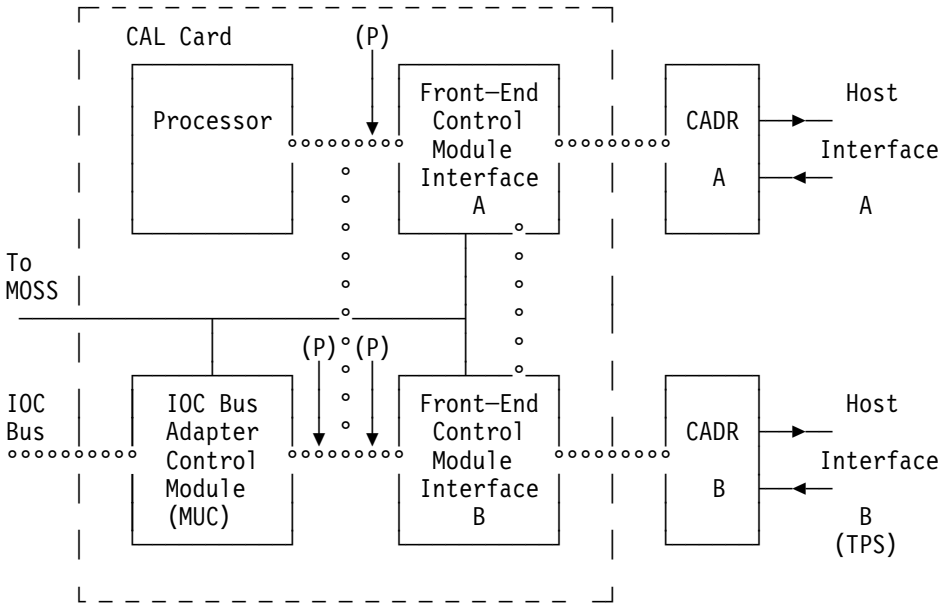
An identifier (C) indicates the data pertaining to the checkpoint trace within the SIT.

The I0H (SIT record) indicates the executed command, and the Address 1 (CPT record) gives the scanner storage address of the module that starts this execution of the command. Then Address 2, (CPT record) indicates the address of the second module in sequence, and so on.



Internal Channel Adapter Trace

The internal channel adapter (CA) trace is started at the same time as the external NCP CA trace and can also be started at the operator console. The internal CA trace captures basic hardware and microcode CA registers located in the channel adapter CA RAM. The following figure locates the points (P) at which, in the logic of the CAL card, the information is captured.



Starting the Internal CA Trace

When the NCP CA trace is started from the host, the NCP automatically starts the internal CA trace. The NCP CA trace and the internal CA trace can be started or stopped manually, via a command entered at the operator console by selecting the start trace function (STT) in the CA services (CAS) functions. For more information see the *Service Functions* manual, SY33-2055.

Stopping the Internal CA Trace

The CA microcode stops the trace on the condition which caused the interrupt level 1 to the NCP or the trace may be stopped manually via a command entered at the operator console by selecting the stop trace function (SPT) in the CA services (CAS) functions.

The NCP creates the BER which is passed to the MOSS. On receipt of this BER the MOSS dumps the CA registers and RAM contents in the reserved dump file area of the disk, when one of the following events occurs:

- After the CA RAM and registers have been dumped, the MOSS restarts the internal CA trace and creates a MOSS BER 'Internal CA trace dump event' which carries the channel adapter number. Refer to "Error Logging", Chapter 12, for description of the channel adapter box event records (BER).
- The disk can contain only one dump per CCU. All subsequent dump requests are ignored. The internal CA trace dump file area becomes available as soon as the dump is transferred to the host, or when the file is deleted by a MOSS console delete function.

Transferring and Editing the Internal CA Trace

The internal CA trace dump file is transferred to the host when the scanner dump is requested (this request also transfers the TIC dumps if any).

The internal CA trace dump is edited in the same way as the MOSS or scanner dump file.

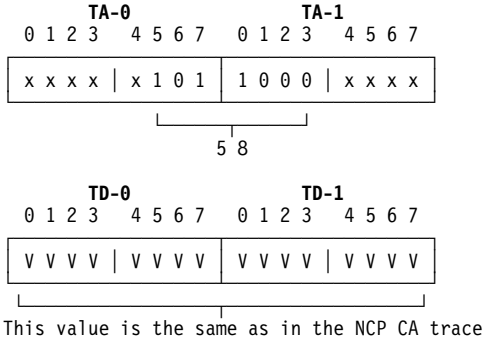
Displaying the Trace Data

The trace area can be displayed at the operator console. See under the CAS functions of the *Service Functions* manual, the display trace data (DTD) or the display storage functions (DST) to display the trace data. (Refer also to the *Advanced Operations Guide* SA33-0097, for more information.)

Correlating Internal CA and NCP CA Traces

A 'trace stamp' is given by the NCP CA trace to the internal CA trace. This 'trace stamp' is identified in the dumps by input X'58' in the NCP CA trace and by the value X'58' in TA-0 bits 5-7 (5), and TA-1 bits 0-3 (8) fields of the PIO interrupt record (command bits). (See note 1 of the PIO Interrupt Record, page 13-34 for CADS, and page 13-45 for BCCA.)

The correlation is given by the same value in the NCP trace as that found in the TD-0 and TD-1 fields, bits 0-7 in the PIO interrupt trace record.



The CA trace locations and data interpretation depend on CA type CADS or BCCA.

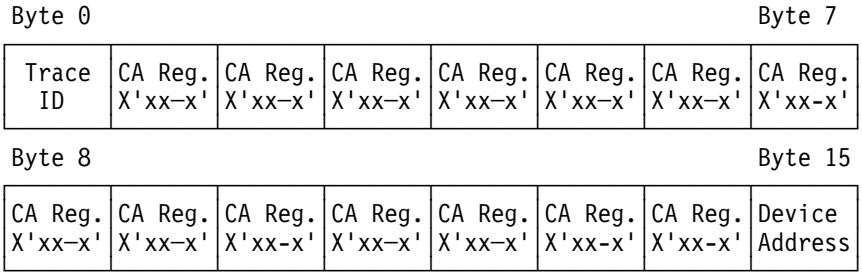
CADS Internal Trace

The internal CA trace save area is thirty-two 16-byte blocks in length. It starts at CA RAM location X'500', and ends at CA RAM location X'6FF'.

When the byte at CA RAM location X'710' is set to 1, the trace is active.

Each internal CA trace entry is 16 bytes long, and the first byte contains the trace ID.

Trace Entry Fields Description



- **Byte 0** is the trace entry and contains the trace identification (trace ID). The trace ID may have different values, and these values identify the trace entry type.

Trace ID	Description
0A	Front-end control module interface A trace entry.
0B	Front-end control module interface B (TPS) trace entry.
mD	IOC bus adapter control module (MUC) trace entry (the m value is microcode (PROM) level-dependent)
0F	Spurious interrupt (ROS parity check) trace entry.
FF	Ignore this trace entry (the inhibit flag has been set).

- **Bytes 1-12** are the contents of CA registers (CA register X'xx').

  When the value of the first 'x' is '2', the contents of the CA register group 2 (channel interface A) are stored in the corresponding fields.

  When the value of the first 'x' is '3', the contents of the CA register group 3 (channel interface B) are stored in the corresponding fields.

  A brief bit description is given under each CA register field. For more details refer to the 'CA Instructions (Register Contents)' topic in the "Channel Adapter (CA)", Chapter 7.

- **Bytes 13-14** may have the following labels: 'Trace1' and 'Trace2' fields.

  The detailed contents of these fields are respectively explained page 13-37 and page 13-38.

- **Byte 15** contains the native subchannel (NSC) or the emulated subchannel (ESC) device address associated with the interrupt.

Front-End Control Module Interrupt Trace (Interfaces A or B)

The contents of the control module interrupt trace entry (interfaces A and B) are described in the following table (the register contents are given in abbreviated form for practical reasons, refer to the "Channel Adapter (CA)", Chapter 7, for a detailed description of those contents):

Byte 0 — Byte 7

Bit	Trace ID	CA Reg. X'x0-0' Interr.	CA Reg. X'xC-0' Data	CA Reg. X'xC-1' Status	CA Reg. X'xD-0' IS	CA Reg. X'xE-0' Tag out	CA Reg. X'xE-1' Tag in	CA Reg. X'xB-0' Command
0	┐	Data	Bus out	0	Bus out	Suppress	Request	Outbound
1	│ 0	Status	Sel.rst	Sel.rst	Sel.rst	Operatnl.	Operatnl	Inbound
2	│	Init.Sel.	Char.rec.	Cmd.chl.	0	Address	Address	Status
3	┘	Host rst.	Cnt.Stop	Stacked	RTS	Command	Status	Alert
4	┐ X'A'	Panel.	DS tmout	Accepted	NSC val.	Service	Service	SOM
5	│ '	Interf.	Chl.stop	Sel.out.	ESC val.	Data out	Data in	Switch
6	│ or	Logic	DLE remb.	SOM	0	Hold out	Disconn.	Busy
7	┘ X'B'	Timer	Halt I/O	Halt I/O	Halt I/O	Select	Select	DS inhib.

Byte 8 — Byte 15

Bit	CA Reg. X'61-0' Flags	CA Reg. X'61-1' Flags	CA Reg. X'62-0' Flags	CA Reg. X'62-1' Flags	CA Reg. X'65-0' State	Trace1	Trace2	Device Address
0	CE remen.	PRI rais.	MUC busy	SR req.				
1	NSC actv.	ESC actv.	MUC wait	0				
2	All enab.	Asynchr.	Set moni.	Force L1				
3	Selected	Temp.bsy.	Rst moni.	PRI req.	See Note 1	See Note 2	See Note 2	See Note 3
4	ESC cmd.	CE sent	0=NI 1=IR	SOM req.				
5	ESC TIO	0=FE 1=O2	IS raisd.	IS req.				
6	NSC stat.	TPS/TCS	DS raisd.	DS req.				
7	Not used	Content.	L1 raisd.	L1 req.				

The value in byte 0 (trace ID) may be X'0A' or X'0B', where 'A' or 'B' identify the front-end control module channel interface traced.

The bit set in byte 1 gives the type of interrupt which has created the trace entry.

Notes:

1. Refer to the 'CA Instructions (Register Contents)' topic in the "Channel Adapter (CA)", Chapter 7 to decode this field.
2. See page 13-37 for the description of these fields.
3. This field contains the NSC or ESC device address associated with the interrupt.

IOC Adapter Control Module Interrupt Trace (IOC Bus)

The value in byte 0 (trace ID) is X'mD', where 'm' depends on the CA microcode (PROM) level, and 'D' means that the IOC control module interrupt is traced.

The bit set in byte 2 (CA X'18-0') identifies the type of interrupt which has created the trace entry. If the value equals X'80', this block is a PIO interrupt trace entry. If the value equals X'40', this block is an AIO interrupt trace entry.

The register contents are given in abbreviated form for practical reasons. Refer to the "Channel Adapter (CA)", Chapter 7, for a detailed description of those contents.

PIO Interrupt Record

Byte 0 — Byte 7

Bit	Trace ID	CA Reg. X'12-0' Sense	CA Reg. X'18-0' Interr.	TA-0 (Note 1)	TA-1 (Note 1)	TD-0 (Note 1)	TD-1 (Note 1)	CA Reg. X'xB-0' Command
0	m	Halt	PIO	Bus 2	Command			Outbound
1	m	Parity	AIO	0	Command			Inbound
2	m	Out excp.	MUC err.	0	Command			Status
3	m	Invalid	Tag rst.	0	Command			Alert
4	X'D'	MUC chck.	Int.req.	1	MOSS			SOM
5	X'D'	Select	0	Command	0			Switch
6	X'D'	Sel.err.	0	Command	Storage			Busy
7	X'D'	Deselect	0	Command	Read			DS inhib.

Byte 8 — Byte 15

Bit	CA Reg. X'61-0' Flags	CA Reg. X'61-1' Flags	CA Reg. X'62-0' Flags	CA Reg. X'62-1' Flags	CA Reg. X'65-0' State	Trace1	Trace2	Device Address
0	CE remen.	PRI rais.	MUC busy	SR req.				
1	NSC actv.	ESC actv.	MUC wait	0				
2	All enab.	Asynchr.	Set moni.	Force L1				
3	Selected	Temp.bsy.	Rst moni.	PRI req.	See Note 2	See Note 3	See Note 3	See Note 4
4	ESC cmd	CE sent	0=NI 1=IR	SOM req.				
5	ESC TIO	0=FE 1=02	IS raisd.	IS req.				
6	NSC stat.	TPS/TCS	DS raisd.	DS req.				
7	Not used	Content.	L1 raisd.	L1 req.				

Notes:

1. TA-0, TA-1, TD-0, and TD-1 respectively correspond to IOC bus bytes 0 and 1 at TA time, and IOC bus bytes 0 and 1 at TD time.

   If the value of the TA-0 field equals X'0D' or X'8D', and the TA-1 field equals X'80', TD-0 and TD-1 contain the trace stamp which correlates the internal and NCP CA traces (refer to “Correlating Internal CA and NCP CA Traces” on page 13-31).

2. Refer to the 'CA Instructions (Register Contents)' topic in the "Channel Adapter (CA)", Chapter 7, to decode this field.

3. See page 13-37 for the description of these fields.

4. This field contains the NSC or ESC device address associated with the interrupt.

AIO Interrupt Record

The register contents are given in abbreviated form for practical reasons. Refer to the "Channel Adapter (CA)", Chapter 7, for a detailed description of those contents.

Byte 0 Byte 7

Bit	Trace ID	CA Reg. X'12-0' Sense	CA Reg. X'18-0' Interr.	MAVLCNT	FEAVLCNT	Burst Byte Count	CA Reg. X'0C-1'	CA Reg. X'xB-0' Command
0	m	Halt	PIO					Outbound
1		Parity	AIO					Inbound
2		Out excp.	MUC err.					Status
3		Invalid	Tag.rst.			See Note 1		Alert
4	X'D'	MUC chck.	Int.req.					SOM
5		Select	0					Switch
6		Sel.err.	0					Busy
7		Deselect	0					DS inhib.

Byte 8 Byte 15

Bit	CA Reg. X'61-0' Flags	CA Reg. X'61-1' Flags	CA Reg. X'62-0' Flags	CA Reg. X'62-1' Flags	CA Reg. X'65-0' State	Trace1	Trace2	Device Address
0	CE remen.	PRI rais.	MUC busy	SR req.				
1	NSC actv.	ESC actv.	MUC wait	0				
2	All enab.	Asynchr.	Set moni.	Force L1				
3	Selected	Temp.bsy.	Rst moni.	PRI req.	See Note 2	See Note 3	See Note 3	See Note 4
4	ESC cmd	CE sent	0=NI 1=IR	SOM req.				
5	ESC TIO	0=FE 1=O2	IS raisd.	IS req.				
6	NSC stat.	TPS/TCS	DS raisd.	DS req.				
7	Not used	Content.	L1 raisd.	L1 req.				

Notes:

1. The **Burst Byte Count** field gives the number of bytes exchanged between the CA and the CCU.
2. Refer to the 'CA Instructions (Register Contents)' topic in the "Channel Adapter (CA)", Chapter 7, to decode this field.
3. See page 13-38 for the description of these fields.
4. This field contains the NSC or ESC device address associated with the interrupt.

Spurious Interrupt Trace

If the spurious interrupt occurred during an operation on interface A or interface B, the following trace is recorded.

The register contents are given in abbreviated form for practical reasons. Refer to the "Channel Adapter (CA)", Chapter 7, for a detailed description of those contents.

Byte 0 — Byte 7

Bit	Trace ID	CA Reg. X'2F-1' Interr.	CA Reg. X'3F-1' Data	NA	NA	CA Reg. X'xE-0' Tag out	CA Reg. X'xE-1' Tag in	CA Reg. X'xB-0' Command
0	0	Syn.cnt1	Syn.cnt1.			Suppress	Request	Outbound
1	0	Syn.cnt2	Syn.cnt2.			Operatnl.	Operatnl	Inbound
2	0	Addr.rem	Addr.rem.			Address	Address	Status
3	0	DI/DO	DI/DO			Command	Status	Alert
4	X'F'	SI/SO	SI/SO			Service	Service	SOM
5	X'F'	0	0			Data out	Data in	Switch
6	X'F'	Op.out	Op.out			Hold out	Disconn.	Busy
7	X'F'	Int.req.	Int.req.			Select	Select	DS inhib.

Byte 8 — Byte 15

Bit	CA Reg. X'61-0' Flags	CA Reg. X'61-1' Flags	CA Reg. X'62-0' Flags	CA Reg. X'62-1' Flags	CA Reg. X'65-0' State	Trace1	Trace2	Device Address
0	CE remen.	PRI rais.	MUC busy	SR req				
1	NSC actv.	ESC actv.	MUC wait	0				
2	All enab.	Asynchr.	Set moni.	Force L1				
3	Selected	Temp.bsy.	Rst moni.	PRI req.	See Note 1	See Note 2	See Note 2	See Note 3
4	ESC cmd	CE sent	0=NI 1=IR	SOM req.				
5	ESC TIO	0=FE 1=O2	IS raisd.	IS req.				
6	NSC stat.	TPS/TCS	DS raisd.	DS req.				
7	Not used	Content.	L1 raisd.	L1 req.				

Notes:

1. Refer to the 'CA Instructions (Register Contents)' topic in the "Channel Adapter (CA)", Chapter 7, to decode this field.
2. See page 13-37 for the description of these fields.
3. This field contains the NSC or ESC device address associated with the spurious interrupt.

Trace1 and Trace2 Fields (CADS)

Trace1 and the **Trace2** are interrupt-dependent fields. When either or both of these fields have the value X'FF', they are non significant. They may have the following contents:

Interrupt Types	Trace1 Field	Trace2 Field
Autoselect interrupt	CA Reg. X'0F–0'	CA Reg. X'0F–1'
CA microcode error	CA Reg. X'60–0'	CA Reg. X'60–1'
Data interrupt	Count1 (Note 1)	Count2 (Note 1)
Front–end module logic error	CA Reg. X'5x–0' (Note 2)	CA Reg. X'5x–1' (Note 2)
IOC bus control module check	CA Reg. X'50–0'	CA Reg. X'50–1'
Invalid command	CA Reg. X'16–0'	CA Reg. X'10–0'
Initial selection	Command (Note 3)	Initial Status (Note 3)
Level 1 interrupt	CA Reg. X'0D–0'	CA Reg. X'0D–1'
Out X'09' or X'0A'	CA Reg. X'14–0'	NA
Outbound or inbound AIO	CA Reg. X'0C–0'	CA Reg. X'0C–1'
Outbound or inbound PIO	CA Reg. X'04–0'	CA Reg. X'04–1'
Reset data status	CA Reg. X'02–0'	CA Reg. X'02–1'
Status transfer	Status	NA
Status interrupt	ActionA (Note 4)	ActionB (Note 4)

Notes:

1. The **Count1** and **Count2** contents are explained in the following table.
2. Depending on the interface traced, the contents of these fields come from, either X'51' for interface A, or X'52' for interface B.
3. **Command** and **Status Fields**

For the bit meanings of these fields refer to the paragraph “NCP Channel Command Information” on page 13-52.

4. See the **ActionA** and **ActionB** field description in the following section:

Bit	ActionA Field	ActionB Field
x...	Raise IS level 3	Not used
.x..	Raise DS level 3	Not used
..x.	Set NSC active	Reset CE remember and CE sent
...x	Set CE remember	Not used
.... x...	Update CA register X'0B' and test I/O status available	Reset NSC active
.... .x..	Set ESC address active	Not used
.... ..x.	Set status byte 'cleared'	Not used
....x	Ignore status 'stacked'	Not used

Count1 Field

In inbound operations (host-to-CCU), the Count1 field (byte 13) contains the number of bytes left to be sent to the CCU.

In outbound operations (CCU-to-host), it contains the number of bytes remaining to be received from the CCU.

Count2 Field

In inbound operations (host-to-CCU), the Count2 field (byte 14) contains the number of bytes left to be received from the host.

In outbound operations (CCU-to-host), it contains the number of bytes remaining to be sent to the host.

BCCA Internal Trace

The internal CA trace save area is 128 times 16-byte blocks in length, starting at CA RAM location X'800', and ending at CA RAM location X'FFF'.
When the byte at CA RAM location X'710' is set to 1, the trace is active, and when it is set to 0, the trace is inactive.
Each internal CA trace entry is 16 bytes long, and the first byte contains the trace ID.

Trace Entry Fields Description

Byte 0							Byte 7
Trace ID	CA Reg. X'xx–x'	CA Reg. X'xx–x'	CA Reg. X'xx–x'	CA Reg. X'xx–x'	CA Reg. X'xx–x'	CA Reg. X'xx–x'	CA Reg. X'xx-x'

Byte 8							Byte 15
CA Reg. X'xx–x'	CA Reg. X'xx–x'	CA Reg. X'xx-x'	CA Reg. X'xx–x'	CA Reg. X'xx–x'	CA Reg. X'xx-x'	CA Reg. X'xx-x'	Device Address

- **Byte 0** is the trace entry and contains the trace identification (trace ID). The trace ID may have different values, and these values identify the trace entry type.

Trace ID	Description
1A	Front-end control module interface A trace entry, buffer chaining mode OFF.
2A	Front-end control module interface A trace entry, buffer chaining mode ON.
1B	Front-end control module interface B (TPS) trace entry, buffer chaining mode OFF.
2B	Front-end control module interface B (TPS) trace entry, buffer chaining mode ON.
m1	IOC bus adapter control module (MUC) trace entry when the BC mode is OFF (the m value is microcode (PROM) level-dependent).
m2	IOC bus adapter control module (MUC) trace entry when the BC mode is ON (the m value is microcode (PROM) level-dependent).
0F	Spurious interrupt (ROS parity check) trace entry.
FE	First available entry after the trace has been stopped (this particular entry is 4 blocks long and it is described on page 13-51.
FF	Ignore this trace entry (the inhibit flag has been set).

- **Bytes 1-14** are the contents of CA registers (CA register X'xx').

  When the value of the first 'x' is '2', the contents of the CA register group 2 (channel interface A) are stored in the corresponding fields.

  When the value of the first 'x' is '3', the contents of the CA register group 3 (channel interface B) are stored in the corresponding fields.

A brief bit description is given under each CA register field. For more details refer to the 'CA Instructions (Register Contents)' topic in the "Channel Adapter (CA)", Chapter 7.

- **Byte 15** contains the native subchannel (NSC) or the emulated subchannel (ESC) device address associated with the interrupt.

Front-End Control Module Interrupt Trace (Interfaces A or B) (Buffer Chaining OFF)

The contents of the control module interrupt trace entry (interfaces A and B) are described in the following table (the register contents are given in abbreviated form for practical reasons, refer to the "Channel Adapter (CA)", Chapter 7, for a detailed description of those contents):

Byte 0 — Byte 7

Bit	Trace ID	CA Reg. X'x0-0' Interr.	CA Reg. X'xC-0' Data	CA Reg. X'xC-1' Status	CA Reg. X'xD-0' IS	CA Reg. X'xE-0' Tag out	CA Reg. X'xE-1' Tag in	CA Reg. X'xB-0' Command
0	1	Data	Bus out	0	Bus out	Suppress	Request	Outbound
1		Status	Sel.rst	Sel.rst	Sel.rst	Operatnl.	Operatnl	Inbound
2		Init.Sel.	0	Cmd.chn.	0	Address	Address	Status
3		Host rst.	Cnt.Stop	Stacked	RTS	Command	Status	Alert
4	X'A'	Panel.	DS tmout	Accepted	NSC val.	Service	Service	SOM
5	'	Interf.	Chl.stop	Sel.out.	0	Data out	Data in	Switch
6	or	Logic	0	SOM	0	Hold out	Disconn.	Busy
7	X'B'	Timer	Halt I/O	Halt I/O	Halt I/O	Select	Select	DS inhib.

Byte 8 — Byte 15

Bit	CA Reg. X'61-0' Flags	CA Reg. X'61-1' Flags	CA Reg. X'62-0' Flags	CA Reg. X'62-1' Flags	CA Reg. X'65-0' State	Trace1	Trace2	Device Address
0	CE remen.	PRI rais.	MUC busy	SR req.				
1	NSC actv.	0	MUC wait	0				
2	All enab.	Asynchr.	Set moni.	Force L1				
3	Selected	Temp.bsy.	Rst moni.	PRI req.	See Note 1	See Note 2	See Note 2	See Note 3
4	0	CE sent	0=NI 1=IR	SOM req.				
5	0	0=FE 1=O2	IS raisd.	IS req.				
6	NSC stat.	TPS/TCS	DS raisd.	DS req.				
7	Not used	Content.	L1 raisd.	L1 req.				

The value in byte 0 (trace ID) may be X'0A' or X'0B', where 'A' or 'B' identify the front-end control module channel interface traced.

The bit set in byte 1 gives the type of interrupt which has created the trace entry.

Notes:

1. Refer to the 'CA Instructions (Register Contents)' topic in the "Channel Adapter (CA)", Chapter 7 to decode this field.
2. See page 13-42 for the description of these fields.
3. This field contains the NSC or ESC device address associated with the interrupt.

Trace1 and Trace2 Fields (BCCA)

Trace1 and the **Trace2** are interrupt-dependent fields. When either or both of these fields have the value X'FF', they are non significant. They may have the following contents:

Interrupt Types	Trace1 Field	Trace2 Field
Initial selection	Command	Status
Request to switch	CA Reg. X'64-0'	FE03
Status transfer	ActionA	ActionB
Data interrupt	FBYTECNT	MBYTECNT
FE logic error	FE0A	FE0B
Host reset	FE1B	X'FFF'
Panel interrupt	FE1B	X'FFF'
Level 1 interrupt	CA Reg. X'0D-0'	CA Reg. X'0D-1'
Microcode detected error	CA Reg. X'60-0'	CA Reg. X'60-1'

Front-End Control Module Interrupt Trace (Interfaces A or B) (Buffer Chaining ON)

The contents of the control module interrupt trace entry (interfaces A and B) are described in the following table (the register contents are given in abbreviated form for practical reasons, refer to the "Channel Adapter (CA)", Chapter 7, for a detailed description of those contents):

Byte 0 — Byte 7

Bit	Trace ID	CA Reg. X'x0-0' Interr.	CA Reg. X'xC-0' Data	CA Reg. X'xC-1' Status	CA Reg. X'xD-0' IS	CA Reg. X'xE-0' Tag out	CA Reg. X'xE-1' Tag in	CA Reg. X'xB-0' Command
0	2	Data	Bus out	0	Bus out	Suppress	Request	Outbound
1	2	Status	Sel.rst	Sel.rst	Sel.rst	Operatnl.	Operatnl	Inbound
2	2	Init.Sel.	0	Cmd.chn.	0	Address	Address	Status
3	2	Host rst.	Cnt.Stop	Stacked	RTS	Command	Status	Alert
4	X'A'	Panel.	DS tmout	Accepted	NSC val.	Service	Service	SOM
5	X'A'	Interf.	Chl.stop	Sel.out.	0	Data out	Data in	Switch
6	or	Logic	0	SOM	0	Hold out	Disconn.	Busy
7	X'B'	Timer	Halt I/O	Halt I/O	Halt I/O	Select	Select	DS inhib.

Byte 8 — Byte 15

Bit	CA Reg. X'61-0' Flags	CA Reg. X'61-1' Flags	CA Reg. X'62-0' Flags	CA Reg. X'62-1' Flags	CA Reg. X'65-0' State	Trace1	Trace2	BCCAFLAG
0	CE remen.	PRI rais.	MUC busy	SR req.	See Note 1	See Note 2	See Note 2	See Note 3
1	NSC actv.	0	MUC wait	0				
2	All enab.	Asynchr.	Set moni.	Force L1				
3	Selected	Temp.bsy.	Rst moni.	PRI req.				
4	0	CE sent	0=NI 1=IR	SOM req.				
5	0	0=FE 1=O2	IS raisd.	IS req.				
6	NSC stat.	TPS/TCS	DS raisd.	DS req.				
7	Not used	Content.	L1 raisd.	L1 req.				

The value in byte 0 (trace ID) may be X'0A' or X'0B', where 'A' or 'B' identify the front-end control module channel interface traced.

The bit set in byte 1 gives the type of interrupt which has created the trace entry.

Notes:

1. Refer to the 'CA Instructions (Register Contents)' topic in the "Channel Adapter (CA)", Chapter 7 to decode this field.
2. See page 13-42 for the description of these fields.
3. This field is described in the following section.

BCCAFLAG Description

Bit	Description
x...	BCCA mode
.x..	EODR
..x.	FIRST
...x	MUC_NDAI
.... x...	FE_NDAI
.... .x..	Availability flag for data area 0
.... ..x.	Availability flag for data area 1
....x	IN_OUT

IOC Adapter Control Module Interrupt Trace (IOC Bus)

The value in byte 0 (trace ID) is X'm1' or X'm2', where 'm' depends on the CA microcode (PROM) level, and '1' or '2' means that the IOC control module interrupt is traced.

The bit set in byte 2 (CA X'18-0') identifies the type of interrupt which has created the trace entry. If the value equals X'80', this block is a PIO interrupt trace entry. If the value equals X'40', this block is an AIO interrupt trace entry.

The register contents are given in abbreviated form for practical reasons. Refer to the "Channel Adapter (CA)", Chapter 7, for a detailed description of those contents.

PIO Interrupt Record

Byte 0 — Byte 7

Bit	Trace ID	CA Reg. X'12-0' Sense	CA Reg. X'18-0' Interr.	TA-0 (Note 1)	TA-1 (Note 1)	TD-0 (Note 1)	TD-1 (Note 1)	CA Reg. X'xB-0' Command
0	m	Halt	PIO	Bus 2	Command			Outbound
1	m	Parity	AIO	0	Command			Inbound
2	m	Out excp.	MUC err.	0	Command			Status
3	m	Invalid	Tag rst.	0	Command			Alert
4	X'1'	MUC chck.	Int.req.	1	MOSS			SOM
5	X'1'	Select	0	Command	0			Switch
6	X'1'	Sel.err.	0	Command	Storage			Busy
7	X'1'	Deselect	0	Command	Read			DS inhib.

Byte 8 — Byte 15

Bit	CA Reg. X'61-0' Flags	CA Reg. X'61-1' Flags	CA Reg. X'62-0' Flags	CA Reg. X'62-1' Flags	CA Reg. X'65-0' State	Trace1	Trace2	Trace3
0	CE remen.	PRI rais.	MUC busy	SR req.				
1	NSC actv.	0	MUC wait	0				
2	All enab.	Asynchr.	Set moni.	Force L1				
3	Selected	Temp.bsy.	Rst moni.	PRI req.	See Note 2	See Note 3	See Note 3	See Note 4
4	0	CE sent	0=NI 1=IR	SOM req.				
5	0	0=FE 1=O2	IS raisd.	IS req.				
6	NSC stat.	TPS/TCS	DS raisd.	DS req.				
7	Not used	Content.	L1 raisd.	L1 req.				

Notes:

1. TA-0, TA-1, TD-0, and TD-1 respectively correspond to IOC bus bytes 0 and 1 at TA time, and IOC bus bytes 0 and 1 at TD time.

   If the value of the TA-0 field equals X'0D' or X'8D', and the TA-1 field equals X'80', TD-0 and TD-1 contain the trace stamp which correlates the internal and NCP CA traces (refer to “Correlating Internal CA and NCP CA Traces” on page 13-31).

2. Refer to the 'CA Instructions (Register Contents)' topic in the "Channel Adapter (CA)", Chapter 7, to decode this field.

3. The contents of the **Trace1** and **Trace2** fields is described page 13-42.

4. The contents of the **Trace3** field depends on the interrupt type and is described in the following table.

Trace3 Contents Description

Interrupt Types	Trace3 Field
OUT02 data transfer buffer chaining	BCCAFLAG
All other cases	Address

AIO Interrupt Record (Buffer Chaining OFF): The register contents are given in abbreviated form for practical reasons. Refer to the "Channel Adapter (CA)", Chapter 7, for a detailed description of those contents.

Byte 0 ... Byte 7

Bit	Trace ID	CA Reg. X'12-0' Sense	CA Reg. X'18-0' Interr.	MAVLCNT	FEAVLCNT	Burst Byte Count	CA Reg. X'0C-1'	CA Reg. X'xB-0' Command
0	m	Halt	PIO					Outbound
1		Parity	AIO					Inbound
2		Out excp.	MUC err.					Status
3		Invalid	Tag.rst.			See Note 1		Alert
4	X'1'	MUC chck.	Int.req.					SOM
5		Select	0					Switch
6		Sel.err.	0					Busy
7		Deselect	0					DS inhib.

Byte 8 ... Byte 15

Bit	CA Reg. X'61-0' Flags	CA Reg. X'61-1' Flags	CA Reg. X'62-0' Flags	CA Reg. X'62-1' Flags	CA Reg. X'65-0' State	Trace1	Trace2	Device Address
0	CE remen.	PRI rais.	MUC busy	SR req.				
1	NSC actv.	0	MUC wait	0				
2	All enab.	Asynchr.	Set moni.	Force L1				
3	Selected	Temp.bsy.	Rst moni.	PRI req.	See Note 2	See Note 3	See Note 3	See Note 4
4	0	CE sent	0=NI 1=IR	SOM req.				
5	0	0=FE 1=O2	IS raisd.	IS req.				
6	NSC stat.	TPS/TCS	DS raisd.	DS req.				
7	Not used	Content.	L1 raisd.	L1 req.				

Notes:

1. The **Burst Byte Count** field gives the number of bytes exchanged between the CA and the CCU.
2. Refer to the 'CA Instructions (Register Contents)' topic in the "Channel Adapter (CA)", Chapter 7, to decode this field.
3. See page 13-42 for the description of these fields.
4. This field contains the NSC or ESC device address associated with the interrupt.

AIO Interrupt Record (Buffer Chaining ON): The register contents are given in abbreviated form for practical reasons. Refer to the "Channel Adapter (CA)", Chapter 7, for a detailed description of those contents.

Byte 0 Byte 7

Bit	Trace ID	CA Reg. X'12-0' Sense	CA Reg. X'18-0' Interr.	MUCSTAT	(A)	(B)	(C)	CA Reg. X'xB-0' Command
0	m	Halt	PIO					Outbound
1		Parity	AIO					Inbound
2		Out excp.	MUC err.					Status
3		Invalid	Tag.rst.	See Note 2	See Note 2	See Note 2	See Note 2	Alert
4	X'2'	MUC chck.	Int.req.					SOM
5		Select	0					Switch
6		Sel.err.	0					Busy
7		Deselect	0					DS inhib.

Byte 8 Byte 15

Bit	CA Reg. X'61-0' Flags	CA Reg. X'61-1' Flags	CA Reg. X'62-0' Flags	CA Reg. X'62-1' Flags	CA Reg. X'65-0' State	MUCSTAT	Trace2	BCCAFLAG
0	CE remen.	PRI rais.	MUC busy	SR req.				
1	NSC actv.	0	MUC wait	0				
2	All enab.	Asynchr.	Set moni.	Force L1				
3	Selected	Temp.bsy.	Rst moni.	PRI req.	See Note 1	See Note 2	See Note 2	
4	0	CE sent	0=NI 1=IR	SOM req.				
5	0	0=FE 1=O2	IS raisd.	IS req.				
6	NSC stat.	TPS/TCS	DS raisd.	DS req.				
7	Not used	Content.	L1 raisd.	L1 req.				

Notes:

1. Refer to the 'CA Instructions (Register Contents)' topic in the "Channel Adapter (CA)", Chapter 7, to decode this field.
2. The values of the fields **(A)**, **(B)**, **(C)**, and **Trace2** depend on the **MUCSTAT** value as described in the following section.

MUCSTAT Value Description

MUCSTAT	(A) Field	(A) Field	(A) Field	Trace2 Field
1	CBA1	CBA2	CBA3	AGSTAT
2	NBA1	NBA2	NBA3	X'FFF'
3	NPA1	NPA2	NPA3	COUNT
4	NBA1	NBA2	NBA3	X'FFF'
5	NBA1	NBA2	NBA3	X'FFF'
6	CBA1	CBA2	CBA3	AGSTAT
7	NBA1	NBA2	NBA3	X'FFF'
8	X'FFF'	X'FFF'	X'FFF'	MBRSTCNT
9	NBA1	NBA2	NBA3	X'FFF'
A	NCP_ADD1	NCP_ADD2	NCP_ADD3	CP0C-1

Spurious Interrupt Trace

If the spurious interrupt occurred during an operation on interface A or interface B, the following trace is recorded.

The register contents are given in abbreviated form for practical reasons. Refer to the "Channel Adapter (CA)", Chapter 7, for a detailed description of those contents.

Byte 0 — Byte 7

Bit	Trace ID	CA Reg. X'2F-1' Interr.	CA Reg. X'3F-1' Data	NA	NA	CA Reg. X'xE-0' Tag out	CA Reg. X'xE-1' Tag in	CA Reg. X'xB-0' Command
0	0	Syn.cnt1	Syn.cnt1.			Suppress	Request	Outbound
1	0	Syn.cnt2	Syn.cnt2.			Operatnl.	Operatnl	Inbound
2	0	Addr.rem	Addr.rem.			Address	Address	Status
3	0	DI/DO	DI/DO			Command	Status	Alert
4	X'F'	SI/SO	SI/SO			Service	Service	SOM
5	X'F'	0	0			Data out	Data in	Switch
6	X'F'	Op.out	Op.out			Hold out	Disconn.	Busy
7	X'F'	Int.req.	Int.req.			Select	Select	DS inhib.

Byte 8 — Byte 15

Bit	CA Reg. X'61-0' Flags	CA Reg. X'61-1' Flags	CA Reg. X'62-0' Flags	CA Reg. X'62-1' Flags	CA Reg. X'65-0' State	FE0A	FE0B	NA
0	CE remen.	PRI rais.	MUC busy	SR req.				
1	NSC actv.	0	MUC wait	0				
2	All enab.	Asynchr.	Set moni.	Force L1				
3	Selected	Temp.bsy.	Rst moni.	PRI req.	See Note 1			
4	0	CE sent	0=NI 1=IR	SOM req.				
5	0	0=FE 1=O2	IS raisd.	IS req.				
6	NSC stat.	TPS/TCS	DS raisd.	DS req.				
7	Not used	Content.	L1 raisd.	L1 req.				

Notes:

1. Refer to the 'CA Instructions (Register Contents)' topic in the "Channel Adapter (CA)", Chapter 7, to decode this field.

Stop Trace Entry Description

The stop trace entry is four 16-byte blocks long and has the following format and contents.

X'FE'	X'60–0'	X'60–1'	X'2D–1'	X'2E'-0	X'2E'-1	X'3E'-0	X'3E'-1
X'50–0'	X'50–1'	X'51–0'	X'51–1'	X'52–0'	X'52–1'	X'x5'-0	X'x5'-1

X'2A–0'	X'2B–1'	X'2F–1'	X'26–0'	X'26–1'	X'2B–0'	X'64–0'	X'64–1'
X'3A–0'	X'3B–1'	X'3F–1'	X'36–0'	X'36–1'	X'3B–0'	X'74–0'	X'74–1'

X'00–0'	X'01–0'	X'01–1'	X'02–0'	X'02–1'	X'03–0'	X'03–1'	X'04–0'
X'04–1'	X'05–0'	X'05–1'	X'06–1'	X'07–0'	X'07–1'	X'08–0'	X'08–1'

X'0C–0'	X'0C–1'	X'0D–0'	X'0D–1'	X'0E–0'	X'0E–1'	X'0F–0'	X'0F–1'
X'10–0'	X'10–1'	X'11–0'	X'12–0'	X'14–0'	X'16–1'	X'17–0'	X'FF'

Field 'FE' (byte 0) identifies the last trace entry, and field 'FF' (byte 63) identifies the end of the 'FE' trace.

The other fields give the contents of the specified CA registers.

NCP Channel Command Information

Command Code	Command Name	Description
X'00'	TIO	Requests the 3745 to present pending status.
X'01'	Write	The write command is initiated to the NCP. Data in the host processor main storage is transferred to the NCP.
X'02'	Read	The read command is initiated at the NCP. Data at controller storage are transferred to host processor main storage.
X'03'	No-Op	This command is required as the last CCW in a read or write CCW chain.
X'04'	Sense	The host initiates this command. One byte of sense data is transferred to the host.
X'05'	Write IPL	Host command to the 3745 indicating that an NCP/PEP/EP is to be loaded.
X'09'	Write break	The write break command is identical to the write command except that it indicates that it is the last or only write command in a chain of write CCWs.
X'31'	Write start 0	This is the first command expected in the write channel program after IPL of the NCP. It is also expected after each successful write start 1 command.
X'32'	Read start 0	This is the first command expected in the write channel program after IPL of the NCP. It is also expected after each successful read start 1 command.
X'51'	Write start 1	This is the second command expected in the write channel program after IPL of the NCP. It is also expected after each successful read start 0 command.
X'52'	Read start 1	This is the second command expected in the read channel program after IPL of the NCP. It is also expected after each successful read start 0 command.
X'61'	WXID	The host sends the write XID command to signal NCP that a channel contact sequence is beginning and to prepare to receive the host's XID.
X'62'	RXID	The host sends the write XID command to signal NCP that a channel contact sequence is beginning and to prepare to receive the host's XID.
X'72'	Read configuration data	When a read configuration data (RCD) CCW is executed by the channel, the BCCA returns an initial status of X'00' with an associated count of X'CO', a sense ID X'E4' command, and also interrupts the NCP. Then the NCP returns to the host: • A node element descriptor (NED) for the I/O device • Two specific node element qualifiers (NEQ) • A node element descriptor (NED) for the control unit • A token node element descriptor (NED) • A general node element qualifier (NEQ) For more details, refer to the sense ID X'E4' command in this table and to the paragraph “Extended Sense Identification” on page 13-53.
X'93'	Reset restart	This command causes the NCP to reset its switches to indicate that the last write start and read start commands were write start 1 and read start 1.
X'A3'	Discontact	This command tells the NCP to exit the contacted state with the host. The host: • Indicates that the channel is no longer contacted. • Indicates that attachment to the transmission group should be broken. • Releases PIUs on the channel hold and the intermediate queues.
X'C3'	Contact	This command tells the NCP to set up for operation with the host identification data.

Command Code	Command Name	Description
X'E4'	Sense ID	This command requests the machine type and model number the NCP returns to the host in CADS mode and in addition the command-information word in BCCA mode: • In CADS mode four bytes X'FF 37 45 0x', (x=0 for models 1xx, x=1 for models 21x/31x or x=2 for models 41x/61x) • In BCCA mode twelve bytes X'FF 37 45 0x 00 00 00 00 40 72 00 C0' (the last four bytes form the command information word). For more details, refer to the RCD X'72' command in this table and to the paragraph “Extended Sense Identification” on page 13-53.

Note: Data transfer does not occur on read start and write start commands.

Extended Sense Identification

The information returned to a sense identification (sense ID) CCW by the NCP consists of four bytes given by the MOSS: X'FF374501' for a 3745 model 21x, or X'FF374502' for a model 41x. But for a CA type 7 (BCCA), the NCP transfers twelve bytes. The above four bytes is followed by four bytes of zeroes, and a command-information (four bytes) with the following layout:

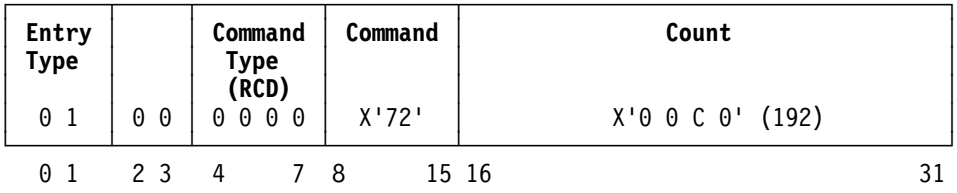


Figure 13-2. The Extended-Identification Information. The command type 0 indicates read configuration data.

The command field gives the hexadecimal value that the channel put in the CCW command field to execute a read configuration data (RCD) command to this device (this value may differ from device to device). The count of 192 indicates that three node-element descriptors (NEDs) and three node-elements qualifiers (NEQs), each having 32 bytes length, are transferred to the host when an RCD command is executed.

Read Configuration Data (RCD)

When the read configuration data CCW is executed by the channel, the BCCA returns an initial status of X'00' and interrupts the NCP. The NCP returns the following information:

- A node-element descriptor (NED) for the I/O device,
- Two specific node-element qualifiers (NEQ),
- A NED for the control unit,
- A token NED,
- A general NEQ.

The general format of the configuration data is the following:

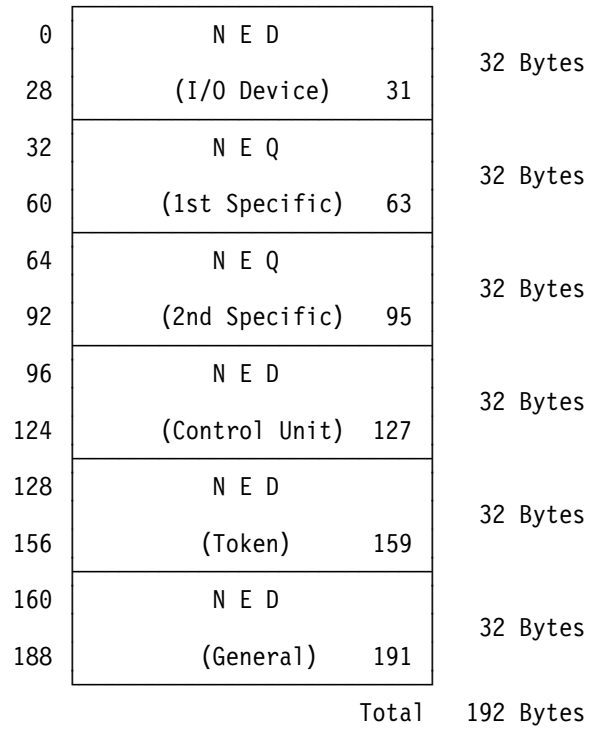


Figure 13-3. The General Format of the Configuration Data

Node-Element Descriptor (NED)

A NED has the following layout:

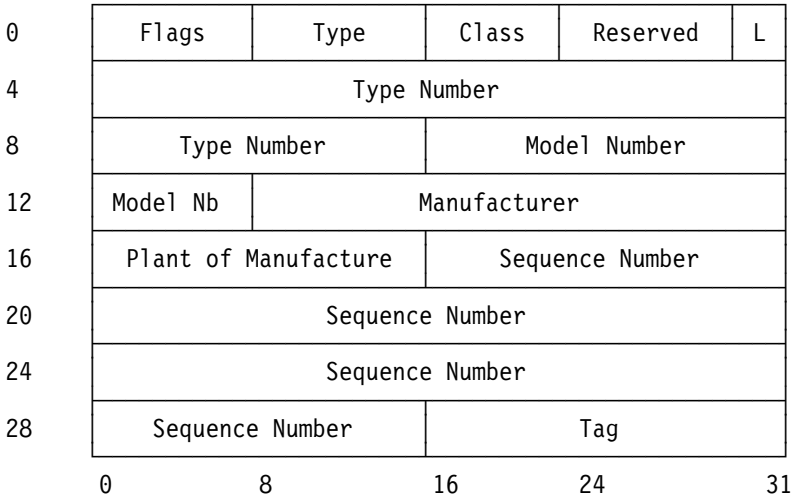


Figure 13-4. The Node-Element Descriptor

The Specific Node-Element Qualifiers (NEQ)

A specific node-element qualifier (NEQ) contains device-dependent configuration information.

The First Specific NEQ

The first specific NEQ contains the SYSGEN NCP values. It has the following format:

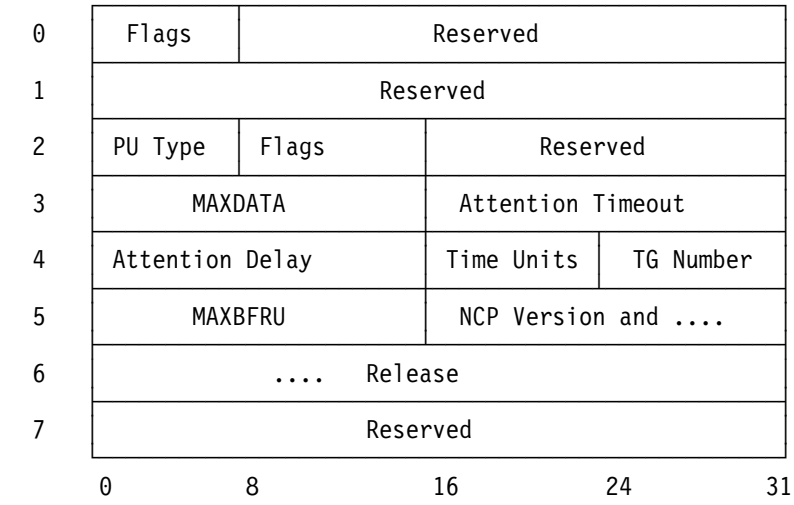


Figure 13-5. The First Specific Node-Element Qualifier (NEQ)

The Second Specific NEQ

The second specific NEQ contains either the values currently in use or the host values and it has the following format:

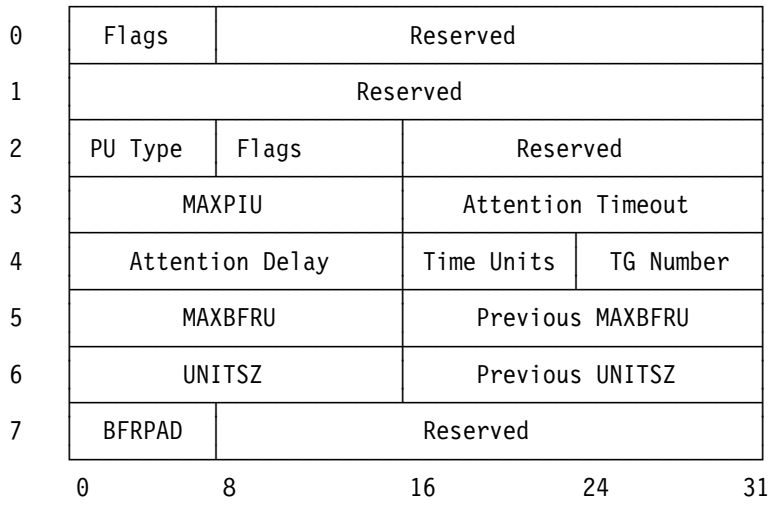


Figure 13-6. The Second Specific Node-Element Qualifier (NEQ)

The General Node-Element Qualifier (NEQ)

The general node-element qualifier (NEQ) contains the control unit and the I/O device configuration information (node-elements) described in the configuration record. It has the following format:

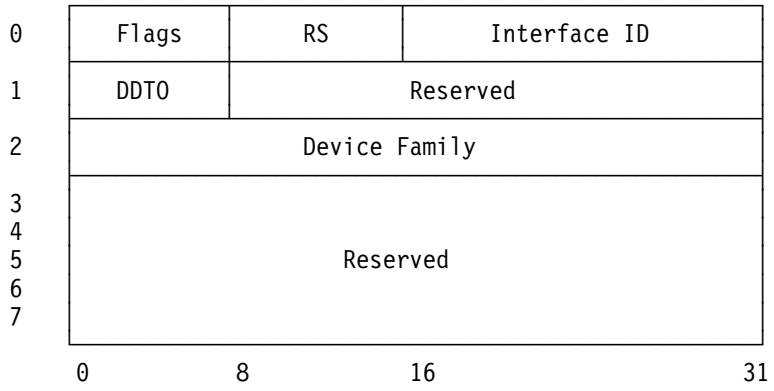


Figure 13-7. The General-Node Element Qualifier (NEQ)

NCP Sense Information

Sense Bits	Error	Probable Cause	Error Description
0	Command reject	Host program failure	Command reject. The control unit has detected an invalid command from the channel.
1	Intervention required	Program failure	Intervention required. The control unit has detected an internal programming error.
2	Bus out check	Channel failure	Bus out check. The control unit has detected data from the channel that is not in proper parity.
3	Equipment check	I/O control unit failure	Equipment check. The control unit has detected an internal hardware error.
4	Data check	Host program failure	Data check. Host buffer too small, PIU incorrect, possibly caused by halt I/Os or channel errors.
5	Overrun	I/O control unit failure or channel failure	Overrun. Data rate exchange between the 3745 and the channel either too high or too low
6	Not initialized	Host program failure	Not initialized. The control unit doe snot have a control program loaded.
7	Abort	I/O control unit failure	Abort. The control unit has halted its channel operation abnormally (automatic network shutoff)

EP Channel Commands

Command Code	Command Name	Description
X'00'	TIO	Requests pending status for addressed line.
X'01'	Write	Data from the host is transferred to the addressed EP line
X'02'	Read	Data from the addressed EP line is transferred to the host
X'03'	No-Op	This command is sent from the host to the 3745. The 3745 responds with an immediate CE+DE; or, if an initial selection is present or, if a programmed interrupt is pending, short busy is presented.
X'04'	Sense	A byte of sense data pertaining to the addressed EP line is transferred to the host.
X'05'	Diag write	This command is treated by EP as an No-Op
X'05'	Write IPL	Host command to the 3745 indicating that an NCP/PEP/EP is to be loaded.
X'06'	Prepare	When a wake-up or line break signal is received on the line addressed by the prepare command, the command is terminated by a CE+DE.
X'09'	Poll	This command causes EP to request polling characters from the host.
X'0A'	Inhibit	An X'02' operation is performed except that line time out is inhibited.
X'0D'	Break	A break signal is sent over the addressed EP line.
X'0E'	Search	Data from the addressed communication line is not transferred to the host except for characters of an ending sequence. This command is valid only if the CSP controlling the line is in emulation mode.
X'12'	Diag read	This command is treated by EP as a No-Op.

Command Code	Command Name	Description
X'13'	SAD zero Set addr0	This command is treated by EP as a No-Op.
X'17'	SAD zero Set addr1	This command is treated by EP as a No-Op.
X'19'	Poll SOH	An X'09' operation is performed except that an SOH character is sent to the addressed line before the poll characters.
X'1B'	SAD two Set addr2	This command is treated by EP as a No-Op.
X'1D'	Diag poll	This command is treated by EP as a No-Op.
X'1E'	Adprep Address prepare	The host prepares the 3745 for polling by a BSC terminal on the addressed line. This command is valid only if the CSP controlling the line is in emulation mode.
X'1F'	Sad three Set addr3	This command is treated by EP as a No-Op.
X'23'	SETMODE	The host specifies the operating mode of the 2701 or 2703 being emulated by EP.
X'27'	Enable	The host requests that the addressed EP line be enabled. No data transfer occurs.
X'29'	Dial	Dial digits are transferred from the host to the dial equipment.
X'2F'	Disable	The host requests that the addressed EP line be disabled. No data transfer occurs.
X'41'	Write break	Execution is similar to X'01' except that no data is sent to the addressed EP line. The command ends when carrier from the line drops, or when a time out occurs.
X'58'	Read clear	Execution is identical to X'02' except that no decoding of control characters is performed.

EP Sense Information

Same as NCP sense information page 13-57, except bits 6 and 7:

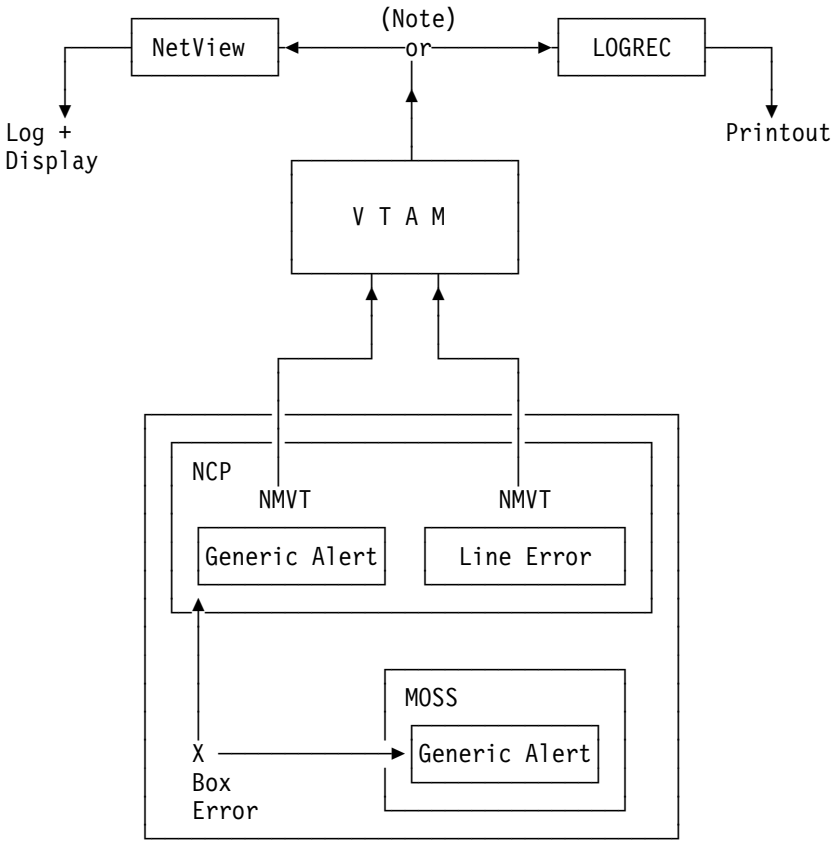
- Bit 6 : Lost data
- Bit 7 : Time out

Status Bytes Contents

Status Bit	Status Byte 0	Status Byte 1
x	Attention	Program controlled interrupt
. x	Status modifier	Incorrect length
. . x	Control unit end	Channel program check
. . . x	Busy	Protection check
. . . . x . . .	Channel end	Channel data check
. . . . . x . .	Device end	Channel control check
. . . . . . x .	Unit check	Interface control check
. . . . x	Unit exception	Chaining check

LOGREC Display With EREP

The environmental recording, editing, and printing program (EREP) edits and prints statistical error records that have been stored in the LOGREC file of the recorder file (SYSREC) by the recovery management support recorder (RMSR).



Note: If NetView is not available, VTAM sends the NMVTs to the LOGREC.

For information on how and when to run EREP, refer to "VS Environmental Recording, Editing, and Printing (EREP) Program".

Dumps and File Transfer to the Host

The list of the 3745 files which can be dumped is given in the following table.

File Transfer

The 3745 files that can be transferred are:

- MOSS dump
- NCP dumps (1) (3)
- CA dump (1) (3)
- Scanner dumps (TSS, HPTSS, and ESS) (1)
- TIC dumps (2)
- Configuration data file (CDF)
- Port swap file
- Vital product data (VPD)
- BER file.

(1) There are two dumps, one for each CCU (CCU-A and CCU-B).

(2) There are eight TIC dumps.

(3) These dumps are not automatically erased after a file transfer to the host and they are still accessible via RETAIN. All other dumps are automatically erased after the file transfer. (The validity of the dumps stored on the hard-disk is explained in the next paragraph.)

To print the 3745 files listed above, you must transfer them to the host. (Refer to *Service Functions* manual, SY33-2055, to display dumps from the MOSS console.)

The TIC dump file (CHGTRSS) holds up to eight TIC dumps. It is deleted automatically after the transfer to the host.

Once a dump is taken to the disk buffer area, it may be transferred to the host for printing.

There is no MOSS transfer function for the NCP residing in CCU storage.

MOSS, Scanner (TSS, HPTSS, ESS) and NCP Dump Validity

The MOSS, scanner (TSS, HPTSS, ESS) and NCP dumps are kept on the hard disk on the following conditions:

MOSS Dump

As soon as an automatic MOSS dump is taken, a threshold counter is set to 4 and the MOSS dump flag is set ON. If a MOSS dump already exists on the hard disk (MOSS dump flag set ON), a new automatic MOSS dump will be allowed after a 4-day delay (threshold=0).

The threshold check is made at two different times:

At MOSS IML time: The MOSS IML checks the dump date against the current date. The difference is used as threshold counter.

- If the difference is zero, the threshold counter is set to 4.

- If the difference is greater than 4, the MOSS dump flag is reset and the threshold counter is set to 4: this will allow an automatic MOSS dump.

When the MOSS runs: Each day the threshold counter is decremented. When it reaches zero, the MOSS dump flag is reset and a new automatic dump could be taken.

This process occurs with the following exeptions:

- The MOSS dump taken from the panel (ROS) has the highest priority and will always be taken.
- The MOSS dump transfer resets the MOSS dump flag which allows a new automatic MOSS dump.

Scanner Dump (TSS, HPTSS, or ESS)

If a scanner dump (TSS, HPTSS, or ESS) already exists on the hard disk, a new automatic scanner dump will be allowed after a 4-day delay threshold. Whenever an automatic scanner dump is requested by the NCP. The MOSS checks the scanner dump date against the current date. If the date is older than 4 days, the new scanner dump request will be processed and a new automatic scanner dump will be taken.

This process occurs with the following exeptions:

- A scanner dump during a re-IPL has the highest priority and will always be taken.
- The manual scanner dump under TSS services is protected by operator messages. The operator is given the choice to override a previous scanner dump.
- Scanner dump transfer allows a new automatic scanner dump.

NCP Dump

A new automatic NCP dump during IPL phase 1B will be allowed after a 7-day delay threshold. The dump date from DII (CHGCTLI) is checked against the current date.

This process occurs with the following exeptions:

- The purge of the NCP dump (VTAM command) allows a new NCP dump to be taken.
- The purge from DII allows a new NCP dump to be taken.

Transferring Dump Files to the Host

Functions in the host are used to transfer the dump files from the controller disk into the host and also to print them.

These host functions are described in the appropriate software publication.

When a dump is transferred to the host, it is automatically deleted from the disk dump area. The disk is then ready to receive another dump if necessary.

For the NCP dump, the delete function must be specifically requested.

Transferring Other 3745 Files to the Host

The file transfer and printing procedures are described in the appropriate software publication.

Vital Product Data (VPD)

The vital product data (VPD) information identifies the file printout on the host side and provides the control program with:

- Customer identification
- 3745 serial number
- Microcode EC level
- A record of the applied and restored microcode fixes (MCFs).

VPD Example

```
        "PRINT MOSS/CSP FILES" UTILITY

DATA WAS TRANSFERRED ON: mm/dd/yy AT: hh:mm:ss

THE FOLLOWING DATA WILL BE FORMATTED:
        ddddddddddddddddddddddddddddddd

CUSTOMER IDENTIFICATION: ccccccccccccccc

CONTROLLER TYPE: 3745   MODEL: n    SERIAL NUMBER: nnnnnnn

DISK EC: nnnnnn  EC MESSAGE: nnnnnn.......nnnnnnn (70 chars)

LAST APPLIED MCF: cccccccc
```

File Transfer to RETAIN

From a RETAIN terminal, it is possible to collect different 3745 dumps:

- Partial NCP dumps
- MOSS dumps
- TSS dumps
- HPTSS dumps
- ESS dumps
- TIC dumps
- CA dumps
- SIT trace
- BER file.

When transferring a MOSS dump; CDF, MLT, and VPD are automatically transferred.

It is also possible to transfer any MOSS screen via the remote log retrieval function (RLR).

Chapter 14. Ethernet Subsystem (ESS)

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ESS in 3745 Data Flow

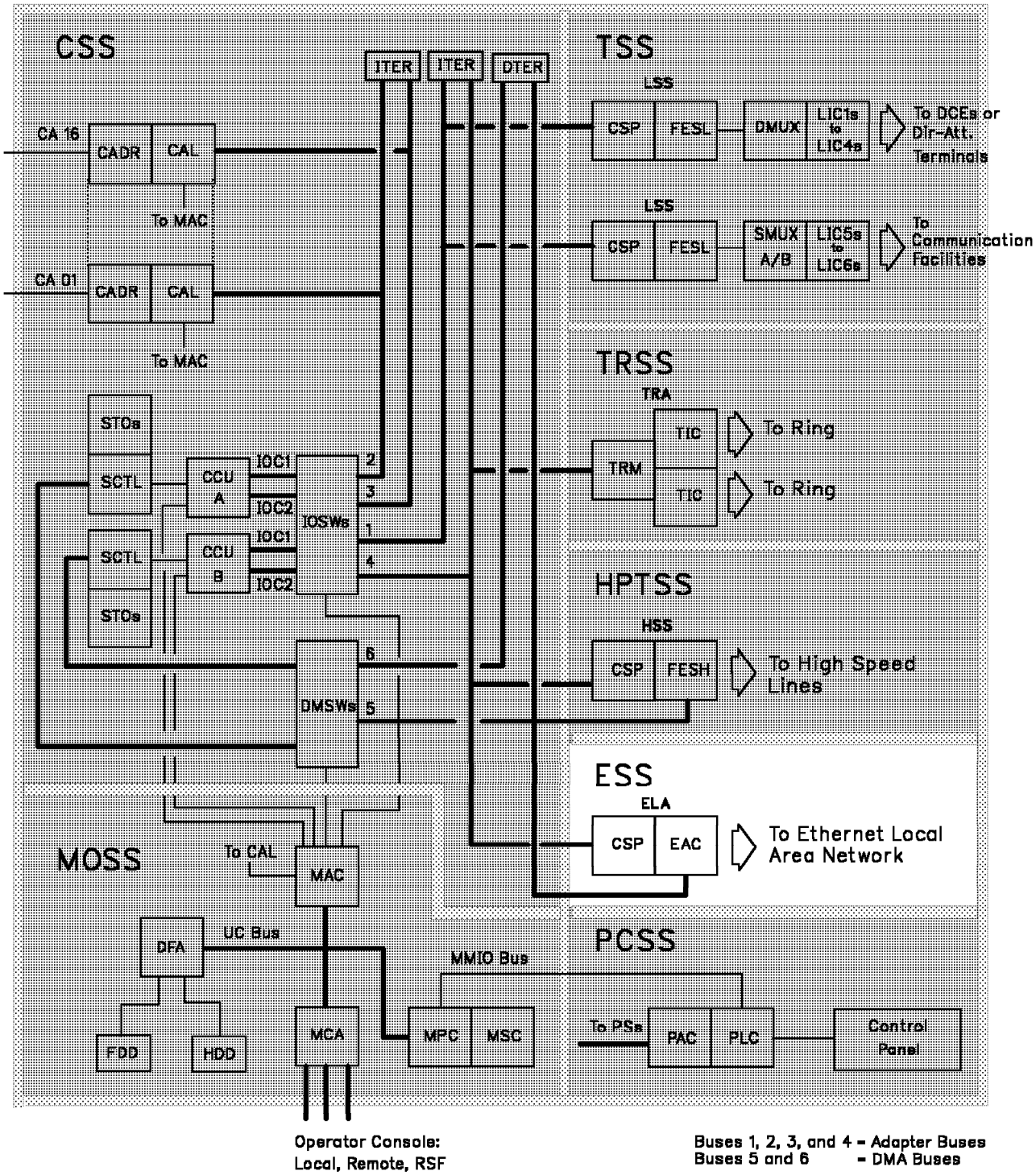


Figure 14-1. ESS in 3745 Data Flow. For models 21A-61A, DMA and IOC buses are connected to the CBC in the 3746-900. The MCA card is replaced by the MLA card which interfaces to the MPC card through the MMIO bus. This MLA card links the MOSS to the Service Processor through a LAN.

Introduction

The Ethernet LAN subsystem (ESS) attaches a maximum of 16 Ethernet-type local area networks (maximum of eight when token-ring adapters are installed). It consists of up to eight Ethernet LAN adapters (ELA). Each adapter can attach up to two Ethernet-type LANs, through a media adapter unit (MAU) operating at 10 million bits per second (Mbps).

The Ethernet LAN adapter (ELA) can be installed in all 3745 models, (configuration dependent) but it cannot be installed in the 3746 expansion units.

Ethernet subsystem provides attachment to a carrier sense multiple access, with collision detection (CSMA/CD).

System Environment

The ELA supports both Ethernet LAN Version 2 and IEEE 802.3 frames.

ELA Packaging

The handling and management of such a communication is achieved by an Ethernet LAN adapter (ELA) made of two cards:

- One communication scanner processor packaged on one card, the CSP card identical to those of the high-speed scanner (HSS) but with a different CSP microcode load module (see “ELA Microcode Description” on page 14-10).
- One Ethernet adapter card, the EAC card.

ELA is installed in HSS positions.

The ELA interface to the external equipment is a IEEE 802.3 15-pin D-type female AUI connector requiring a slide latch on mounting connector. The ESS uses the tail gate location of the corresponding HPTSS.

For board and card locations, see the Chapter 5 of the "Maintenance Information Procedures", SY33-2054.

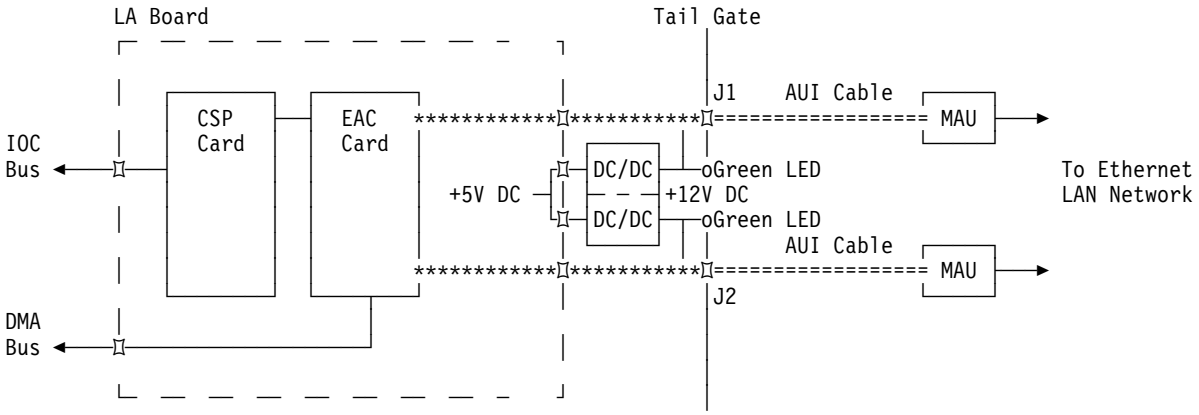
The tail gate contains also a DC/DC converter, one per port, which provides + 12V DC with up to 500 mA per port. The + 12V DC supplies an external transceiver called media access unit (MAU).

On the tail gate a green LED is On when the + 12 V DC is present on the corresponding J connector.

Use of MAUs

The performance of the Ethernet feature have been checked with a wide range of OEMs MAUs.***:*** Although meeting the 802.3 standards, some MAUs are more sensitive than others to electromagnetic environment and may degrade the box performance related to the noise margin.

The MAU must be equipped with the SQE-TEST (also called HEARTBEAT) function.



Up to eight ELAs (coupled CSP/EAC cards) may be installed on the line adapter board of the base frame, to control up to 16 data links at one time.

On each EAC two data links to be connected at the tail gate to that EAC. Both ports can be active at the same time.

Line Addressing

Each ELA supports a maximum of two line addresses.

With eight possible ELAs, the maximum number of lines is 16. Line numbers 1056 through 1071 are dedicated for ELA use.

The two lines associated with a particular ELA are addressed by the TD1 field of the IOH. TD1 bit 6 selects one of the two lines. TD1 bit 7 selects either the transmit or receive interface of the line. When TD1 bit 7 = 0 it selects the transmit interface and when TD1 bit 7 = 1 it selects the receive interface.

Refer to “ESS Line Addressing” on page 3-73 for the mapping of the lines between the boards and the tail gate.

ELA Commands

Commands are set in TD0 of the start line or start line initial instructions. The following NCP commands are supported by the ELA:

Commands	Codes (Hex)
Set mode	01
Enable	02
Disable	03
Change	06
Transmit Data	51
Receive Data	53
Trace	2C
Stop trace	2D
Halt	F0
Halt immediate	F1
Dump Control blocks (no status)	F4
Dump Control blocks (status)	F5
Suspend Receive	F8
Get Counters	50

For details on ELA commands, see “ELA Command Description” on page 14-32.

Interface or Port Types

Up to eight ELAs attaching up to 16 Ethernet LAN Version 2 or IEEE 802.3 networks operating at 10 Mbps.

ESS Data Flow

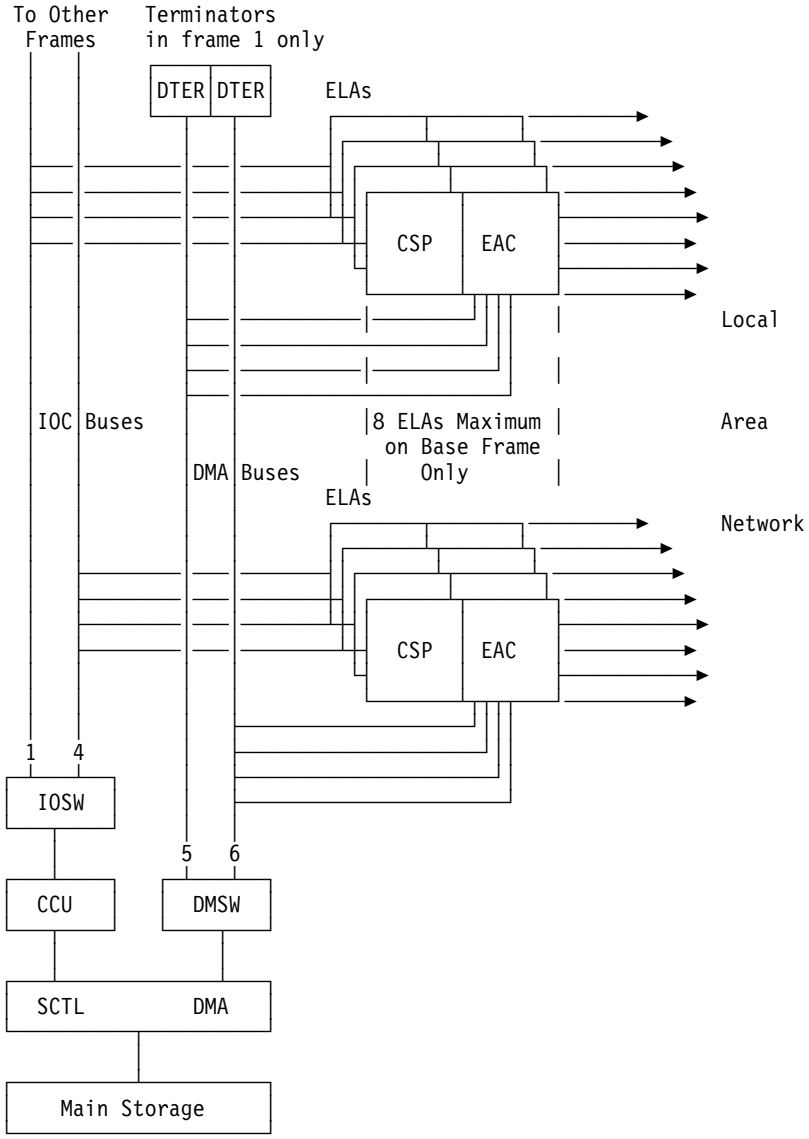


Figure 14-2. ESS Data Flow

Frame Types Supported

The ESS supports two types of frame:

- Ethernet Version 2 (Ethernet V2) frame
- IEEE 802.3 frame.

Internet Protocol (IP) and Address Resolution Protocol (ARP) are supported with both frame types.

Ethernet Version 2

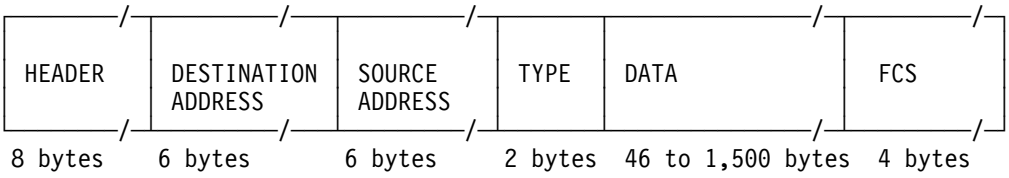


Table 14-1. Ethernet V2 Frame

Field Name	Bytes	Field Function
HEADER	0 - 7	Fixed bit sequence to identify the start of a frame.
DESTINATION ADDRESS	8 - D	Only 48 bit addresses are supported by Ethernet V2.
SOURCE ADDRESS	E - 13	Address of the source Ethernet adapter for the frame.
TYPE	14 - 15	To identify the higher level protocol that is embedded within the Ethernet V2 frame. The types supported by the 3745 Ethernet are: **X'800'** IP **X'806'** ARP
DATA		The size of this field can vary from a minimum of 46 bytes to a maximum of 1500 bytes. Since the requirement is that the Ethernet V2 data field be at least 46 bytes any use of PAD characters will have to be carried out by the NCP.
FCS		A 4 byte frame check sequence is included at the end of an Ethernet frame.

IEEE 802.3 Frame

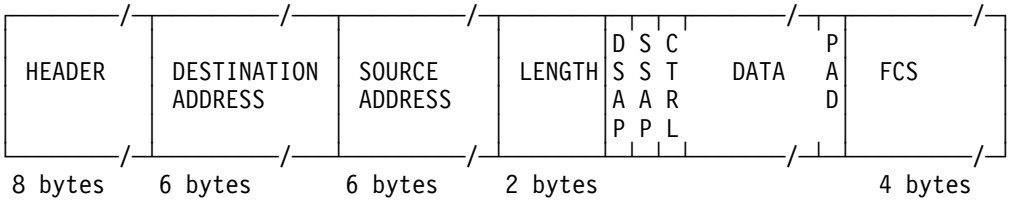


Table 14-2. IEEE 802.3 Frame

Field Name	Byte	Field Function
HEADER	0 - 7	Fixed bit sequence used for identifying the start of a frame. The last byte is the start frame delimiter.
DESTINATION ADDRESS	8 - D	Only 48 bit addresses are supported by the 3745 Ethernet.
SOURCE ADDRESS	E - 13	Address of the source Ethernet adapter for the frame.
LENGTH	14 - 15	Length from the next field to the end of the information. This value includes the DSAP, SSAP, CONTROL, and DATA fields. It does not include the PAD field.
DSAP	16	Destination Service Access Point. Bit 6 is the user defined address indicator. Bit 7 is the individual/group indicator.
SSAP	17	Source Service Access Point. Bit 6 is the user defined address indicator. Bit 7 is the command/response indicator.
CONTROL		May be a one byte or two byte field. For the type 1 frames used with connectionless protocols, the field will always be one byte. Only three types of frames are supported: Unnumbered information frame (x'03'), XID frame (x'BF'), and Test frame (X'F3').
DATA		Variable length field that contains the information portion of the frame. The length of the information must be within a range that allows the total size of the IEEE 802.3 frame data to less than the allowed maximum. For the 10 megabit 500 meter IEEE 802.3 standard, this value is the same as that for Ethernet V2 1500 bytes. Note however that the IEEE 802.2 header fields are counted as part of the data. So that the maximum size of a higher level protocol data unit that is embedded in an IEEE 802.3 frame will be less than the 1500 bytes allowed for an Ethernet V2 frame.
PAD		The size of an IEEE 802.3 frame must exceed a minimum value. For a 10 megabit 500 meter baseband implementation, this value is 64 bytes. The entire frame except for the PREAMBLE is included in this value. When the 18 byte length of the DA, SA, LENGTH, and FCS are subtracted, the 46 byte remainder is equivalent to the Ethernet V2 minimum packet size. If necessary the PAD field is included in an IEEE 802.3 frame to bring the frame up to the minimum size. The length of the PAD field is not included in the value in the LENGTH field.
FCS		A 4 byte frame check sequence is included at the end of an IEEE 802.3 frame.

ELA Microcode Description

ELA Microcode Functions

The ELA RAM Microcode provides:

- Interconnection between the control program and the EAC.
- Interconnection between MOSS and the EAC.
- Error handling.
- Loading the EAC Picocode.
- Problem determination items such as SIT, ESS services, EID.
- Handling of all of the SIT functions currently handled by the EAC picocode.
- Handling of early transmit status and error reporting to the control program to minimize the inter-packet gap.
- Handling a set of counters for certain Ethernet errors.

The ELA ROS Microcode provides:

- IPL of the ELA RAM Microcode
- Initialization of the ELA RAM Microcode
- Dump of the ELA RAM Control Storage (Microcode, control blocks,..).

ELA Microcode Structure

CSP Card

The CSP card provides:

- Interconnection to the IOC bus.
- Interconnection to the EAC card.
- JIB processor which includes:
  - The CSP ROS
  - Local Store registers
  - Control Storage (RAM)
  - Ping and Pong buffers
- External Registers (addressing for 32 registers).
- Address compare hardware.

Microcode Interrupt Levels

The CSP/JIB provides 8 interrupt levels for the microcode to use. Following are the functions positioned on these levels for the ELA:

- Level 0: Error processing, MOSS command processing
- Level 1:
  - NCP/MOSS commands (PIO IOH/IOHI, MIOH)
  - Cycle Steal (AIO)
- Level 2: EAC status
- Level 3:

  - Receive command processing
  - Cycle steal initiation

- Level 7: Background, transmit, set mode, enable, disable, F4/F5, SIT, timer control.

Microcode Control Blocks in CSP Control Storage

The following types of control blocks are used by the microcode:

- ICB (Interface Control Block)

  There are two ICBs for each line; one for each interface (transmit and receive). The ICBs contain items necessary for the microcode to perform the action in process. For example, the CSP and CCU addresses for cycle steal operation, operational flag bits, TA/TD of the command in progress, and so on.

- PSA (Parameter Status Area)

  There are two PSAs for each line; one for each interface (transmit and receive). The PSAs contain the parameters obtained from the CCU for the command in progress and the Status after the command is complete.

- LCB (Line Control Block)

  There is one LCB for each line. The LCB contains information about the line, such as the Set Mode data, Internal Box error status, line timers, and so on.

- Other control blocks include ones for MOSS and SIT commands, EAC control words, EAC data trace for SIT, ...

Internal Interconnections

As shown in “ESS Data Flow” on page 14-7, each ELA interconnects with the communication subsystem (CSS) and the MOSS via the IOC bus and the DMA bus.

CSP-to-IOC Bus

This connection is used for:

- Communication with the NCP (through the same IOH high level commands as the other HSS scanners)
- MOSS command exchange
- ELA IML
- Diagnostics.

The physical interconnection between the ELA CSP and the CCU is identical to that between the LSS CSP to the CCU (refer to Chapter 4, "Transmission Subsystem").

For board and card locations, see the Chapter 5 of the *Maintenance Information Procedures Manual*, SY33-2054.

NCP-ELA Microcode

The CCU uses IOH and IOHI to exchange data, commands and statuses with the ELA CSP in the same way as with the LSS, but cycle steal is not used when the EAC is running.

EAC to CSP

The physical interconnection between the EAC and the CSP is identical to that between the FESH and the CSP of the HSS.

For board and card locations, see the Chapter 5 of the *Maintenance Information Procedures Manual*, SY33-2054.

Microcode to EAC

The picocode is loaded from the CSP in each layer of the EAC RAM at IML time.

The EAC-to-CSP interconnection is activated and controlled via external registers and control words (CW).

A CW is built by the CSP microcode and specifies the actions to be performed by the EAC.

The CW is cycle stolen by EAC, then executed.
The EAC informs the CSP microcode when the action is completed.

EAC to DMA Bus

This connection is used for direct CCU storage access and specifically:

- NCP buffer prefix exchange
- Data transfer between the Ethernet LAN and main storage

The physical interconnection between the EAC and the DMSW is identical to that between the FESH and the DMSW of the HSS.

Communication Scanner Processor (CSP)

The ELA CSP hardware is identical to that of the LSS CSP (refer to Chapter 4, "Transmission Subsystem" for details).

Ethernet LAN Coupler Card (EAC)

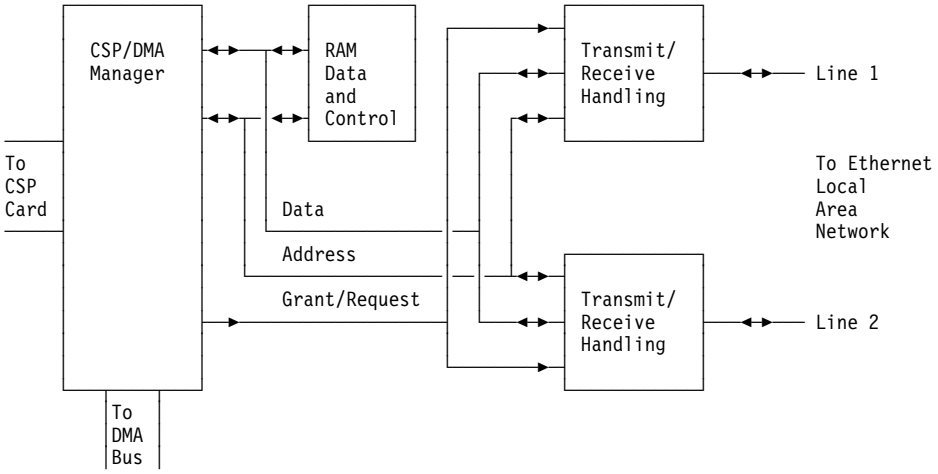


Figure 14-3. EAC Data Flow

The transmit/receive handling of the EAC is functionally organized in layers:

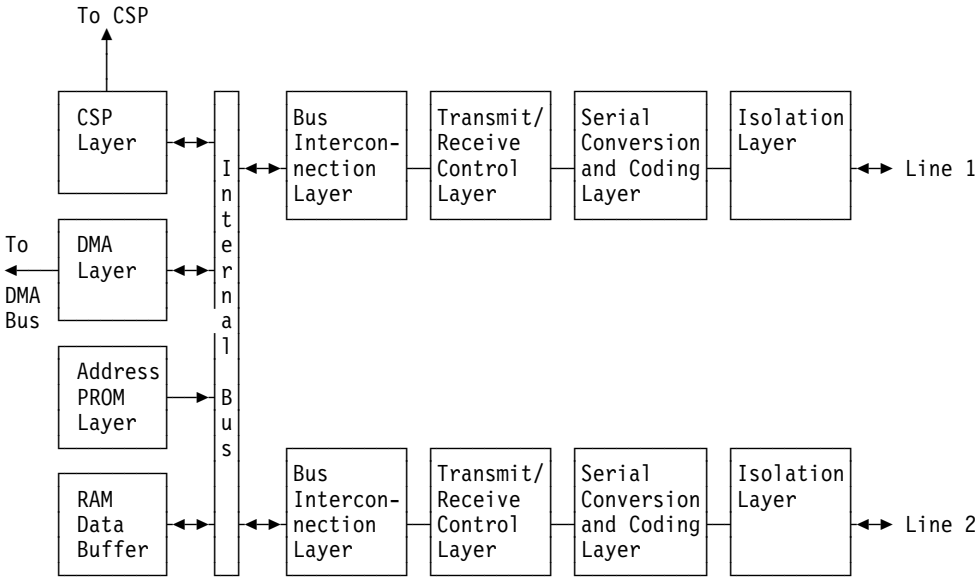


Figure 14-4. EAC Layers

CSP Layer

The CSP layer:

- Interconnects on one side with the CSP storage and microcode.
- Interconnects on the other side with the various EAC layers via CSP external registers and cycle steal operations.
- Handles the protocols of CSP external registers and cycle steal operations.
- Handles cycle steal requests from the CSP layer.

DMA Manager Layer

The DMA manager layer:

- Interconnects on one side with:
  - EAC RAM
  - Data buffers
- Interconnects on the other side with the DMA bus.
- Handles the DMA bus protocol.
- Performs data transfer from/to CCU main storage, to/from transmit/receive/data buffers.

Address PROM Layer

The address PROM contains:

- The 48 bit Universal Ethernet address for line 1.
- The 48 bit Universal Ethernet address for line 2.
- The one's complement of each of the above addresses.
- The addresses are read by the picocode and placed in the RAM where they are accessed by the CSP microcode.

Bus Interconnection Layer

The bus interconnection layer:

- Provides communication between the CSP layer and the transmit/receive control layer.
- Provides communication between the RAM and the transmit/receive control layer.
- Communicates with the bus arbitrator.

Transmit/Receive Control Layer

The transmit/receive control layer:

- Obtains data from the RAM and transfers it to the serial conversion for transmission to the line.
- Filters out frames that the control program does not support. If IP Dynamics is supported, this filtering process is made more flexible by using an Ethernet Type table provided by the control program by the Set Mode command.
- Receives data from the serial conversion layer and transfers it to the RAM.
- Provides status to the CSP layer after each transmit/receive operation.
- Generates CRC.
- Checks CRC.
- Checks network addresses.
- Synchronizes adapter with network.
- Checks receive frame lengths.

Serial Conversion and Coding Layer

The serial conversion and coding layer:

- Converts from parallel to serial data on transmit.
- Converts from serial to parallel data on receive.
- Converts to/from binary from/to differential Manchester code.

Isolation Layer

The isolation layer:

- Provides electrical isolation from the transceivers.

Reset EAC

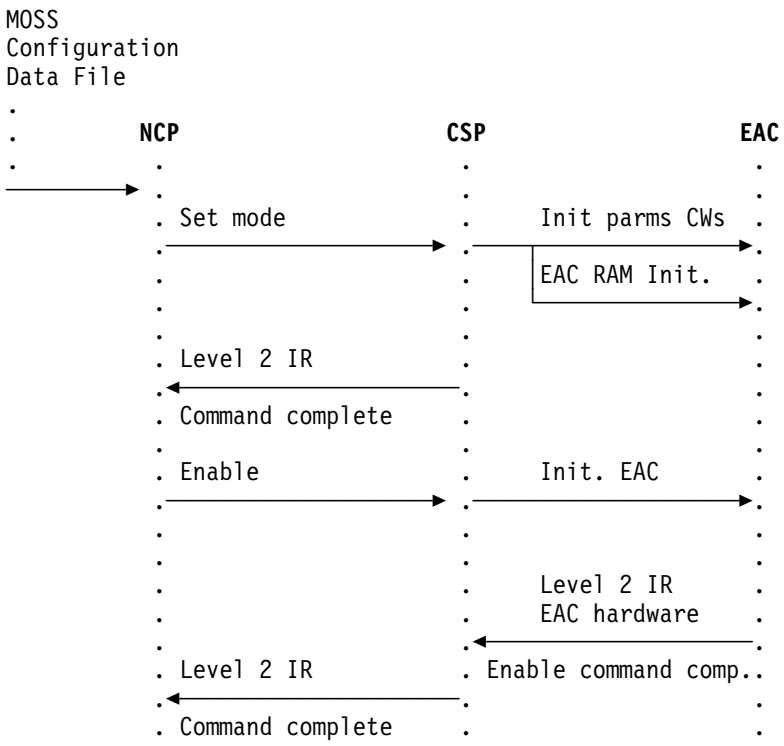
All latches are reset, the DMA is disabled, the card is kept in 'freeze mode' (EAC not operational) until the CSP loads the microcode.

NCP-to-CSP Command Flow

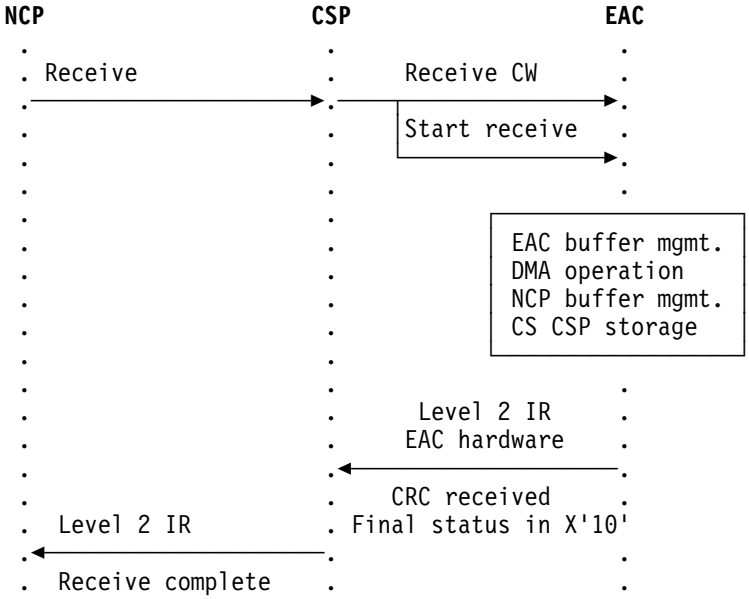
The following shows the general command flow between the NCP and the ELA (CSP + EAC). These diagrams are the main line paths of command execution in the ELA. Exception and error conditions are not covered.

The supported NCP commands are listed in “ELA Commands” on page 14-6.

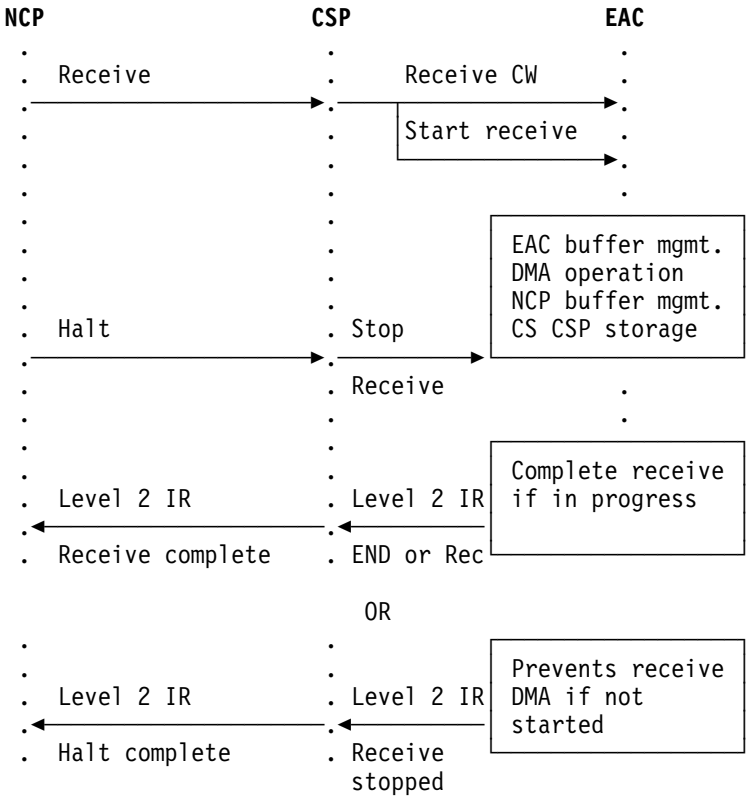
Set Mode/Enable Commands



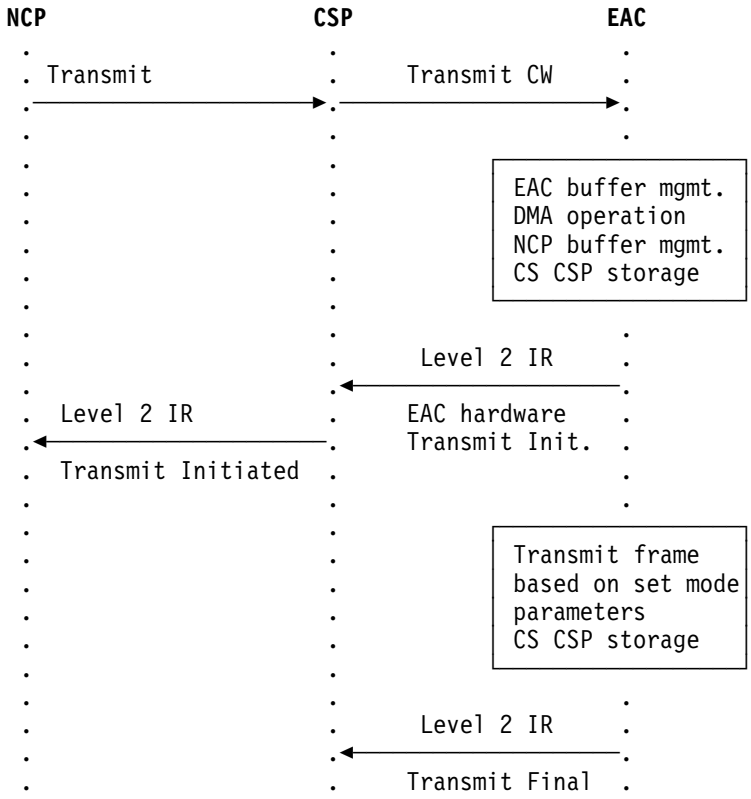
Receive Command



Halt Command



Transmit Command



Microcode Interaction With Control Program

This section describes the software interconnection between the network control program (NCP), which resides in the 3745 central control unit (CCU) and the ELA microcode residing in the communication scanner processor (CSP).

NCP-to-CSP Interconnection Description

The program interconnection provides a control path between the NCP and the CSP. The interconnection uses only programmed output instructions and programmed input (PIO) instructions during normal operation.

The interconnection is composed of the following functional components:

1. The NCP parameter/status area (PSA) to store the CSP control and status information.
2. Two programmed output instructions: set line vector table high and set line vector table low to tell the scanner the location of the line vector table (LNVT) in CCU storage.
3. Two programmed output instructions: set special line vector table high and set special line vector table low to tell the scanner the location of the trace line vector table (TLNVT) in CCU storage.
4. A programmed output instruction: start line initial to set or modify the parameter/status area address, and to initiate a command sequence.
5. A programmed output instruction: start line to initiate command sequences without modifying the parameter-status area address.
6. A programmed input instruction: fast get line ID to initiate auto-selection of a CSP and to get line identification data when servicing CSP interrupts.
7. A programmed input instruction: get error status to get information about a CSP program or hardware check.
8. A programmed input instruction: get command reject status to get additional information about a command reject status.
9. A programmed input instruction: get microcode check to get additional information about microcode-detected errors.

NCP and CSP Control Block Relationship

The following shows the relationship among the NCP and CSP control blocks:

- The NCP parameter/status areas are accessed by the CSP through the LNVT segment corresponding to that CSP.
- Identification of the NCP interface blocks are communicated to the CSP through the set mode command.
- The data to transmit is taken by the EAC using DMA from the transmit buffer chain and sent on the line.
- Received data is stored in the EAC receive queue and transferred through DMA to the receive buffer chain.

Parameter/Status Area

The control program residing in the CCU (NCP) provides a fixed-length field of CCU storage for each line interface serviced by high-level commands.

The parameter/status area is a field reserved in CCU storage by the NCP.

It is used to transfer the control and status information between the control program in the CCU and the CSP.

Information is transferred using cycle steal under control of the CSP.

The parameter/status area is made up of:

1. A parameter area (16 bytes long)
2. A status area (12 bytes long).

The parameter area is used to pass to the CSP, parameters required in the execution of a command.

The status area is used to pass ending status to the control program in the CCU.

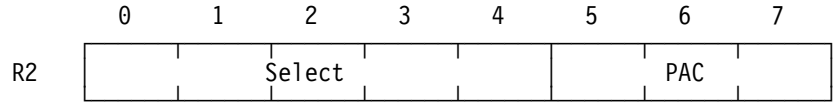
Upon receipt of a start line or start line initial instruction, the CSP gets information from the parameter area, executes the command, puts ending status into the status area, and requests a CCU level 2 interrupt.

Refer to “Parameter/Status Area Layout” on page 14-25 for field description.

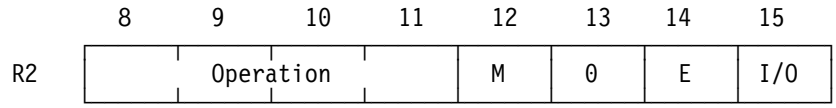
Input/Output Instruction Formats

The CCU communicates with the CSP via input/output halfword (IOH) or input/output halfword immediate (IOHI) instructions sent on the IOC bus at TA time.

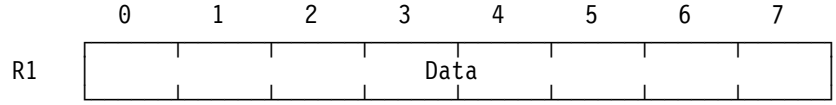
TA Field Byte 0



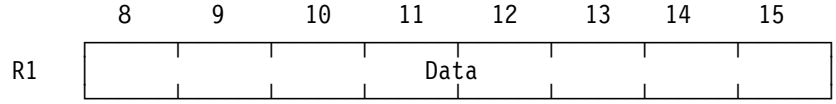
TA Field Byte 1



TD Field Byte 0



TD Field Byte 1



I is the 16-bit immediate data field of the IOHI instruction.

TD fields:

The contents of these two bytes depend on the instruction (as indicated in the operation field of TA1). For example, if the operation is start line or start line initial, TD byte 0 is the command to be performed by the scanner, and TD1 contains the line interface address. Refer to the description of each operation for a definition of the TD fields.

IOH/IOHI Instruction Summary

IOH/IOHI Byte 1[1]	Instruction
00	Start line
01	Fast Get line ID
10	Start line initial
11	Get error status
20	Set line vector table high
21	Get command reject status
30	Set line vector table low
31	Get microcode check
50	Set special line vector table high
60	Set special line vector table low
F2	Automatic dump

[1] IOH: byte 1
IOHI: byte 1 of second halfword

Start Line
The start line (TA byte 1=X'00') is issued to the CSP when a new command is to be started and the location of the parameter/status area has already been established.

Get Line ID
The get line ID (TA byte 1=X'01') is issued to all CSPs (select bits 2 and 3 are ON to indicate a 'broadcast address') when servicing a CCU level 2 interrupt.

Start Line Initial
The start line initial (TA byte 1=X'10') is issued to the CSP when a line operation is to be started and it is necessary to establish the location of the parameter/status area.

Get Error Status
The get error status (TA byte 1=X'11') is issued to the CSP in response to a CCU level 1 interrupt request. This interrupt indicates a CSP program or hardware error.

Set Line Vector Table High
Set line vector table high (TA byte 1=X'20') indicates to the CSP its entry into the line vector table (LNVT) in CCU storage. More specifically, the NCP passes the high byte LNVT address for the first interface supported by a given CSP.

Get Command Reject Status
Get command reject status (TA byte 1=X'21') is issued to the CSP after the CCU has received a command reject error status to gather more information about the command reject.

The CSP responds with a two-byte status which identifies the command in process followed by the command that overlapped it. There is no default value for TD.

Set Line Vector Table Low
Set line vector table low (TA byte 1=X'30') indicates to the CSP its entry into the line vector table (LNVT) in CCU storage. More specifically, the NCP passes the low halfword LNVT address for the first interface supported by a given CSP.

Get Microcode Check
Get Microcode Check (TA byte 1=X'31') is issued to the CSP after the CCU has received a type 3 error status with bit 4 set (microcode check) to get information about the microcode check.

The CSP responds with a two-byte field containing the identification of the checker in the second byte. The following is a list of the ELA microcode checks that can be returned:

Status	Meaning
0001	Double queuing of an ICB pointer
0003	Fast get line ID not active
0008	Branch to X'8000'
000A	Branch to X'A000'
000B	Branch to X'B000'
000C	Branch to X'C000'

Set Special Line Vector Table High

Set special line vector table high byte (TA byte 1=X'50') is used to modify the location of the special line vector table (SLNVT).

Set Special Line Vector Table Low

Set special line vector table low halfword (TA byte 1=X'60') is used to modify the location of the special line vector table (SLNVT).

Automatic Dump

Automatic dump (TA byte 1=X'F2') is used to cause a scanner dump.
As a result of this instruction, the ELA sets a CCU level 1 interrupt and returns a status that causes NCP to request a scanner dump from MOSS.

IOH/IOHI Instruction (from MOSS) Summary

IOH/IOHI Byte 1[2]	Instruction
08	Start MOSS
09	Get command completion
18	Run JIB checkout
19	Get error status
28	Set MOSS area high
29	Get JIB checkout results
38	Set MOSS area low
39	Get scanner status
48	Reset

CSP Addressing

The CSPs associated with the possible eight ELAs installed in a 3745 are assigned the addresses of the first eight line adapters (LA) on the LA board 1 (TSSB board).

These addresses are used in the input and output instructions to select individual ELA adapters. In addition, all CSPs respond to a general broadcast address which is used in the get line ID instruction during auto-selection.

[2] IOH: byte 1
IOHI: byte 1 of second halfword

Parameter/Status Area Layout

The configuration of the parameter/status area differs from command to command. However, the fields which appear in multiple commands are always found in the same PSA location.

A layout of an ELA PSA follows.

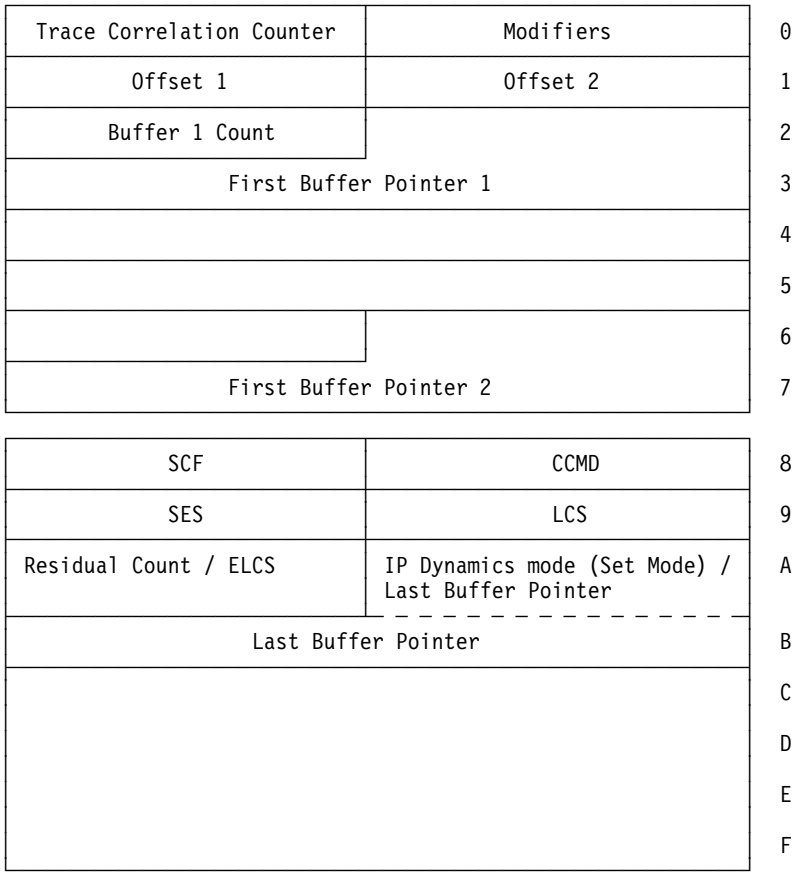


Figure 14-5. General ELA PSA Layout

Status Control Field (SCF)

This byte contains information which describes the progress of the operation being executed.

Bit **0 1 2 3 4 5 6 7**	**Meaning**
x	Halt
. x	Service request
. . x	Unused
. . . x	Hardware error LCAR
. . . . x . . .	Data stored
. . . . . x . .	End of message (EOM)
. . . . . . x .	Data transmitted occurred
. . . . x	Counters overflowed

Current Command (CCMD)

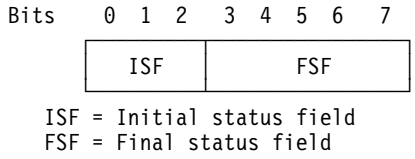
This byte identifies the CSP command to which this status applies.

Secondary Status (SES)

Unused

Line Communication Status (LCS)

This byte contains status applicable to the line being serviced. The byte is divided into two fields as shown below:



Initial Status Field (ISF) Bit Definition

The ISF (LCS bits 0 - 1) indicates essentially the type of line control that is used. The ISF is decoded as follow:

ISF / FSF 0 1 2 3 4 5 6 7	Meaning
1 0 0	Special status
1 1 0	Internal box error
1 1 1	Hardware error

Special Status: See paragraph “Initial Status = B'100' (Special)” on page 14-27 for more explanation.

Internal box error: See paragraph “Initial Status = B'110' (Internal Box Error)” on page 14-27 for more explanation.

Hardware error: See paragraph “Initial Status = B'111' (Hardware Error)” on page 14-30 for more explanation.

Final Status Field (FSF)

The FSF (LCS bits 3 - 7) gives further status information. The encoding is based upon the ISF configuration and is defined as follows:

Initial Status = B'100' (Special)

ISF	FSF	
0 1 2	**3 4 5 6 7**	**Meaning**
1 0 0	0 0 0 0 x	Time out (nothing received)
1 0 0	1 1 1 0 x	Disconnected
1 0 0	1 1 1 1 x	Connected

Initial Status = B'110' (Internal Box Error)

ISF	FSF	
0 1 2	**3 4 5 6 7**	**Meaning**
1 1 0	0 0 0 0 0	AIO error
1 1 0	0 0 1 0 0	CSP interconnection error
1 1 0	0 0 1 1 0	EAC failed to answer
1 1 0	0 1 0 0 0	EAC internal error
1 1 0	0 1 0 0 1	Transmitter timeout error
1 1 0	0 1 0 1 0	Storage error
1 1 0	0 1 0 1 1	Transmit overrun
1 1 0	0 1 1 1 0	Receive buffer error
1 1 0	1 0 0 0 0	No interrupt from EAC
1 1 0	1 0 0 1 0	Command rejected (See Note 1)
1 1 0	1 0 1 0 0	Trace already active
1 1 0	1 0 1 1 0	Transmit buffer error
1 1 0	1 1 0 0 0	Invalid level 2 interrupt
1 1 0	1 1 0 1 0	Underflow
1 1 0	1 1 1 0 0	SCTL/DMA/DMSW error (See Note 2)
1 1 0	1 1 1 1 0	Overflow
1 1 0	1 1 1 1 1	Collision

Notes:

1. An extended LCS code (ELCS) is generated. Refer to “Extended Line Communication Status (ELCS) For LCS X'D2'” on page 14-28 for details.
2. An extended LCS code (ELCS) is generated. Refer to “Extended Line Communication Status (ELCS) For LCS X'DC'” on page 14-29 for details.

Initial Status = B'110' (Internal Box Error): The code is the value of the LCS bits 0 to 7 (fields ISF, FSF).

Code	Description
C0	AIO error indicates a hardware error during an adapter-initiated operation (cycle-steal).
C4	CSP/EAC interconnection hardware error.
C6	No answer to a microprogram initiated operation to the EAC.
C8	EAC hardware error detected by the EAC.
C9	Transmitter timeout error. It indicates that the transmitter has been active longer than the time to send the maximum length packet. It occurs when 1519 bytes have been transmitted. The entire packet will continue to be transmitted unless a failure occurs.
CA	Internal storage access in the EAC did not receive a ready signal from the EAC hardware when trying to access memory.
CB	This indicates that neither of the two internal EAC transmit buffers is free to be used by DMA for the transmit command issued.
CE	The EAC hardware receive buffers are defined large enough to hold the maximum expected receive frame of 1518 bytes. If a receive frame is received greater than 1518 bytes, the EAC picocode will detect this and report this condition to the microcode which will result in a counter increment.
D0	The EAC has failed to respond to a microcode request.
D2	The command issued by the control program has been rejected by the CSP. An extended LCS code (ELCS) is generated. Refer to “Extended Line Communication Status (ELCS) For LCS X'D2'” for details.
D4	A scanner internal trace is already running on this interface.
D6	EAC does not find an end of packet flag in the current internal EAC buffer and does not own the next buffer.
D8	An unexpected CSP level 2 interrupt from the EAC has occurred.
DA	Indicates that the EAC transmitter has truncated a message due to data late from the EAC internal memory.
DC	SCTL/DAM/DMSW type error. An extended LCS code (ELCS) is generated. Refer to “Extended Line Communication Status (ELCS) For LCS X'DC'” on page 14-29 for details.
DE	EAC receiver lost part or all of a packet because it could not store it into an EAC buffer before the front end internal silo overflowed.
DF	Collision error indicates that the collision input to the EAC failed to activate within 2 microseconds after a EAC-initiated transmission was completed.

Extended Line Communication Status (ELCS) For LCS X'D2': When the LCS = X'D2', additional statuses for command reject may be found in byte 4 of the status area. These additional statuses are:

Code	Description
01	Line not enabled, common command
02	SIT buffer not available
03	Receive command received but line not enabled
04	Receive command received not using NCP type buffers
05	Invalid command received on receive interface
06	Transmit command received but line not enabled
07	Transmit command received not using NCP type buffers
08	Invalid command received on transmit interface

09 Transmit type command to receive ICB
0A Halt received with no command in progress and line disabled
0B Set Mode addressed to a line other than the first 2 in this ESS
0C Transmit frame longer than 1514 bytes
0D NCP receive buffer shorter than 1518 bytes.
0E F5 issued when no command is in progress.

Extended Line Communication Status (ELCS) For LCS X'DC': When the LCS = X'DC', additional statuses, as with internal box errors, may be found in byte 4 of the status area. These additional statuses are:

Code	Description
02 (a)	SCTL/DMA internal error
04 (e)	SCTL/DMA interconnection error
06	Combination of (f) and (g)
08 (3)	DMA time out on write
0A (1)	DMA interconnection error in write
10 (c)	SCTL/DMA storage protect/address exception
12 (b)	SCTL/DMA logical error
14 (f)	DMSW main bus parity check
16	Combination of (f) and (h)
18 (4)	DMA time out on read
1A (2)	DMA interconnection error on read
22 (d)	Storage unrecoverable error/SCTL internal error
24	Combination of (e) and (f)
28 (g)	DMSW parity check on primary/secondary bus
2A (5)	DMA bus driver fault
34	Combination of (e), (f) and (g)
3A (6)	DMA burst count error
44	Combination of (2), (e), (f) and (g)
4A (h)	DMSW driver fault
5A	Combination of (1), (e), (f), and (g)
6A	Combination of (2) and (g)
7A	Combination of (2) and (h)
9A	Combination of (5), (e), (f) and (g)
AA	Combination of (6) with any of (a) through (h)
BA	Combination of (1) through (6) with any of (a) through (h) which are not listed above.

Initial Status = B'111' (Hardware Error):

ISF	FSF	
0 1 2	3 4 5 6 7	Meaning
1 1 1	1 0 0 1 0	Connection not established
1 1 1	1 0 1 0 0	Loss of carrier

Initial Status = B'111' (Hardware Error): The code is the value of the LCS bits 0 to 7 (fields ISF, FSF).

Code Description

F2 During the Enable command process, the ESS will perform an external loopback to determine if a connection to the LAN is made. Any internal box errors will be reported as normal. But, all other errors that occur during the loopback will result in this F2 LCS. These include excessive retries on transmit, late collisions, CRC errors, framing errors, and missed packets.

F4 This is set when the carrier input to the EAC goes false during a transmission. This is a transmit error. No retries have been done on the packet.

Note: In all cases of Internal Box Errors and Hardware Errors:

- The line is disabled by the CSP.
- The command on the failed interface is ended. LCS contains the error and a level 2 interrupt request is raised to the CCU.
- The command on the other interface is cleared without any ending status nor level 2 interrupt request to the CCU.

After such an error the only commands that will be accepted on the line are set mode or enable.

Residual Count

This byte indicates the number of unused bytes remaining in the last buffer used.

Last Buffer Pointer

This three-byte address points to the last buffer used during receive operations.

Data Management

The exchange of information between the NCP and the ELA microcode (Parameters, statuses, and so on) is done through cycle steal.

In receive or transmit, the parameters are used by the microcode to build the control word (CW). The CW allows the EAC hardware to start handling the frame exchange in receive or transmit.

The microcode builds the status to be sent to the NCP:

- After the completion of a transmit or receive command,
- At the end of the NCP buffer chain detected by the EAC, and before the reception of a complete frame to request a buffer for the EAC,
- At buffer request from the EAC,

– When an error is detected in the EAC adapter.

The microcode issues one single request to the EAC to manage the receive line interface and the transmit line interface.

ELA Command Description

Once a command is received by the CSP it becomes 'outstanding'. It stays outstanding until the CSP sets a CCU level 2 interrupt to terminate the command.

The following commands do not create an 'outstanding command' condition:

- Halt
- Halt immediate
- Dump control blocks (no status)
- Dump control blocks (status)

These four commands are accepted even when there is an outstanding command and are used to terminate the outstanding command.

If a new command is received when there is an outstanding command, the new command is rejected (a CCU Level 1 interrupt request is set).

Set Mode

The Set Mode command is used to select and personalize the line. It is also used to either get a locally administered address from the control program and provide it to the ESS, or transfer the adapter Ethernet address (universally administered address) from the ESS.

The NCP IP address for the line is provided by Set Mode command. If the control program is supporting IP Dynamics, the Set Mode provides an Ethernet Type table to be used in filtering of frames being received.

Set Mode must be the first command issued to a line. If another command is received before the Set Mode, it is rejected and a CCU level 1 interrupt request is raised. One exception to this rule exists: a Halt Immediate, issued before the Set Mode (for example when there is no outstanding command) will be accepted. It will, however, be ignored as there is no outstanding command.

Set Mode data includes:

1. NCP buffer information
2. Counter overflow limits
3. Split First Buffer specification
4. Type of address used.
5. Locally Administered Address
6. NCP IP address

A Set Mode command may only be issued to the even interface of a line. It will be rejected if issued to the odd interface. The Set Mode command may be issued at any time as long as there is no other command outstanding.

CSP Processing

1. Get the parameters from the CCU.
2. Save the line (interface) IDs, which are part of the parameters.
3. If ESS and NCP support IP Dynamics, get Ethernet Type table and provide it to the EAC picocode. Also, set the ESS in IP Dynamics mode so the table will be used for filtering incoming frames.
4. Get the set mode data from the CCU.

5. Initialize the CSP control blocks and the EAC with the set mode parameters from NCP.
6. Transfer the proper Ethernet address.
7. Build the command ending status and transfer it to the CCU.
8. Set a CCU level 2 interrupt.

Typical Ending Statuses:

SCF	SES	LCS	Meaning
44	00	00	Set mode complete
00	00	D2	Command rejected
C4	00	00	Halt executed
00	00	See[1]	Internal box error

[1] = Refer to “Line Communication Status (LCS)” on page 14-26 for details.

Enable

The Enable Command is used to prepare the line for data transfer.

The EAC picocode will initialize the hardware so that it can accept a transmit or receive command.

The Enable must be issued to the even interface only. It will be rejected if issued to the odd interface. In addition the Enable must be executed before any data transfer commands are sent to the CSP.

Internal box errors that occur after completion of the Enable command, are stacked in the CSP and will be passed to NCP in the ending status of the next command.

The ESS microcode will run a 10 second timer waiting for the EAC to finish its Enable process. If the timer expires, an LCS of D0 will be returned as an internal box error because this is a picocode/hardware function only.

CSP Processing

1. Start an Enable timer.
2. Initialize the ECA initialization block for external loopback.
3. Initialize control blocks in EAC external RAM and then issue a DISABLE, INIT and START commands to the EAC to allow for an external loopback.
4. Perform the external loopback.
5. Check result of loopback. In case of errors, repeat the loopback up to 32 times.
6. Initialize the ECA initialization block for normal opereation.
7. Initialize control blocks in EAC external RAM and then issue a DISABLE and INIT commands to the EAC.
8. Clear the ESS error and status counters.
9. Clear any counter overflow indications.
10. The ending status is built and transferred to the CCU.
11. A CCU level 2 interrupt request is set.

Typical Ending Statuses:

SCF	SES	LCS	Meaning
44	00	9E	Enable complete
C4	00	00	Halt executed
00	00	F2	Connection not established
00	00	D2	Command rejected
00	00	See[1]	Internal box error

[1] = Refer to “Line Communication Status (LCS)” on page 14-26 for details.

Disable

The Disable command is used to stop the EAC and prevent it from receiving any more packets or being able to transmit any packets. The line is placed in the disabled state and an Enable command must be issued before the line can transfer data again.

A Disable may be issued to the even interface only. It will be rejected if issued to the odd interface.

The ESS microcode will run a 10 second-timer, waiting for the EAC to finish its Disable process.

CSP Processing

1. Start the disable timer.
2. Issue a Disable command to the EAC and wait for an EAC interrupt.
3. The ending status is built and transferred to the CCU.

Typical Ending Statuses

SCF	SES	LCS	Meaning
44	00	9C	Disable complete
00	00	D2	Command rejected
00	00	See[1]	Internal box error

[1] = Refer to “Line Communication Status (LCS)” on page 14-26 for details.

Change

This command is used to update up to ten contiguous bytes of the Set Mode data.

The Change command is rejected if received on the odd interface or if it is sent to a line that has not received a Set Mode command.

CSP Processing

1. Get the parameters from the CCU.
2. Update the Set Mode data bytes as requested.
3. Initialize the CSP control blocks and EAC with the new data.
4. Build the ending status and transfer it to the CCU.
5. Set a CCU level 2 interrupt request.

Typical Ending Statuses

SCF	SES	LCS	Meaning
44	00	00	Change complete
00	00	D2	Command rejected
00	00	See[1]	Internal box error

[1] = Refer to “Line Communication Status (LCS)” on page 14-26 for details.

Transmit Data

The Transmit Data Command is used to transmit:

- Ethernet V2 frames
- IEEE 802.3 frames.

This command will be rejected if issued to the odd interface.

The entire frame must be contained in the first NCP buffer chain. When a buffer pointer of zero is detected in the buffer prefix area, the end of data for the frame has been reached.

CSP Processing

1. Get the parameters from the CCU.
2. Prepare a transmit control word for the EAC containing:
   - The buffer count from the PSA
   - The buffer offset from the PSA
   - The first transmit buffer address from the PSA.

   Note: The buffer prefix length is forced to x'08' by the ESS.

3. Issue a Start Transmit command to the EAC. The EAC will enter in a transmit mode and then start processing the transmit buffer provided in the control word.

   EAC buffer processing works as follows:
   - If the first transmit buffer address is not zero and the NCP buffer count is not zero, then all data in the chain of NCP buffers is transmitted, until an NCP buffer link pointer of zero is detected.
   - If the first transmit buffer address is not zero and the NCP buffer count is zero, then the first buffer is skipped. Data in all buffers chained to the first is transmitted, until an NCP buffer link pointer of zero is detected.
   - For buffers subsequent to the first, the offset and count are taken from the buffer prefix and a prefix length of x'08' is used.
4. Build the ending status and transfer it to the CCU.
5. Set a CCU level 2 interrupt request.

Typical Ending Statuses

SCF	SES	LCS	Meaning
46	00	00	Transmit started
00	00	D2	Command rejected
00	00	See[1]	Internal box error
10	00	F4	Ethernet error (LCAR)
C4	00	00	Halt executed

[1] = Refer to “Line Communication Status (LCS)” on page 14-26 for details.

Receive

The Receive Command is used to pass the address of the first buffer in a receive data buffer chain to the CSP and to place the CSP in receive mode.

CSP Processing

1. Get the parameters from the CCU.
2. Prepare a receive control word for the EAC containing:
   - The buffer count from the PSA
   - The buffer offset from the PSA
   - The first receive buffer address from the PSA.

   Note: A Buffer Prefix Length of x'08' is used by the ESS.

3. Issue a Start Receive command to the EAC. The EAC will enter in receive mode where it is allowed to start receiving packets from the line.
4. Start a timer to wait for any received packets. This timer value will be internal to the microcode, but must be less that the NCP backup timer value used to wait for any command status.
5. If any statistical counters have overflowed, bit 7 of the SCF status will be set indicating this fact.
6. When an end of message interrupt is received from the EAC or the receive timer expires, build an ending status and transfer it to the CCU.
7. Set a CCU level 2 interrupt request.

Typical Ending Statuses

SCF	SES	LCS	Meaning
4C	00	00	End of frame, data stored
4D	00	00	End of frame and counters overflowed
00	00	80	Timeout, no packets received
01	00	80	Timeout and counters overflowed
00	00	D2	Command rejected
00	00	See[1]	Internal box error
C4	00	00	Halt executed

[1] = Refer to “Line Communication Status (LCS)” on page 14-26 for details.

Get Counters

The Get Counters command is used to pass the address of an NCP buffer to be used by the ESS to return error counter information. This command is issued by NCP in response to a counters overflowed status on a receive command (SCF bit 7 on) from the ESS. It may also be issued at other times when deemed necessary by NCP to retrieve the current set of counters.

CSP Processing

1. Get the parameters from the CCU.
2. Place the counters in the buffer provided.
3. Build an ending status and transfer it to the CCU. This status will include the 'Counters that Overflowed' status byte.
4. Set a CCU level 2 interrupt request.

Typical Ending Statuses

SCF	SES	LCS	Meaning
4C	00	00	Counter Data Stored
00	00	D2	Command rejected
00	00	See[1]	Internal box error
C4	00	00	Halt executed

[1] = Refer to “Line Communication Status (LCS)” on page 14-26 for details.

Halt

The halt command is used to terminate an outstanding command before it completes. The halt, service request and EOM bits are set in the SCF. Other status bits are not changed. Thus, the status will show any condition that existed at the time the halt was processed. Refer to the SCF bit description on page 14-25 for more details.

The following commands may not be Halted:

- Start Trace
- Stop Trace
- Dump control blocks (no status)
- Dump control blocks (status)

Any attempt to halt these commands will result in unexpected responses from the ESS.

A halt to any of the following commands is ignored:

- Set Mode
- Disable
- Change

However, it is not an error to issue a halt when one of these commands is in process.

If no command is active in the CSP when a halt is issued, the halt becomes the outstanding command. Activity on the line is halted; an ending status is built for the halt command and sent to the CCU.

Consecutive halts with no intervening CCU level 2 interrupt will cause a CCU level 1 command reject interrupt from the ESS.

It is possible that status for an outstanding command has been built and sent to the CCU and a CCU level 2 interrupt has been set at the time a Halt command is issued, but the NCP has not yet honored the interrupt (the line ID is still waiting in the CSP).

In this case, the CSP will invalidate the queued line ID. A new line ID, formed by adding X'80' to the low halfword of the special LNVT address, replaces the old ID. The halt will then become the outstanding command.

CSP Processing

1. Make the halt the outstanding command if there is no other command in process.
2. Perform the defined operation.
3. Update the status area and transfer it to the CCU.
4. Raise a CCU level 2 interrupt.

Halt Immediate Command

The halt immediate (Halti) command is used to terminate an outstanding command and does not require a CCU level 2 status interrupt from the ESS.

In general, the halt immediate command may be issued to the CSP at any time, whether or not there is an outstanding command. However, the following commands may not be Halti'ed:

- Start Trace
- Stop Trace
- Dump control blocks (status)

Any attempt to Halti these commands will result in unexpected responses from the ESS.

A Halti to the following command is ignored:

- Dump control blocks (no status)

However, it is not an error to issue a Halti when this command is in process.

The Halt Immediate command requires no parameters and builds no status; therefore, no PSA transfer to or from CCU storage occurs.

The Halt Immediate command does not create an outstanding command condition in the CSP. Therefore, the control program may issue a Halti and follow it immediately with another command.

The CSP will ignore a Halti if it is issued when there is no outstanding command.

If a command is outstanding to both the CCU and CSP at the time the Halti is issued, the CSP will:

1. Perform the defined operation.
2. Discard any pending status.

Line Dump Commands

See "Chapter 13".

Start Scanner Interface Trace (SIT) and Stop Trace

See "Chapter 13".

Microcode Interaction With MOSS

The interconnection between the MOSS and the ELA is based on:

- IOH instructions issued by MOSS.
- A dedicated communication area located in CCU storage called the 'MOSS area'. This area can be read and written by MOSS and by the ELA. It is divided into two parts:
  - A parameter/status area in which each of the scanners has its own specific 'mail box'.
  - A data area used by functions like 'Alter/Display', 'Dump', 'IML' and 'Init'.
- A special interrupt line through which a scanner can interrupt MOSS on level 4 to signal completion of a command.

In all cases, the ELA acts as a slave to the MOSS and therefore cannot initiate any unexpected action. The MOSS communicates with only one scanner at a time.

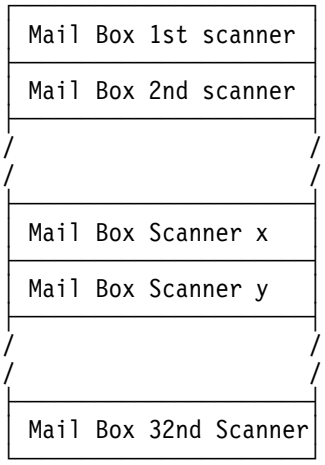
Communication Schemes

Communications between MOSS and the ELA for any function requested from MOSS follows one of these schemes:

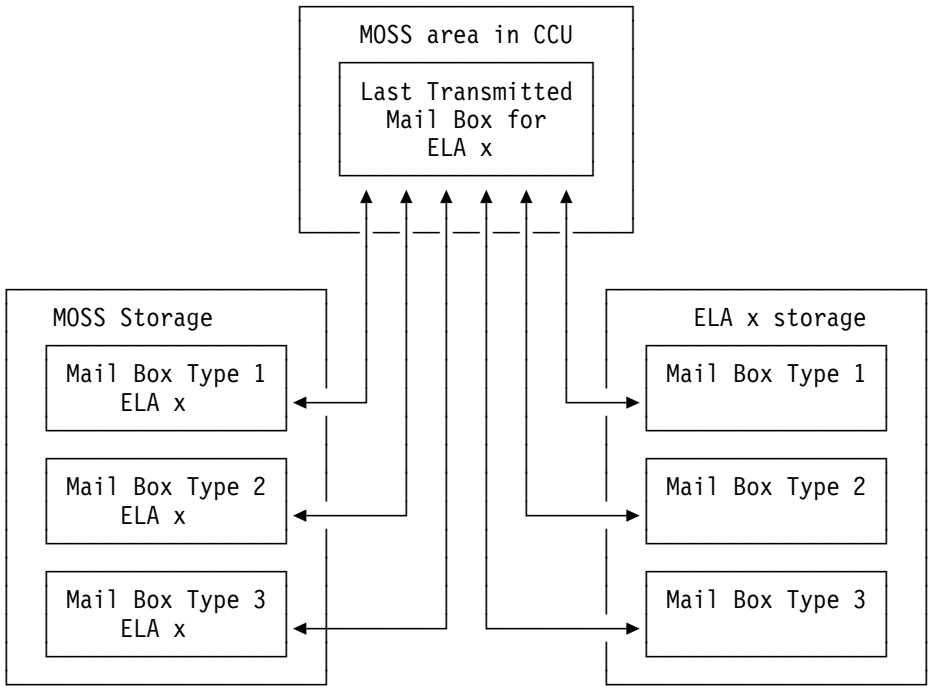
1. Input IOH where two bytes of data are synchronously returned to MOSS at the TD area of the IOH. The MOSS area is not used. There is no MOSS interrupt. The following applications use this scheme:
   - Get scanner status
   - Get processor checkout results
   - Get command completion
   - Get error status.
2. Output IOH where there is no mail box and no interrupt. MOSS sets a timer at the completion of which it can interrogate the ELA with an input IOH. The following applications use this scheme:
   - Scanner reset
   - Run processor checkout
   - Set MOSS area high
   - Set MOSS area low.
3. Output IOH where the mail box is used for status and/or parameters and no interrupt. The ELA transfers its own mail box from the MOSS area into CSP storage to get the parameters. After completion of the command, the ELA puts its command status into the status part of the MOSS area mail box.
4. Output IOH where there are no mail box for parameters, status in mail box for errors, MOSS interrupt. MOSS waits for its timer to expire or for the ELA interrupt.
5. Output IOH where the mail box is used for parameters, status for errors, interrupt. MOSS waits for its timer to expire or for the ELA interrupt.

MOSS Area Layout

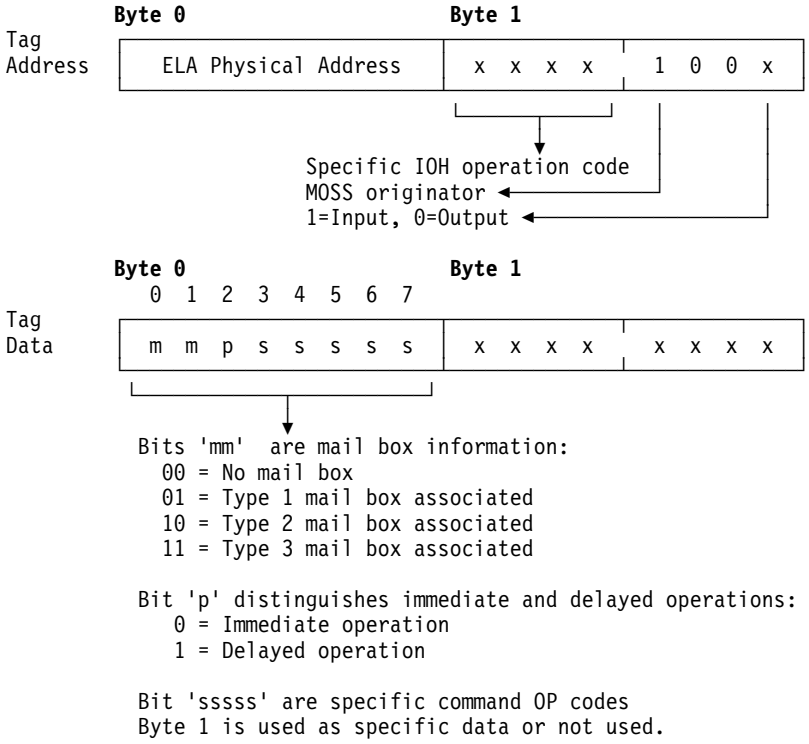
The MOSS area is located in CCU storage. The beginning address of this area is provided to the ELA via the set MOSS area high and set MOSS area low IOHs. The following figure shows the scanners/MOSS mail box area layout used by the ELA:



Mail Box Layout



MOSS I/O Instruction (MMIO)



Scanner Status After the IML

At the end of scanner IML it is possible to get from the CCU storage, the status of the scanners associated with their mailbox.

The 16-byte mailboxes are located from CCU storage address 3F8000 (for 4MB storage) or 7F8000 (for 8MB storage).

The status of the scanners just IMLed are in the last two bytes of the mailbox. These values must be displayed before any mailbox exchange between the CCU storage and the corresponding scanner (for example: CCU functions). Below are the possible statuses of the scanner after an IML:

Values	Description
X'nnFF'	No answer from scanner following the MOSS cmd 'nn'
X'C900'	Normal status IML OK
X'C901'	ECA RAM checkout or ECA picocode load failed
X'C902'	EAC card and picocode level not compatible
X'C904'	EAC card not installed
X'C90A'	No response from EAC during the fetch of universally administered address from EAC EPROMs
X'C90C'	Universally administered address not valid

Figure 14-6. Values of the Last Two Bytes of the Mailboxes after IML

ELA Registers

ELA CSP External Registers

The ELA CSP microcode uses the same external register format and numbering as the LSS CSP microcode. Refer to the Chapter 4, "Transmission Subsystem" for more information on the CSP external register bit descriptions.

EAC External Registers

This status register contains information about the type of status from the EAC . CSP storage will contain the actual status information.

The EAC will load the status details into a CSP data area, set the status type into XR 10, and then raise a level 2 interrupt to the microcode indicating that the status is available. The microcode then can obtain this status Xreg (x'10') to determine the type of status (such as: transmit, receive, DMA,), and obtain the status details from a data area in CSP storage.

ELA External Register Details

XR10 0 1 2 3 4 5 6 7	Meaning
1 0 0 0 0 0 0 v	Transmit initial status
1 0 0 0 w x 1 v	Transmit final status w = 1 means transmit overrun x = 1 means transmit frame > 1514 bytes
0 1 0 0 y z 0 v	Receive status y = 1 means NCP buffer depletion z = 1 means receive frame > 1518 bytes
0 1 0 0 0 0 1 v	Receive stopped
0 0 1 0 0 0 0 v	DMA error status
0 0 1 0 0 0 1 v	EAC internal error status
0 0 0 1 0 0 0 v	Error status from CSR0
0 0 0 0 1 0 0 v	Initialization complete
0 0 0 0 1 0 1 v	Disable complete

- v = 0 : Status is for first EAC port
  v = 1 : Status is for second EAC port
- w = Transmit overrun indicates that neither of the two internal EAC transmit buffers is free to be used by DMA for this new transmit command.
- x = Transmit frame too long indicates that the picocode detected a frame more than 1514 bytes long during the process of DMAing the data from the CCU.
- y = NCP buffer depletion is set during the DMA process on receive if the EAC picocode detects an end of buffer chain condition before all of the packet had been DMAed from a single EAC receive buffer.
- z = Receive frame too long is set by the picocode when it detects a frame of greater than 1518 bytes received.

The following sections explain in more details the statuses.

Transmit Initial Status (XR10 = X'80' or X'81')

CSP Storage Address	Bit	Meaning
9018	0-15	Starting address of transmit data in EAC
9019	0-15	Count in bytes of xmit data DMAed by the EAC (value is in normal binary form)

Transmit Final Status (XR10 = X'82' or X'83')

CSP Storage Address	Bit 0 1 2 3 4 5 6 7	Meaning
9016	x	Not used
	. x	One or more errors occurred
	. . x	Not used
	. . . x	More than one retry needed to transmit a packet
	. . . . x . . .	One retry needed to transmit a packet
	. . . . . x . .	The EAC had to defer while trying to transmit a packet
	6-15	Not used
9017	x	No end of packet flag in the current buffer
	. x	Underflow, message truncated
	. . x	Not used
	. . . x	Collision occurred after a slot time
	. . . . x . . .	Loss of carrier
	. . . . . x . .	Retry error
	6- 15	Time domain reflectometry

Receive Status (XR10 = X'40' or X'41')

CSP Storage Address	Bit 0 1 2 3 4 5 6 7	Meaning
9016	x . . . . x . . . . x . . . . x . . . . x . . . . x . . 6-15	Not used One or more errors occurred Framing error Overflow error CRC error in incoming packet Buffer error Not used

Disable Complete (XR10 = X'0A' or X'0B')

The EAC will present this status to the microcode in XR10 after the requested or Disable Port command function is completed.

DMA Error Status (XR10 = X'20' or X'21')

SCP Storage Address	Bit 0 1 2 3 4 5 6 7	Meaning
9016	1 . . . . 0 . . . . 0 . . . . x . . . . x . . . . x . . . . x . . . . x 1 . . . . 0 . . . . 1 . . . . x . . . . x . . . . x . . . . x x	Always 1 Always 0 Always 0 DMA interface error DMA time out DMA burst count error DMA error during read (1) or write (0) DMA driver fault Always 1 Always 0 Always 1 SCTL/DMSW error line 0 SCTL/DMSW error line 1 SCTL/DMSW error line 2 SCTL/DMSW error line 3 Not used

CSR0 Status (XR10 = X'10' or X'11')

CSP Storage Address	Bit 0 1 2 3 4 5 6 7	Meaning
9016	x . . . . x . . . . x . . . . x . . . . x . . . 5-15	Error status Transmitter timeout error Collision error Missed packet Storage error Not used

EAC Error Status (XR10 = X'22' or X'23')

CSP Storage Address	Bit 0 1 2 3 4 5 6 7	Meaning
9016	x . . . . x . . . . x . . . . x . . . . x . . . 5-15	Not used Not used Not used CSP INTERCONNECTION ERROR EAC INTERNAL ERROR Not used

EAC Initialization Complete (XR10 = X'08' or X'09')

The EAC will present this status to the microcode in XR10 when it finishes the functions associated with the INIT command from the microcode. No CSP storage status bits are required.

Receive Stopped (XR10 = X'42' or X'43')

The EAC will present this status to the microcode in XR10 when a Stop Receive command has been completed. No CSP storage status bits are required.

Registers for Indirect Addressing Format

Following are the components required to indirectly address the EAC areas and the bits of those components used to access a particular area.

Area	Paging Register 0 1 2 3	XR13 0 2 3 4 5 6 7	XR12 0 1 2 3 4 5 6 7
IXR	- - - -	- - - - - - -	x x x x x a 0 1
XRAM	x x x x	0 x x x x x x	x x x x x a 1 0
State Machine	- - - -	x x x x x x x	x x x x x a 1 1
Special Regs	- - - -	0 0 0 0 0 0 0	0 0 x x x a 1 0

- The 'x' indicates that these bits are used to address the particular area. The high order address bit is the left most 'x' bit on each line.
- The 'a' bit of XR12 defines the read or write access of the area:
  - 'a' = 0 for write
  - 'a' = 1 for read
- Bits 6 and 7 of XR12 indicate the area to be accessed in the ECA:
  - '0 1' = IXR
  - '1 0' = XRAM or special registers
  - '1 1' = State machine
- State machine RAM are a maximum of 512 halfwords long each. Bits 4-7 of XR13 and 0-4 of XR12 select the halfword address inside the particular state machine RAM. Bits 0-3 of XR13 select the state machine RAM. For the EAC, only the following RAMs are available:

XR13 0 1 2 3	State Machine	Meaning
1 0 0 0	CSP	Most significant half
1 0 0 1	CSP	Least significant half
1 0 1 0	DMA	Most significant half
1 0 1 1	DMA	Least significant half

- EAC special registers:

XR12 2 3 4	Read/Write	Meaning
0 0 0	R/W	Data buffer port 1
0 0 1	R/W	Data buffer port 2
0 1 0	W	Paging register for microcode use
0 1 1	W	Paging register for picocode use
1 0 0	W	Function register
0 1 0	W	Ready register

Data Register 1 (XR 14)

Addr	Bit 0 1 2 3 4 5 6 7	Meaning
14	x	Data bit 0
	. x	Data bit 1
	. . x	Data bit 2
	. . . x	Data bit 3
	. . . . x . . .	Data bit 4
	. . . . . x . .	Data bit 5
	. . . . . . x .	Data bit 6
	 x	Data bit 7

Data Register 2 (XR 15)

	Bit	
15	x	Data bit 0
	. x	Data bit 1
	. . x	Data bit 2
	. . . x	Data bit 3
	. . . . x . . .	Data bit 4
	. . . . . x . .	Data bit 5
	. . . . . . x .	Data bit 6
	 x	Data bit 7

Miscellaneous EAC Register (XR 17)

Addr	Bit 0 1 2 3 4 5 6 7	Meaning
17	x	Not used
	. x	Freeze EAC
	. . x	EAC EC level bit 0 (adapter definition)
	. . . x	EAC EC level bit 1
	. . . . x . . .	EAC EC level bit 2
	. . . . . x . .	CDS bit 0
	. . . . . . x .	CDS bit 1
	 x	CDS bit 2

NCP Receive Data Maximum Length (EAC Indirect Register IXR 00)

This register contains the NCP receive data maximum length provided by NCP with the set mode command.

DMA Diagnostics Register Format (ECA Indirect Register IXR 10)

Bit 0 1 2 3 4 5 6 7	Meaning
x	Disable '+ DMA Ready' signal from switch card
. x	a] See note below
. . x	b]
. . . x	Force bad parity on external register address
. . . . x . . .	Force bad parity on cycle steal address
. . . . . x . .	Disable external register data parity checker
. . . . . . x .	Disable external RAM parity checkers
. . . . x	Disable all internal data bus parity checkers

Note: a b = 0 0 Normal operation
0 1 Force bad parity on EAC-to-SCTL transfer
1 0 Force bad parity on SCTL-to-EAC transfer (byte 0)
1 1 Force bad parity on SCTL-to-EAC transfer (byte 1)

Error Detection and Reporting

Program/Hardware Checks

In addition to the program/hardware errors reported in the command status via level 2 interrupts, the CCU may be notified by a CCU level 1 interrupt that a program or hardware check occurred.

To obtain the error information, the control program issues a get error status instruction, which transfers a two-byte error status to the CCU.

The control program also resets the check and the interrupt, and performs the recovery actions. The following conditions may cause a level 1 program or hardware check:

1. CCU/ELA problems:
   - IOH/IOHI instruction not supported.
   - IOH/IOHI rejected because there is already an outstanding command on the interconnection. For example, a second transmit command has been sent while a transmit command is already outstanding.
   - IOH/IOHI rejected because a set mode command has not yet been received for that line.
   - Abnormal conditions detected during I/O operations on the IOC bus. These errors may be detected by the CCU or by the ELA. Errors are related to CCU storage and address checks, invalid sequences, and timed-out IOH/IOHI instructions.
2. ELA problems:
   - Invalid interrupts.
   - Microcode-detected program failures. (These set the microcode check bit in the error status and cause the NCP to issue a get microcode check instruction.)
   - CCU level 2 interrupt stack overflow.
   - CSP or EAC hardware check (for example parity or address check).

If the check is not related to a particular line, the CSP microcode builds the error status, freezes the EAC, and waits for the get error status IOH.

For some severe errors, the CSP enters the disconnect/stop environment and ignores all IOH instructions generated by the NCP. Re-IML of the CSP microcode is required to return to an operational state.

Refer to “Error Status” on page 14-56 for the error status description.

Hardware Error Detection and Reporting

Two types of error:

- DMA and modem interface errors which raise the level 2 interrupt to the CSP.
- Errors which raise the level 0 interrupt to the CSP.

Internal Box Error (IBE) Reporting

The internal box errors generate box event records (BERs). For details on BERs, see chapter 12.

The IBEs can be divided into three categories:

1. CSP and EAC internal errors or events (similar to the errors defined for the CSP/FES in the LSS):
   - Adapter interconnection check
   - CSP/EAC interconnection error
   - EAC failing to answer
   - Transmitter error
   - Invalid interrupt from EAC
   - Command rejected
   - Trace already active
   - EAC internal error
   - EAC hardware not ready
   - AIO error
   - Frame greater than 1518 bytes
   - Collision error
   - EAC receiver lost part or all of a packet
   - Internal EAC transmit buffers not free
2. DMA errors detected by the EAC:
   - DMA parity error during write or read
   - DMA time out during write or read
   - DMA bus driver fault
   - DMA burst count error
   - DMA interconnection errors for improper DMA tag sequence.
3. Errors detected in the SCTL/switch cards:
   - Storage internal error
   - SCTL internal error
   - DMA internal error
   - DMA logical error
   - DMA storage protect/address exception
   - DMA interconnection error in read or write (a)
   - DMSW parity check main bus (b)
   - DMSW parity check primary/secondary bus (c)
   - DMSW driver fault. (d)

Notes:

1. The following errors can occur concurrently:
   - a and b
   - b and c
   - b and d
   - a, b, and c
2. All the errors listed above are reported to the NCP via a level 2 interrupt and associated status area as an LCS and ELCS code (refer to “Line Communication Status (LCS)” on page 14-26, “Extended Line Communication Status (ELCS) For LCS X'D2'” on page 14-28, and “Extended Line Communication Status (ELCS) For LCS X'DC'” on page 14-29 for codes description).

3. The SCTL/switch errors and the EAC DMA interconnection errors are mutually exclusive. There is no double-reporting of errors.

DMA Interconnection Errors Detected by EAC (Register X'10')

DMA Tag Sequence

The EAC circuitry monitors the sequence of the DMA interconnection signals from the SCTL/switch card.

An error is reported when the tag sequence does not occur properly.

DMA Data Bus Parity Checker

This parity checker verifies the validity of the data received/sent, from/to the DMA data bus byte 0 and byte 1 by the EAC.

DMA Time out

One hardware timer is implemented to detect possible time out conditions on the DMA bus.

The duration of the timer is in the range of 100 ms to cover a complete transfer operation on the DMA bus.

DMA Burst Count Checker

This checker verifies that the transfer is successfully completed on the DMA bus when the burst count in the EAC reaches zero.

SCTL/Switch Card Detected Errors Reported by EAC

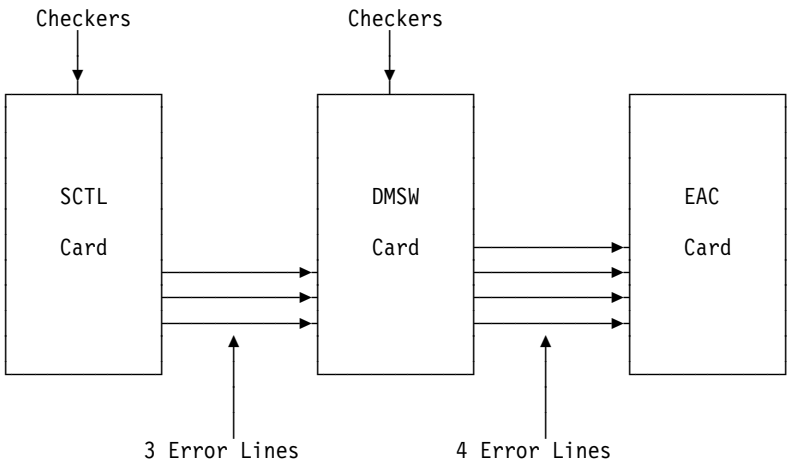
The SCTL-DMA card and the switch cards have internal checkers which detect the following error conditions which may occur during a DMA transfer initiated by an ELA (see the figure 'Line Error Hexadecimal Code' next):

Line Error Hexadecimal Code	SCTL–DMA/Switch Error Conditions								
	a	b	c	d	e	f	g	h	i
0	Normal mode (no error)								
1	x								
2		x							
3			x						
4				x					
5					x				
6						x			
7							x		
8								x	
9									x
A					x	x			
B						x	x		
C						x		x	
D									
E									
F					x	x	x		

Figure 14-7. Line Error Hexadecimal Code

- SCTL error detection:
  a. DMA internal error
  b. DMA logical error
  c. DMA storage protect/address exception error
  d. Storage unrecoverable error or control error
  e. DMA interconnection error.
     - Switch card error detection:
  f. DMSW parity check main bus
  g. DMSW parity check primary/secondary bus
  h. DMSW DMA driver fault
  i. Not used

The error conditions just described are encoded by the SCTL-DMA card and the switch card, and reported on 4 x SCTL/DMSW error lines which go from the DMSW card to the EAC card as shown in the following figure:



Reporting

Reporting of DMA errors is done by issuing a level 2 interrupt to the CSP. The nature of the error is set into an LCS/ELCS (refer to “Line Communication Status (LCS)” on page 14-26 and “Extended Line Communication Status (ELCS) For LCS X'D2'” on page 14-28 for code description).

When any of the above checkers becomes active:

1. The hardware:
   - Stores the corresponding error condition in an error register X'10' and CSP storage.
   - Interrupts the CSP microcode.
2. The CSP microcode
   - Stops the transmit and receive operations in process.
   - In case of transmit, puts the transmit data line at mark.
   - In case of receive, stops the receive command.

DMA/SCTL Errors

They are reported by the EAC through a level 2 interrupt and then both interfaces are disabled by the microcode.

The CSP microcode fills the LCS field of the PSA status with a status byte giving the reason for the error (refer to “Line Communication Status (LCS)” on page 14-26 and “Extended Line Communication Status (ELCS) For LCS X'DC'” on page 14-29 for code description).

The microcode then raises CCU level 2 interrupt.

Line interfaces are started again by the CSP microcode when the NCP sends the proper command sequence.

CSP Interconnection Errors

The CSP communicates with the EAC through the external registers located in the EAC (register range X'0D' to X'17').

The EAC completes the operation with the 'acknowledge' signal to the CSP if no error conditions were detected.

The EAC monitors the CSP interconnection for the following errors:

- Interconnection error signal from the CSP
- Bidirectional cycle steal data bus parity error
- External register address and select out parity error
- Data out odd parity error during an external register write operation.
- External register address invalid.

If an error occurs in the external register address because of a parity error or because the external register does not exist in the EAC, the 'acknowledge' signal is not sent to the CSP.

Also, if the data bus parity is incorrect during an external register write, the 'acknowledge' signal is not sent to the CSP.

When 'acknowledge' is not returned to the CSP by the EAC, the CSP sets the adapter interconnection check bit ON (external register X'03' bit 6 = 1) and terminates the operation.

The EAC does not report any error condition.

Parity errors occurring on the cycle steal interconnection can be detected by the EAC or by the CSP.

If the EAC detects a parity error on the data bus during a cycle steal write, the EAC sets a level 2 interrupt to the CSP with the CSP interconnection error status set after completing the operation.

The parity checking on the cycle steal address bus and the CSP data bus during a cycle steal or external register read operation is performed by the CSP.

When the CSP detects a parity error, the CSP sets the adapter interconnection check in the CSP register X'03' and activates the 'cycle steal error' line.

When the EAC detects this signal, the cycle steal operation ceases and the EAC activates a level 2 interrupt to the CSP.

The CSP interconnection error bit is set ON in the EAC external register X'10'.

Detection of this error causes a level 2 interrupt to the CSP.

If an NCP transmit or receive operation is in progress, it continues until the CSP microcode stops reception of data for the receive command, or stops transmission of data and sets the transmission line to mark.

EAC Internal Checkers

Data Parity Checkers

All the microcode (DMA layer, CSP layer) and data are checked for parity when the EAC internal buffers are read or written.

Reporting

When any of the above checkers becomes active:

- The EAC:
  - Stores the corresponding error condition in an error register.
  - Interrupts the CSP microcode at level 0.
- The CSP Microcode:
  - Provides a level 1 status to the control program.

Error Status

The error status is provided as the LA or L-STAT field in some ESS 08 type BERs. Refer to Chapter 12.

Four types of error may be reported:

Type 1 Error detected by the CCU during PIO. A halt is send to the CSP, which results in a CCU or MOSS level 1 interrupt.

Type 2 Error detected by the CCU during AIO. A halt is send to the CSP, which results in a CCU or MOSS level 1 interrupt.

Type 3 Internal logical errors detected by the CSP microcode. A CCU level 1 or MOSS level 4 interrupt is set.

Hard Stop A CSP microprocessor check has been encountered. The CSP hardware responds with the error status.

The following tables show the detailed responses that may be presented to a get error status command:

Error Status Byte 0

Bit 0123 4567	Type 1	Type 2	Type 3
x...	R/W (IOH)	R/W (AIO)	Always ON
.x..	I/O bus check	I/O bus check	Invalid level 0 int.
..x.	Not used	Cycle steal grant	Invalid level 1 int.
...x	I/O bus tag I/O	I/O bus tag I/O	Invalid level 2 int.
.... x...	Halt	Halt	Microcode check
.... .x..	TA	Not used	CS/CCU L2 stack overf.
.... ..x.	TD	TD	Reject: command on cmd
....x	Not used	Not used	Disconnect state

Error Status Byte 1

Bit 0123 4567	Type 1	Type 2	Type 3
x...	TA select	Not used	Command reject
.x..	Not used	Cycle steal select	Invalid output IOH type
..x.	Not used	Not used	┐
...x	Not used	Line interface address bit 0	│
.... x...	Not used	Line interface address bit 1	│
.... .x..	Not used	Line interface address bit 2	├ See note below
.... ..x.	Not used	Line interface address bit 3	│
....x	Invalid input IOH	Line interface address bit 4	┘
....x			Adapter interconn. check

Note: Next comes the decoding of bits 0 to 7 when command reject occurs.

Bit 0123 4567	Normal Command Reject	Trace Command Reject	Invalid Output IOH
x...	Command reject	Command reject	Always OFF
.x..	Always OFF	Always ON	Invalid output IOH
..x.	┐	Not used	Not used
...x	│ Line interface	Not used	┐
.... x...	├ address	┐	│ Line interface
.... .x..	│ (0 to 3F)	├ Slot number	├ address
.... ..x.	│	│ (0 to F)	│ (0 to 1F)
....x	┘	┘	┘

Hard Stop Error Status (Detected by CSP Hardware)

Byte 0

Bit 0 1 2 3 4 5 6 7	Meaning	
* * * * * . . .	Not used	
. . . . . x . .	Control store data check	Only if processor check
. . . . . . x .	LSR or external register parity check	Only if processor check
. . . . x	Internal check	Only if processor check

Byte 1

Bit 0 1 2 3 4 5 6 7	Meaning
x	Unexpected adapter acknowledgment
. x	Control store write data check
. . x	Processor check
. . . x	External register address check
. . . . x . . .	Control store address check
. . . . . x . .	LSR address check
. . . . . * *	Not used

Diagnostic Facilities

Refer to the *3745 Diagnostic Descriptions*, SY33-2059, for more details.

Problem Determination Aids

The following tools are provided to help define which area is failing:

1. Scanner interface trace (SIT) and checkpoint trace (Refer to Chapter 13, "Traces, Dumps and file transfer" in this manual).
2. ESS interface display (EID).
3. LSS functions from the MOSS service menu (see *Service Functions Manual*, SY33-2055).

Microcode Service Aids

The EAC registers, the microcode RAM locations and the external data control RAM locations can be accessed, using the following facilities (See *Service Functions Manual*, SY33-2055, and *Advanced Operations Guide*, SA33-0097):

1. Alter/display
2. CSP address compare
3. CSP dumps.

These facilities, invoked from the operator console, help in analyzing/modifying the contents of the ELA storage and registers (CSP and EAC): (see “ELA Registers” on page 14-42 for register description).

Programming Support for Problem Determination

It includes, as for LSS microcode:

1. Error detection
2. Error collection
3. Error reporting.

Types of errors tracked are:

- CSP/IOC bus interconnection errors
- CSP internal errors
- CSP/EAC interconnection errors
- DMA/SCTL/Switch errors
- EAC errors
- EAC-to-line interface errors.

NCP Buffer Prefix Validity Checking in Receive

This test is performed by the microcode for the first buffer only, by using the parameters coming from the PSA.

SIT Trace

The scanner interface trace (SIT) traces the address and control field, and up to 252 data bytes of each frame transmitted or received by the EAC card.

For the CSP, the NCP commands and the CCU IOH commands are also traced to provide a listing of the command and data transmission sequence for the line.

Refer to Chapter 13 "Traces, Dumps and File Transfer" in this manual, for more information.

List of Abbreviations

A	ampere
abend	abnormal end of task
ABP	active bypass card
AC	1) alternating current 2) abandon call 3) address compare
ACB	adapter control block
ACF	Advanced Communications Function
ACK	affirmative acknowledgement (BSC)
ACPW	ac power box
ACR	1) add character register (instruction) 2) abandon call request
ACU	automatic calling unit
ACUN	acccess unit (token ring access unit such as the IBM 8228)
AC1	ac power box (ACPW) installed in position 1 of the 3746-900
AC2	ac power box (ACPW) installed in position 2 of the 3746-900
ADB1	adapter bus 1
ADB2	adapter bus 2
ADB3	adapter bus 3
ADB4	adapter bus 4
AE	address exception
AEK	address exception key
AFD	airflow detector
AGC	automatic gain control (signal)
AHR	add halfword register (instruction)
AIO	adapter-initiated operation
AIT	algorithm interface table
ALC	Airlines Line Control
ALU	arithmetic and logic unit
AMD	air moving device
ANSI	American National Standards Institute
AR	add register (instruction)
ARC	active remote connector
ARI	add register immediate (instruction)
AS	autoselection chain
ASCII	American National Standard Code for Information Interchange
AUI	attachment unit interface
AXB	adapter expansion block
B	1) branch (instruction) 2) byte
BAL	branch and link (instruction)
BALR	branch and link register (instruction)
BAT	basic assurance test
BB	branch on bit (instruction)
BCC	block check character (BSC)
BCCA	buffer chaining channel adapter
BCCW	bit clock control word
BCD	binary-coded decimal notation
BCL	branch on C latch (instruction)
BCLE	buffer control list element
BCT	branch on count (instruction)
BER	box event record
B/M	bill of material
BPC1	bus propagation card type 1
BPC2	bus propagation card type 2
bps	bits per second
BR	bus request
BRC	BER reference code
BSC	binary synchronous communication
BT	branch trace
BTAM	Basic Telecommunications Access Method
BTAM-ES	BTAM extended support
BZL	branch on Z latch (instruction)
C	1) Celsius 2) control (X.21 signal)
CA	channel adapter
CAB	channel adapter board
CAC	common adapter code
CACM	channel adapter concurrent maintenance
CADR	channel adapter driver receiver card
CADRUK	channel adapter driver receiver type UK card
CADS	channel adapter data streaming
CAL	channel adapter logic card
CAL6	CAL type 6 for CADS
CAL7	CAL type 7 for BCCA

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CAMPOR CA MOSS power-ON-reset (register)

CARST CA reset (register)

CATPS channel adapter with two-processor switch

CB circuit breaker

CBC controller bus coupler

CBTRA controller bus and token-ring adapter

CBSA controller bus and service adapter (CBSP+CBC+TIC3)

CBSP controller bus and service processor

CCITT Comite Consultatif International Telegraphique et Telephonique. The International Telegraph and Telephone Consultative Committee

CCMD current command (storage)

CCN communications controller node

CCPF common customer profile facility

CCR compare character register (instruction)

CCU central control unit

CCW channel command word

CD 1) carrier detector (signal)
2) connector

CDF configuration data file

CDG concurrent diagnostic

CDS configuration data set (NCP/EP)

CE customer engineer

CEPT Comite Europeen des Postes et Telecommunications

CHCV channel control vector

CHCW channel control word

CHIO channel input/output

CHPID channel path identification

CHR compare halfword register (instruction)

CI calling indicator (signal)

CLDP controller load/dump program

CLP communication line processor

CMOS complementary metal oxide semiconductor

CMSA CCU/MOSS status register A

CMSB CCU/MOSS status register B

CMSC CCU/MOSS status register C

CNM communication network management

CNMI communication network management interface

CNSL console

CO/CS contact operate/contact sense

CONFSW configuration switch

CP 1) communication processor, control program
2) circuit protector

CPIT control program information table

CPM connection point manager

CPN customer problem number

CPR channel pointer register

CPT checkpoint trace

CR 1) compare register (instruction)
2) call request (signal)

CRC cyclic redundancy check character

CRI compare register immediate (instruction)

CRP check record pool

CRQ call request

CRU customer replaceable unit

CS 1) cycle steal
2) communication scanner
3) connectivity switch

CSA common subassembly

CSC connectivity switch cable

CSCE connectivity switch cable extension

CSCW cycle steal control word

CSG cycle steal grant

CSGH cycle steal grant high

CSGL cycle steal grant low

CSP communication scanner processor

CSR cycle steal request

CSRH cycle steal request high

CSRL cycle steal request low

CSS control subsystem

CSU 1) customer setup
2) customer service unit (DCE-like for high-speed communication lines)

CSW channel status word

CTS clear to send (signal)

CW control word

CZ carry/zero (latch)

DAF destination address field (SNA)

DB data byte

DC 1) direct current
2) data chaining (channel status)

DCAF Distributed Console Access Facility

DCDP dc distribution and protection box

DCE data circuit-terminating equipment

DCF diagnostic control function

DCM diagnostic control monitor

DCPW dc power box

DCRLSD data channel receive line signal detector (same as CD)

DDS digital data service

DE device end (channel status)

DFA disk file adapter card

DFI defect-free installation

DI data in

DICO DMA IOC connection card

DIFF differentiator

DIV diagnostic information vector

DLE data link escape character

DLO data line occupied (signal)

DMA direct memory access

DMSW direct memory access switch card

DMUX double multiplex card for board on LIC unit 1

DO data out

DOI duration of interrupt

DP digit present (signal)

DPR digit present request

DRA duration of repair action

DRS data rate select

DRV driver

DS data streaming

DSC distant station connected

DSI data store interface

DSR data set ready (signal)

DSRS data signaling rate selection (signal)

DSU data service unit (DCE-like for high-speed communication lines)

DTE data terminal equipment

DTER DMA bus terminator

DTR data terminal ready (signal)

DVB device block

DX duplex

EAC Ethernet adapter card

EBCDIC extended binary-coded decimal interchange code

EC engineering change

ECB even control block

ECC error checking and correction

EDE elementary data exchange

ED/FI error detection/fault isolation

EIA Electronic Industries Association

EIB error intermediate block

EINTP1 extended interrupt 1 (register)

EIRV error interrupt request vector

ELA Ethernet LAN adapter

ELCS extended line communication status

ENQ enquiry (BSC)

EOT end of transmission (BSC)

EP emulation program

EPO emergency power-OFF

ERC error reference code

EREP environmental recording, editing, and printing (program)

ERP error recovery procedure

ESC emulation subchannel (address)

ESCA ESCON channel adapter. An ESCA consists of an ESCON channel processor (ESCP) and an ESCON channel coupler (ESCC)

ESCH emulation subchannel high (address)

ESCC ESCON channel coupler. A communication controller hardware unit which is the interface between the ESCON channel processor and the ESCON fiber optic cable

ESCC2 ESCON channel coupler type 2

ESCL emulation subchannel low (address)

ESCON channel A channel having an Enterprise System Connection* channel-control-unit interface that uses optical cables as a transmission medium

ESCP ESCON channel adapter. A communication controller hardware unit which provides the channel data link control for the ESCON channel adapter

ESD electrostatic discharge

ESS Ethernet subsystem

ETB end-of-transmission block character (BSC)

ETG Ethernet tail gate

ETX end-of-text character (BSC)

EXP expected

FAC flag address control (SDLC frame)

FALC front end scanner low speed card for Air Line Control (ALC) lines

FCC Federal Communications Commission

FCPS final call progress signals (X.21)

FCS frame check sequence

FDD flexible disk drive

FDS flat distribution system

FDX full-duplex (synonym for duplex)

FE field engineering

FEIS field engineering information system

FERR FESA error register

FES front-end scanner

FESA front-end scanner adapter

FESH front-end scanner (high-speed)

FESL front-end scanner (low-speed)

FID4 format identification 4

FM frequency modulation

FPS FES parameter/status

FRPE frame relay performance enhancement

FRU field-replaceable unit

ft foot

GPR general purpose register

GPT generalized PIU trace

GTF generalized trace facility

HCS Hardware Central Service

HDD hard disk drive

HDR header

HDX half-duplex

hex hexadecimal

hh hexadecimal value hh

HLIR high-level interrupt request

HLU highest logical unit (largest CPU in an establishment)

HPP bus high-performance parallel bus

HPTSS high-performance transmission subsystem

HSB high-speed buffer

HSC high-speed channel

HSS high-speed scanner

HW hardware

Hz Hertz

I indication (signal)

IACK interrupt acknowledgement

IAR instruction address register

IBE internal box error

IC insert character (instruction)

ICA integrated communication adapter

ICB interface control block (storage)

ICF internal clock function

ICT insert character and count (instruction)

ICW interface control word

ID identifier

IEEE Institute of Electrical and Electronics Engineers

IFT internal function test

IMB in mailbox (MOSS)

IML initial microcode load

in. inch

IN input (instruction)

INN intermediate network node

INOP inoperative (line, modem, or terminal)

INS information network system

INTP1 interrupt 1 (register)

INTP4 interrupt 4 (register)

IOC input/output control

I/O input/output

IOCB input/output control bus

IOCS input/output control system

IOH input/output halfword (instruction)

IOHI input/output halfword immediate (instruction)

IOIRR input/output interrupt request register

IOIRV input/output interrupt request vector

IOSW input/output switch (card) for 3745 models 21x and 41x

IOSW2 input/output switch (card) for 3745 models 31x and 61x

IPF instruction pre-fetch

IPL initial program load

IPR isolated pacing response (SNA)

IR interrupt request

IRR interrupt request removed

ISDN integrated service digital network

ISL inbound serial link

ISO International Organization for Standardization

ITB intermediate text block (BSC)

ITER IOC bus terminator

IVT isolation verification tests

K 1024 (bytes or words)

KB kilobyte (1024 bytes)

KBD keyboard

kbps kilobits per second

kg kilogram

kHz kilohertz

L load (instruction)

LA 1) load address (instruction)
2) line adapter

LAB line adapter board

LAN local area network

LAP line adapter processor

LAR lagging address register

LAS line adapter status

LCB line control block (storage)

LCBB line connection box base

LCBE line connection box expansion

LCD line control definer (storage)

LCEB line connection enclosure base

LCEE line connection enclosure expansion

LCOR load character with offset register (instruction)

LCPB line connection power base

LCPE line connection power expansion

LCR load character register (instruction)

LCS line communication status (storage)

LDF line description file

LED light-emitting diode

LERR line error register/driver check

LH load halfword (instruction)

LHOR load halfword with offset register (instruction)

LHR load halfword register (instruction)

LIB 1) line interface buffer
2) LIC board

LIB1 LIC board type 1 for LICs type 1, 3, and 4

LIB2 LIC board type 2 for LICs type 5 and 6

LIC line interface coupler card

LIC1 line interface coupler type 1 (card)

LIC3 line interface coupler type 3 (card)

LIC4 line interface coupler type 4 (card)

LIC5 line interface coupler type 5 (card)

LIC6 line interface coupler type 6 (card)

LID line interface display

LIU line interface coupler unit

LIU1 LIC unit 1 for LICs type 1, 3, and 4

LIU2 LIC unit 2 for LICs type 5, and 6

LLAP LIC line analysis procedure

LLB local loopback

LLIR low-level interrupt request

LL2 link level 2 test

LNVT line vector table

LOR load with offset register (instruction)

LPDA Link Problem Determination Aid

LR load register (instruction)

LRC longitudinal redundancy check

LRI load register immediate (instruction) local storage

LRU least-recently used

LS local storage

LSAR local storage address register

LSI large scale integration

LSR local storage register (CSP)

LSS low-speed scanner

LSSD level-sensitive scan design

LT local test

LTC1 line terminator card for CAB1 addressing

LTC2 line terminator card for CAB2 addressing

LU logical unit

m meter

mA milliampere

MAC MOSS adapter card for 3745 models 21x and 41x

MAC2 MOSS adapter card for 3745 models 31x and 61x

MAP maintenance analysis-procedure

MAT manual assurance test

MAU media access unit

MB megabyte; 1 048 576 bytes

MCA MOSS console adapter card

MCAD MOSS/CA adapter

MCC MOSS control card

MCCU MOSS/CCU adapter

MCF microcode fix

MCPC machine check/program check

MCT machine configuration table

MDOR MOSS data operand register

MDR miscellaneous data record

MERR MUX error

MES miscellaneous equipment specification

MFM modified frequency modulation

MHz megahertz

MICB MOSS interface control block

MIM Maintenance Information Manual

min minute

MIO MOSS input/output

MIOC MOSS I/O control bus

MIOH MOSS input/output halfword

MIOHI MOSS input/output halfword immediate

MIP Maintenance Information Procedures

MIR Maintenance Information Reference

MIT MOSS interface table

MLA MOSS LAN adapter

MLC machine level control

MLT machine load table

mm millimeter

MMIO memory mapped input/output

MMOD MOSS mode

MOD modifier

MOSS maintenance and operator subsystem

MOSS-E MOSS extended

MPC MOSS processor card for 3745 Models 210 to 610

MPC2 MOSS processor card for 3745 Models 21A to 61A

MPS multiple port sharing

ms millisecond

MSA machine status area

MSAU multistation access unit

MSC MOSS storage card for 3745 Models 210 to 610

MSC2 MOSS storage card for 3745 Models 21A to 61A

MSD machine status display

MUX multiplex function

mV millivolt

MVS Multi Virtual Storage

NA not applicable

NAK negative acknowledgment character (BSC)

NCCF Network Communications Control Facility

NCP Network Control Program

NCR AND character register (instruction)

NCTE network communication terminal equipment

NHR AND halfword register (instruction)

NLDM Network Logical Data Manager

NMPF network management program facilities

NMVT network management vector transport

NO-OP no-operation instruction

NOSP network operation support program (VTAM)

NPDA Network Problem Determination Application

NPM NetView performance monitor

NPSI network packet switching interface

NR AND register (instruction)

NRI AND register immediate (instruction)

NRZI see NRZ-1

NRZ-1 non return-to-zero change on ones recording

NS new sync (signal)

ns nanosecond

NSC native subchannel (address)

NTO Network Terminal Option

NTT Nippon Telegraph and Telephone (Japanese PTT)

N/A	Not available or not applicable
oc	overcurrent
OCR	OR character register
ODG	offline diagnostic
OEM	original equipment manufacturer
OEMI	original equipment manufacturer's interface
OHR	OR halfword register
OLT	online test
OLTEP	online test executive program
OLTSEP	online test stand-alone execution (program)
OLTS	online test system
OLTT	online terminal test
OMB	out mailbox
OP	operation decode
OR	OR register (instruction)
ORI	OR register immediate (instruction)
OS	Operating System
OSL	outbound serial link
OUT	output (instruction)
ov	overvoltage
PAC	power analog card
PAP	previous adapter present
PAR	problem analysis and repair
PC	personal computer
PCB	power control bus
PCF	primary control field (storage)
PCI	program-controlled interrupt
PCR	power check reset
PCSS	power control subsystem
PCW	processor control word
PCWC	power control wrap card
PD	problem determination
PDAID	problem determination aids
PDB	power distribution board
PDF	parallel data field (storage)
PE	Product Engineering
PEP	partitioned emulation program
PF	programmable function
PFAR	prefetch address register
PI	power indication (signal)
PIO	program-initiated operation
PIRR	program interrupt request register
PIRV	program interrupt request vector
PIU	pass information unit
PKD	portable keypad display
PLC	power logic card
PN	part number
PND	present next digit (signal)
POPR	prefetch operation register
POR	power-ON reset
POS	power ON services
PRC	processor
PROM	programable read-only memory
PS	power supply
PSA	program status area
PSS	power subsystem
PSTCE	product support trained CE
PSTY	power supply type
PSV	program status vector
PSW	program status word
PSx	power supply type x
PTCE	product-trained CE
PTER	power bus terminator
PTF	program temporary fix
PTT	Post, Telephone and Telegraph (agency)
PTX	phototransistor
PU	physical unit
PUC	processor unit card (mpdels 31x and 61x)
PUC1	processor unit card type 1 (models 21A and 41A starting EC D55657)
PV	parity valid (signal)
QAM	quadrature amplitude modulation
RA	repair action
RAC	repair action code
RAS	reliability, availability, and serviceability
RC	receive clock
RCDB	reference code data base
RCV	receive
RD	receive data (signal)
RDB	reference code data base
RECFMS	record formatted maintenance statistics

RECMS record maintenance statistics

REQMS request for maintenance statistics

RETAIN Remote Technical Assistance Information Network

RFS ready for sending (signal) (or clear to send CTS)

RH request/response header

RI 1) register to immediate operand (instruction)
2) ring indicator (same as CI)

RIM request initialization mode (SDLC)

RLSD receive line signal detector

RNIO OS/VS VTAM IO trace

ROK read-only key

ROS read-only storage

ROSAR read-only storage address register

rpm revolutions per minute

RPO 1) remote power-off
2) request power-off

RPQ request for price quotation

RR register-to-register (instruction)

RS register-to-storage (instruction)

RSA register-to-storage with addition (instruction)

RSET receive signal element timing (same as RC)

RSF remote support facility

RTC retry count (X.21)

RTM retry timer (X.21)

RTS request to send (signal)

RU request/response unit (SNA)

RVI reverse interrupt (BSC)

R/W read/write

s second

SAC storage and control board assembly

SACL storage and control lower assembly for 3745 models 21x and 41x

SACU storage and control upper assembly for 3745 models 21x and 41x

SACL2 storage and control lower assembly for 3745 models 31x and 61x

SACU2 storage and control upper assembly for 3745 models 31x and 61x

SALT stand-alone link test

SAR storage address register

SAT specific assurance test

SCB scanner control block (storage)

SCF secondary control field (storage)

SCP signal converter product (or DCE)

SCR 1) subtract character register (instruction)
2) serial clock receive (signal)

SCT serial clock transmit (signal)

SCTL storage control card for 3745 models 21A and 41A

SCTL2 storage control card for 3745 models 31x and 61x

SCTL3 storage control card for 3745 models 31A and 61A

SD send data (signal)

SDF serial data field (storage)

SDLC Synchronous Data Link Control

SE system engineer

SES secondary status (storage)

SET signal element timing (signal)

SHM short hold mode

SHR subtract halfword register (instruction)

SI select in

SIDI serial in data in

SIM set initialization mode (SDLC)

SIO start input/output

SIT scanner interface trace

SKA storage key address

SKDR storage-protect key data register

SL serial link

SMPS switching module power supply

SMUXA single multiplex card for lower board on LIC 2

SMUXB single multiplex card for upper board on LIC 2

SNA Systems Network Architecture

SNRM set normal response mode (SDLC)

SO select out

SODO serial out data out

SOH start of heading (BSC)

SP storage protect

SPAE storage protect/ address exception

SPDn signal and power distribution card

SPK storage protect key

SPS service and power support

SR subtract register (instruction)

SRC system reference code

SRI subtract register immediate (instruction)

SRL shift register latch

SS start-stop

SSA system services architecture

SSB system status block

SSCP system services control point

SSP system support programs

ST store (instruction)

STAT0 status 0 register

STAT1 status 1 register

STAT4 status 4 register

STC store character (instruction)

STCT store character and count (instruction)

STER switch terminator

STH store halfword (instruction)

STG storage

STO storage (card)

STX start of text (BSC)

SVC supervisor call

SW switch

SWAD MOSS/SWL adapter

SWER switch error register

SWL switching logic

SWLA switching logic A

SWLB switching logic B

SYN synchronous idle (BSC)

SYSGEN system generation

T transmit (signal)

TA tag address

TAP trace analysis program

TAR temporary address register

TB terminator block

TC transmit clock

TCAM Telecommunications Access Method

TCB task control block

TCC trace correlation counter (storage)

TCM 1) thermal conduction module
2) treillis coded modulation

TCP test connector pin

TCS two-channel switch

TCTR transient error counter

TD 1) tag data
2) transmitted data (signal)

TERM terminator

TG transmission group

TH transmission header

TI test indicator (signal)

TIC token-ring interface coupler

TIC1 token-ring interface coupler type 1 (card)

TIC2 token-ring interface coupler type 2 (card)

TICB trace interface control block

TIO test I/O

TLNVT trace line vector table

TOD time of day

TPF transaction process facility

TPS two-processor switch

TPSA trace parameter status area

TRA token-ring adapter

TRM 1) token-ring multiplexer card that controls up to two TICs
2) test register under mask (instruction)

TRP token-ring processor

TRSS token-ring subsystem

TRU trace record unit

TSET transmitter signal element timing (signal, same as TC)

TSS transmission subsystem

TSSB FRU name for LA board (basic) with no TRA adapters

TSST FRU name for LA board (basic) with TRA adapters

TTA translate table area

TTD temporary text delay (BSC)

T1 US service for very high speed transmissions at 1.5 million bps

UA unnumbered acknowledgment (SDLC)

UC universal controller

UCW unit control word

UE unit exception (channel status)

UEPO unit emergency power-off

UK United Kingdom

UKA user key address

UKP user key program

UKDR user key data register

UKL user key level interrupt

URSF universal remote support facility

USASCII (see *ASCII*)

μs microsecond

uv undervoltage

V volt

VB valid byte (signal)

VAC volts, alternating current

VCNA VTAM node control application

VDC volts, direct current

VFO variable frequency oscillator

VH valid halfword (signal)

VPD vital product data

VRC vertical redundancy check

VS virtual storage

VSE Virtual Storage Extended

VTAM Virtual Telecommunications Access Method

V.24 CCITT V.24 recommendation

V.25 CCITT V.25 recommendation

V.28 CCITT V.28 recommendation

V.35 CCITT V.35 recommendation

W watt

WACK wait before transmit positive acknowledgment (BSC)

WB wrapback (signal)

WLOB wire lobe (cable connecting token-ring adapters to token-ring access units)

WKR work register

WSDR wide storage data register

XI X.25 SNA interconnection

XID exchange identification

XCR exclusive OR character register (instruction)

XHR exclusive OR halfword register (instruction)

XOR exclusive OR

XR exclusive OR register (instruction)

XREG external registers

XRI exclusive OR register immediate (instruction)

X.21 CCITT X.21 recommendation

X.25 CCITT X.25 recommendation

YZxxx wiring diagram

ZI zero insert

ZREG Z register

Glossary

This glossary defines all new terms used in this manual. It also includes terms and definitions from the *IBM Dictionary of Computing,* GC20-1699.

adapter-initiated operation (AIO). A transfer of up to 256 bytes between an adapter (CA or LA) and the CCU storage. The transfer is initiated by an IOH/IOHI instruction, and is performed in cycle stealing via the IOC bus.

addressing. A technique where the control station selects, among the DTEs that share a transmission line, the DTE to which it is going to send a message.

alarm. A message sent to the MOSS console. In case of an error a reference code identifies the nature of the error.

alert. A message sent to the host console. In case of an error a reference code identifies the nature of the error.

asynchronous transmission. Transmission in which each character is individually synchronized, usually by the use of start and stop elements. The start-stop link protocol, for example, uses asynchronous transmission. Contrast with *synchronous transmission*.

auto-answer. A machine feature that allows a DCE to respond automatically to a call that it receives over a switched line.

auto-call. A machine feature that allows a DCE to initiate a call automatically over a switched line.

autoBER. A program to automatically analyse a BER file.

automaint. A function that uses autoBER to isolate failing FRUs.

availability. The degree to which a system or resource is ready when needed to process data.

buffer chaining channel adapter (BCCA). A channel adapter that handles buffer chaining in write channel program and both buffer chaining and PIU chaining in read channel program. BCCA works only under NCP.

Bell 212A. Bell recommendations on transmission interface

binary synchronous communication (BSC). A uniform procedure, using standardized set of control characters and character sequences, for synchronous transmission of binary-coded data between stations.

box event record (BER). Information about an event detected by the controller. It is recorded on the disk/diskette and can be displayed on the operator console for event analysis.

block multiplexer channel. A multiplexer channel that interleaves blocks of data. See also *byte multiplexer channel*. Contrast with *selector channel*.

byte multiplexer channel. A multiplexer channel that interleaves bytes of data. See also *block multiplexer channel*. Contrast with *selector channel*.

cache. A high-speed buffer storage that contains frequently accessed instructions and data; it is used to reduce access time.

central control unit (CCU). In the 3745, the controller hardware unit that contains the circuits and data flow paths needed to execute instructions and to control its storage and the attached adapters.

channel. A one-way path between a host and the controller.

channel adapter (CA). A communication controller hardware unit used to attach the controller to a host processor.

channel interface. The interface between the controller and the host processors.

clear channel. Mode of data transmission where the data passes through the DCE and network, and arrives at the receiving communication controller (for example, the IBM 3745) unchanged from the data transmitted. The DCE or network can modify the data during transmission because of certain network restrictions, but must ensure the received data stream is the same as the transmitted data stream.

command list. In NetView, a sequential list of commands and control statements that is assigned a name. When the name is invoked (as a command) the commands in the list are executed.

communication common carrier. In the USA and Canada, a public data transmission service that provides the general public with transmission service facilities. For example, a telephone or telegraph company (see also *Post Telephone and Telegraph* for countries outside the USA and Canada).

communication controller. A communication control unit that is controlled by one or more programs stored and executed in the unit. Examples are the IBM 3705, IBM 3725/3726, IBM 3720, and IBM 3745.

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communication network management (CNM) application program. An ACF/VTAM application program authorized to issue formatted management services request units containing physical-unit-related requests and to receive formatted management services request units containing information from physical units.

communication scanner. See *scanner*.

communication scanner processor (CSP). The processor of a scanner.

common customer profile facility (CCPF). It is used to create customer profile records for new IBM customers. The records then form the customer profile library, which includes the customer's data processing site, machines and programs used, IBM branch, region, and support center servicing.

communication subsystem. The part of the controller that controls the data transfers over the transmission interface.

configuration data file (CDF). A MOSS file that contains a description of all the hardware features (presence, type, address, and characteristics).

control panel. A panel that contains switches and indicators for the use of the customer's operator and service personnel.

control program. A computer program designed to schedule and to supervise the execution of programs of the controller.

control subsystem (CSS). The part of the controller that stores and executes the control program, and monitors the data transfers over the channel and transmission interfaces.

customer engineer (CE). See *IBM service representative*

cyclic redundancy check. A system of error checking performed at both the sending and receiving station after a block check character has been accumulated.

cyclic redundancy check character (CRC). A character used in a modified cyclic code for error detection and correction.

data circuit-terminating equipment (DCE). The equipment installed at the user's premises that provides all the functions required to establish, maintain, and terminate a connection, and the signal conversion and coding between the data terminal equipment (DTE) and the line. For example, a modem is a DCE (see *modem*.)

Note: The DCE may be separate equipment or an integral part of other equipment.

data communication channel. See *channel*.

data host. A host running application programs only.

data terminal equipment (DTE). That part of a data station that serves as a data source, data sink, or both, and provides for the data communication control function according to protocols.

DIN. Technology of connector contacts.

direct attachment. The attachment of a DTE to another DTE without a DCE.

direct-current interlock (DCI). A mode of data transfer over an I/O interface to enable communication between data processing systems through a channel.

diskette. A thin, flexible magnetic disk, and its protective jacket, that records diagnostics, microcode, and 3745 files.

diskette drive. A mechanism that reads and writes diskettes.

DOS/VS. Disk Operating System/Virtual Storage.

duplex transmission. Data transmission in both directions at the same time. Contrast with *half-duplex*.

Emulation Program (EP). An IBM licensed program that allows a channel-attached communication controller to emulate the functions of an IBM 2701 Data Adapter Unit, an IBM 2702 Transmission Control, or an IBM 2703 Transmission Control.

error recovery procedure (ERP). A procedure designed to help isolate and, where possible, to recover from errors in equipment. The procedures are often used in conjunction with programs that record the information on machine malfunctions.

Ethernet line adapter (ELA). Ethernet-type LAN line adapter composed of a CSP card and an EAC card.

Ethernet subsystem (ESS). The part of the controller that controls the data transfers over the Ethernet-type LAN.

The ESS consists of up to eight Ethernet line adapters (ELAs).

fallback. In twin-backup mode, a state where the traffic of the failing CCU has been redirected to the second one.

In standby mode, a state where the traffic of the failing CCU has been redirected to the standby CCU after it is IPLed.

front-end scanner (FES). A circuit that scans the transmission lines, serializes and deserializes the transmitted characters, and manages the line services. It is part of the scanner.

half-duplex. Data transmission in either direction, one direction at a time. Contrast with *duplex*.

high-performance transmission subsystem (HPTSS). The part of the controller that controls the data transfers over the high-speed transmission interface (speed up to 2 million bps).

The HPTSS consists of up to eight high-speed scanners (HSSs).

high-speed scanner. Line adapter for lines up to 2 million bps, composed of a communication scanner processor (CSP) and a front-end high-speed scanner (FESH).

high-speed transfer. A mode of high-speed data transmission over an I/O interface to enable communication between data processing systems through a channel.

hit. In cache operation, indicates that the information is in the cache storage.

host processor. 1) A processor that controls all or part of a user application netwo rk. 2) In a network, the processing unit in which the access method for the network resides. (3) In an SNA network, the processing unit that contains a system services control point (SSCP). (4) A processing unit that executes the access method for attached communication controllers. Also called *host.*

IBM service representative. An individual in IBM who performs maintenance services for IBM products or systems.

initial microcode load (IML). The process of loading the microcode into a scanner or into MOSS.

initial program load (IPL). The initialization procedure that causes 3745 control program to commence operation.

input/output control (IOC). The circuit that controls the input/output from/to the channel adapters and scanners via the IOC bus.

internal clock function. A LIC function that provides a transmit clock for sending data, and retrieves a receive clock from received data, when the modem does not provide those timing signals. When the terminal is connected in direct-attach mode (without modem) the ICF also provides the transmit and receive clocks to the terminal, via the LIC card.

internal function test (IFT). A set of diagnostic programs designed and organized to detect and isolate a malfunction.

LIC module. A group of four adjacent LICs.

LIC unit. A line interface coupler unit (LIU) consisting of:

- One power supply (PS) associated with
- Two LIC boards (LIBs), housing
- Multiplex cards (DMUX, SMUXA, or SMUXB), and
- Line interface coupler cards (LICs)

line. See *transmission line*.

line adapter (LA). The part of the TSS, HPTSS, or TRSS that scans and controls the transmission lines. Also called *scanner*.

For the TSS the line adapters are low-speed scanners (LSSs).

For the HPTSS the line adapters are high-speed scanners (HSSs).

For the TRSS the line adapters are token-ring adapters (TRAs).

line interface coupler (LIC). A circuit that attaches up to four transmission cables to the controller.

Link Problem Determination Aid (LPDA). A set of test facilities resident in the IBM 386X/586X modems and activated from the control program in the controller and from host.

link protocol. The set of rules by which a logical data link is established, maintained, and terminated, and by which data is transferred across the link.

Logrec. Error logging program managed via the operating system.

longitudinal redundancy check (LRC). A system of error checking performed at the receiving station after a block check character has been accumulated.

low-speed scanner. Line adapter for lines up to 256 kbps, composed of a communication scanner processor (CSP) and a front-end low-speed scanner (FESL).

maintenance and operator subsystem (MOSS). The part of the controller that provides operating and servicing facilities to the customer's operator and the IBM service representative.

microcode. A program, that is loaded in a processor (for example, the MOSS processor) to replace a hardware function. The microcode is not accessible to the customer.

miss. In cache operation, indicates that the information is not in the cache storage.

modem (modulator-demodulator). A functional unit that transforms logical signals from a DTE into analog signals suitable for transmission over telephone lines (modulation), and conversely (demodulation). A modem is a DCE. It may be integrated in the DTE.

MOSS input/output control (MIOC). The circuit that controls the input/output from/to the MOSS.

multiplexer channel. A channel designed to operate with a number of I/O devices simultaneously. Several I/O devices can transfer records at the same time by interleaving items of data. See also *byte multiplexer, block multiplexer*.

multiplexing. In data transmission, a function that permits two or more data sources to share a common transmission medium so that each data source has its own channel.

multipoint connection. A connection established for data transmission among more than two data stations. The connection may include switching facilities.

NetView. An IBM licensed program used to monitor a network, manage it, and diagnose its problems.

network. See *user application network*.

Network Control Program (NCP). An IBM licensed program that provides communication controller support for single-domain, multiple-domain, and interconnected network capability.

nonswitched line. A connection between systems or devices that does not have to be made by dialing. The connection can be point-to-point or multipoint. The line can be leased or private. Contrast with *switched line.*

online tests. Testing of a remote data station concurrently with the execution of the user's programs (that is, with only minimal effect on the user's normal operation).

Operating System/Virtual Storage (OS/VS). A family of operating systems that control IBM System/360 and System/370 computing systems. OS/VS includes VS1, VS2, MVS/370, and MVS/XA:

operator console. The IBM Operator Console that is used to operate and service the 3745 through the MOSS. A local console must be located within 7 m of the 3745. Optionally an alternate console may be installed up to 120 m from the 3745, or a remote console may be connected to the 3745 through the switched network.

owning host. A host which can IPL a 3745 and also run application programs.

partitioned emulation programming (PEP) extension. A function of a network control program that enables a communication controller to operate some telecommunication lines in network control mode while simultaneously operating others in emulation mode.

phototransistor. An electronic part used to sense the light of a light-emitting diode.

point-to-point connection. A connection established between two data stations for data transmission. The connection may include switching facilities.

polling. The process whereby remote stations are invited, one at a time, to transmit.

post telephone and telegraph (PTT). A generic term for the government-operated common carriers in countries other than the USA and Canada. Examples of the PTT are British Telecom in the United Kingdom, Deutsche Bundespost in Germany, and Nippon Telephone and Telegraph Public Corporation in Japan.

program-initiated operation (PIO). A transfer of four bytes between a general register in the CCU and an adapter (channel or scanner). The transfer is initiated by IOH/IOHI instruction and is executed via the IOC bus.

reliability. The ability of a functional unit to perform a required function under stated conditions, for a stated period of time.

scanner. A device that scans and controls the transmission lines. Also called *line adapter*.

selector channel. An I/O channel designed to operate with only one I/O device at a time. Once the I/O device is selected, a complete record is transferred one byte at a time. Contrast with *block multiplexer channel, multiplexer channel*.

services. A set of functions designed to facilitate the maintenance of a device or system.

serviceability. The capability to perform effective problem determination, diagnosis, and repair on a data processing system.

single. Configuration with one CCU

start-stop. A data transmission system in which each character is preceded by a start signal and is followed by a stop signal.

switchback. Operation to reset a twin-backup configuration from fallback to initial state.

switched line. A transmission line with which the connections are established by dialing, only when data transmission is needed. The connection is point-to-point and uses a different transmission line each time it is established. Contrast with *nonswitched line*.

Synchronous Data Link Control (SDLC). A discipline conforming to subsets of the Advanced Data Communication Control Procedures (ADCCP) of the American National Standards Institute (ANSI) and High-level Data Link Control of the International Organization for Standardization, for managing synchronous, code-transparent, serial-by-bit information transfer over a link connection. Transmission exchanges may be duplex or half-duplex over switched or nonswitched links. The configuration of the link connection may be point-to-point, multipoint, or loop.

synchronous transmission. Data transmission in which the sending and receiving instruments are operating continuously at substantially the same frequency and are maintained, by means of correction, in a desired phase relationship. Contrast with *asynchronous transmission*.

Systems Network Architecture (SNA). The description of the logical structure, formats, protocols, and operational sequences for transmitting information through a user application network. The structure of SNA allows the users to be independent of specific telecommunication facilities.

time out. The time interval allotted for certain operations to occur.

token-ring subsystem (TRSS). The part of the controller that controls the data transfers over an IBM Token-Ring Network.

The TRSS consists of up to four token-ring adapters (TRAs).

token-ring adapter (TRA). Line adapter for an IBM Token-Ring Network, composed of one token-ring multiplexer card (TRM), and two token-ring interface couplers (TICs).

The TRSS consists of up to four token-ring adapters (TRAs).

transmission interface. The interface between the controller and the user application network.

transmission line. The physical means for connecting two or more DTEs (via DCEs). It can be nonswitched or switched. Also called *line*.

transmission subsystem (TSS). The part of the controller that controls the data transfers over low- and medium-speed, switched and non switched transmission interfaces.

The TSS consists of:

- Up to 32 low-speed scanners (LSSs) associated with
- LIC units (LIUs), through
- Serial links (SLs).

TSST board. line adapter board for token-ring adapters

twin. Configuration with two CCUs.

twin-dual. Mode of operation with two CCUs operating simultaneously in two distinct subareas.

twin-backup. Mode of operation identical to twin-dual with fallback capability.

twin-standby. Mode of operation with one CCU active and the other in standby, ready to take over.

two-processor switch (TPS). A feature of the channel adapter that connects a second channel to the same adapter.

user application network. A configuration of data processing products, such as processors, controllers, and terminals, for the purpose of data processing and information exchange. This configuration may use circuit-switched, packet-switched, and leased-circuit services provided by carriers or the PTT. Also called *user network*.

vertical redundancy check (VRC). An odd parity check performed on each character of a block as the block is received.

V.24. CCITT V.24 recommendation

V.25. CCITT V.25 recommendation

V.28. CCITT V.28 recommendation

V.35. CCITT V.35 recommendation

X.20. CCITT X.20 recommendation

X.21. CCITT X.21 recommendation

X.21 bis. CCITT X.21 bis recommendation

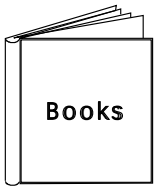
X.25. CCITT X.25 recommendation

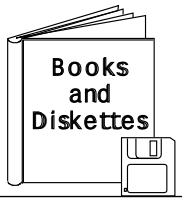
Bibliography

Customer Documentation for the 3745 (Models 210, 21A, 310, 31A, 410, 41A, 610, and 61A) and 3746 (Model 900)

Table X-1 (Page 1 of 4). Customer Documentation for the 3745 Models X10 and X1A, and 3746 Model 900

This customer documentation has the following formats:

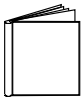




Finding Information

3745 Models A and 3746 Books

Starting with engineering change (EC) F12380, all of the books in the 3745 Models A and 3746 library are available on the CD-ROM that contains the Licensed Internal Code (LIC) for this EC.



SA33-0172

IBM 3745 Communication Controller
Models 210 to 61A
IBM 3746 Expansion Unit Model 900

Customer Master Index[1]

Provides references for finding information in the customer documentation library.

Evaluating and Configuring

GA33-0092

IBM 3745 Communication Controller
Models 210, 310, 410, and 610

Introduction

Gives an introduction about the IBM Models 210 to 610 capabilities.

For Models A refer to the *Overview*, GA33-0180.

GA33-0180

IBM 3745 Communication Controller Models A[2]
IBM 3746 Nways Multiprotocol Controller
Models 900 and 950

Overview

Gives an overview of connectivity capabilities within SNA, APPN, and IP networking.

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Table X-1 (Page 2 of 4). Customer Documentation for the 3745 Models X10 and X1A, and 3746 Model 900

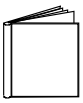
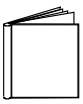
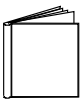
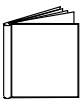
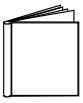
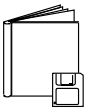
	GA33-0457	***IBM 3745 Communication Controller Models A***[2] ***IBM 3746 Expansion Unit Model 900*** ***Models 900 and 950*** ***Planning Guide*** Planning for: • Field upgrades • Service processor and alert management configuration • Network integration (NCP, APPN, and IP control) • Physical installation.
Preparing Your Site		
	GC22-7064	***IBM System/360, System/370, 4300 Processor*** ***Input/Output Equipment Installation Manual-Physical Planning*** (Including Technical News Letter GN22-5490) Provides information for physical installation for the 3745 Models 130 to 610. For 3745 Models A and 3746 Model 900, refer to the *Planning Guide*, GA33-0457.
	GA33-0127	***IBM 3745 Communication Controller*** ***Models 210, 310, 410, and 610*** ***Preparing for Connection*** Helps for preparing the 3745 Models 210 to 610 cable installation. For 3745 Models A refer to the *Connection and Integration Guide*, SA33-0129.
Preparing for Operation		
	GA33-0400	***IBM 3745 Communication Controller All Models***[3] ***IBM 3746 Nways Multiprotocol Controller*** ***Models 900 and 950*** ***Safety Information***[1] Provides general safety guidelines.
	SA33-0129	***IBM 3745 Communication Controller All Models***[3] ***IBM 3746 Nways Multiprotocol Controller Model 900*** ***Connection and Integration Guide***[1] Contains information for connecting hardware and integrating network of the 3745 and 3746-900 after installation.
	SA33-0416	***Line Interface Coupler Type 5 and Type 6*** ***Portable Keypad Display*** ***Migration and Integration Guide*** Contains information for moving and testing LIC types 5 and 6.
	SA33-0158	***IBM 3745 Communication Controller All Models***[3] ***IBM 3746 Nways Multiprotocol Model 900*** ***Console Setup Guide***[1] Provides information for: • Installing local, alternate, or remote consoles for 3745 Models 130 to 610 • Configuring user workstations to remotely control the service processor for 3745 Models A and 3746 Model 900 using: – DCAF program – Telnet Client program.
Customizing Your Control Program		

Table X-1 (Page 3 of 4). Customer Documentation for the 3745 Models X10 and X1A, and 3746 Model 900

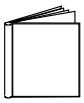
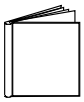
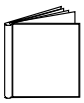
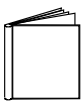
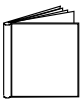
	SA33-0178	***Guide to Timed IPL and Rename Load Module*** Provides VTAM procedures for: • Scheduling an automatic reload of the 3745 • Getting 3745 load module changes transparent to the operations staff.
Operating and Testing		
	SA33-0098	***IBM 3745 Communication Controller*** ***All Models***[4] ***Basic Operations Guide***[1] Provides instructions for daily routine operations on the 3745 Models 130 to 610.
	SA33-0177	***IBM 3745 Communication Controller Models A***[2] ***IBM 3746 Nways Multiprotocol Controller Model 900*** ***Basic Operations Guide***[1] Provides instructions for daily routine operations on the 3745 Models 17A to 61A, and 3746 Model 900 operating as an SNA node (using NCP), APPN/HPR Network Node and IP Router.
	SA33-0097	***IBM 3745 Communication Controller*** ***All Models***[3] ***Advanced Operations Guide***[1] Provides instructions for advanced operations and testing, using the 3745 MOSS console.
	On-line Information	***Controller Configuration and Management Application*** Provides a graphical user interface for configuring and managing a 3746 APPN/HPR Network Node and IP Router, and its resources. Is also available as a stand-alone application, using an OS/2 workstation. Defines and explains all the 3746 Network Node and IP Router configuration parameters through its on-line help.
	SH11-3081	***IBM 3746 Nways Multiprotocol Controller*** ***Models 900 and 950*** ***Controller Configuration and Management: User's Guide***[5] Explains how to use CCM and gives examples of the configuration process.
Managing Problems		
	SA33-0096	***IBM 3745 Communication Controller*** ***All Models***[3] ***Problem Determination Guide***[1] A guide to perform problem determination on the 3745 Models 130 to 61A.
	On-line Information	***Problem Analysis Guide*** An on-line guide to analyze alarms, events, and control panel codes on: • IBM 3745 Communication Controller Models A[2] • IBM 3746 Nways Multiprotocol Controller Models 900 and 950.

Table X-1 (Page 4 of 4). Customer Documentation for the 3745 Models X10 and X1A, and 3746 Model 900



SA33-0175

IBM 3745 Communication Controller Models A[2]
IBM 3746 Expansion Unit Model 900
IBM 3746 Nways Multiprotocol Controller Model 950

Alert Reference Guide

Provides information about events or errors reported by alerts for:

- IBM 3745 Communication Controller Models A[2]
- IBM 3746 Nways Multiprotocol Controller Models 900 and 950.

[1] Documentation shipped with the 3745.
[2] 3745 Models 17A to 61A.
[3] 3745 Models 130 to 61A.
[4] Except 3745 Models A.
[5] Documentation shipped with the 3746-900.

Service Documentation for the IBM 3745 (Models 210, 21A, 310, 31A, 410, 41A, 610, and 61A) and 3746 (Model 900)

Table X-2 (Page 1 of 4). Service Documentation for the 3745 Models X10 and X1A, and 3746 Model 900

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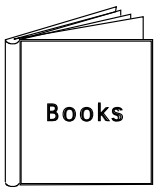
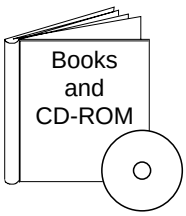
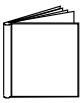




SY33-2080	***IBM 3745 Communication Controller Models 210 to 61A*** ***Service Master Index***[1] Provides references for finding information in the IBM 3745 Models X10 and X1A shipping group documentation.
SY33-2057	***IBM 3745 Communication Controller Models 210 to 61A*** ***Installation Guide***[1] Provides instructions for installing or relocating the IBM 3745 Models X10 and X1A.
SY33-2114	***IBM 3746 Nways Multiprotocol Controller Model 900*** ***Installation Guide***[2] Provides instructions for installing or relocating a 3746-900.
SY33-2116	***IBM 3746 Nways Multiprotocol Controller Model 900*** ***Service Guide***[2] Provides procedures for isolating and fixing the IBM 3746-900 problems.
SY33-2055	***IBM 3745 Communication Controller Models 210, 310, 410, and 610*** ***IBM 3746 Expansion Units Models A11, A12, L13, L14, and L15*** ***Service Functions***[1] Describes MOSS functions using the IBM 3745 Models X10 and X1A consoles.
SY33-2054	***IBM 3745 Communication Controller Models 210 to 61A*** ***Maintenance Information Procedures***[1] Provides procedures for isolating and fixing the IBM 3745 Models X10 and X1A problems.

Table X-2 (Page 2 of 4). Service Documentation for the 3745 Models X10 and X1A, and 3746 Model 900

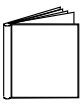


SY33-2115

***IBM 3745 Communication Controller Models A*[3]**
IBM 3746 Expansion Unit Model 900
IBM 3746 Nways Multiprotocol Controller Model 950

***Service Processor Installation and Maintenance*[4]**
(Based on the 7585, 3172, 9585, or 9577)

Provides information on installing and maintaining the service processor based on PS/2 Types 7585, 3172, 9585, or 9577.
Can be for systems with microcode that has up to and including EC D46130 (any level) installed.

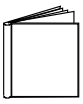


SY33-2120

***IBM 3745 Communication Controller Models A*[3]**
IBM 3746 Expansion Unit Model 900
IBM 3746 Nways Multiprotocol Controller Model 950

***Service Processor Installation and Maintenance*[4]**
(Based on the 7585, 3172, or 9585)

Provides information on installing and maintaining the service processor based on PS/2 Types 7585, 3172, or 9585.
Can be for systems with microcode EC F12380 or higher installed.

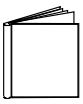


SY33-2118

IBM 3746 Nways Multiprotocol Controller Models 900 and 950

***Multiaccess Enclosure Installation and Maintenance*[4]**

Provides information on installing and maintaining the Multiaccess Enclosure (MAE).

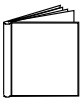


SY33-2112

IBM 3746 Nways Multiprotocol Controller
Models 900 and 950

***Network Node Processor Installation and Maintenance*[4]**
(Based on the 7585 or 3172)

Provides information on installing and maintaining the network node processor based on the PS/2 Type 7585 or 3172.

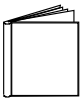


SY33-2056

IBM 3745 Communication Controller
Models 210 to 61A

***Maintenance Information Reference*[1]**

Provides in-depth hardware reference information on the IBM 3745 Models X10 and X1A.

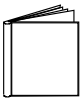


SY33-2075

IBM 3745 Communication Controller
***All Models*[6]**

***External Cable References*[1]**

Provides references to console and line cables used for connecting the IBM 3745 Models 130 to 61A.



SY33-2117

IBM 3746 Nways Multiprotocol Controller
Models 900 and 950

***External Cable Reference*[7]**

Provides references to console and line cables used for connecting the IBM 3746 Models 900 and 950.

Table X-2 (Page 3 of 4). Service Documentation for the 3745 Models X10 and X1A, and 3746 Model 900

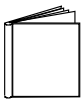
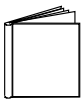
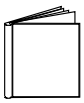
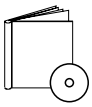
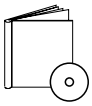
	S135-2015	***IBM 3746 Nways Multiprotocol Controller Models 900 and 950*** ***Parts Catalog***[7] Provides reference information for ordering parts for the IBM 3746 Models 900 and 950.
	S135-2010	***IBM 3745 Communication Controller Models 210 to 61A*** ***Parts Catalog***[1] Provides reference information for ordering IBM 3745 Models X10 and X1A parts.
	S135-2014	***IBM Controller Expansion*** ***Parts Catalog*** Provides reference information for ordering parts for the controller expansion attached to the IBM 3745 Models A[3], and 3746 Models 900 and 950.

Table X-2 (Page 4 of 4). Service Documentation for the 3745 Models X10 and X1A, and 3746 Model 900

CD-ROM Bibliography		
	ZK2T-8214	***IBM Networking*** ***Softcopy Collection Kit*** Allows service manuals consulting via CD-ROM viewer. EMEA version.
	ZK2T-8187	***IBM Networking*** ***Softcopy Collection Kit*** Allows service manuals consulting via CD-ROM viewer. US version.

[1] Documentation shipped with the 3745.
[2] Documentation shipped with the 3746-900.
[3] 3745 Models 17A to 61A.
[4] Documentation shipped with the processor.
[5] Product integrated information
[6] 3745 Models 130 to 61A.

Index

Numerics

A

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B

C

D

E

F

G

H

I

K

L

M

N

O

P

R

S

T

U

V

W

X

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IBM 3745 Communication Controller
Models 210 to 61A
Maintenance Information Reference
Part 2

Publication No. SY33-2056-8

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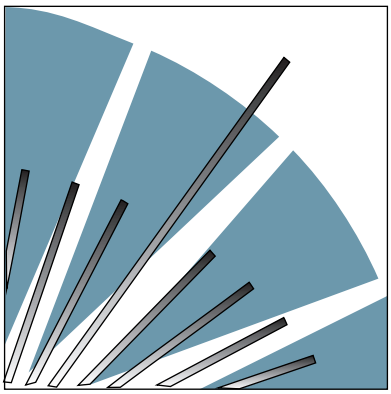

26F1660

SY33-2056-8